

THE MEASURING STANDS FOR MEASURE OF AD CONVERTERS

Linus MICHAELI, Marek GODLA, Ján ŠALIGA, Jozef LIPTAK

Dept. of Electronics and Multimedia Communications, FEI TU of Košice, Slovak Republic,
linus.michaeli@tuke.sk

Abstract: AD converters are the key components in the data acquisition systems. Therefore their accuracy is very important for end users. Teaching and practical experiments of the testing methods are time consuming and requires precise laboratory equipment with the access for students. This paper presents measuring workplace with real circuits of the AD converter. Workplace will contain two AD converters one as subject of testing and second for assessment of its modalities. Workplace will be accessible students remotely through html protocol. Measuring stand is designed in the LabVIEW environment as one workplace of more remotely accessible stands devoted for electronic laboratory training

Keywords: LabVIEW programming, laboratory controlled remotely, ADC testing.

1. INTRODUCTION

Study of elementary electronics is often difficult for lack of time for simulations and testing. Especially AD converters are devices which need more time for better understanding of testing procedures. Students have limited possibilities to connect real AD converter and to evaluate practically their knowledge about application of AD converters in real data acquisition systems and assessment of their metrological properties.

This paper present workplace with two AD converters connected separately to one measuring PC card. Scope of the first ADC is to serve as subject for testing of the functional parameters like integral $INL[k]$ and differential $DNL[k]$ nonlinearities. Second ADC will serve for ADC testing where user can change of converter parameters. The remote control of ADC parameters allows students to understand how ADCs work.

2. DESIGN OF WORKPLACE

Workplace will use measuring card with analog and digital inputs and outputs. As AD converters will use a circuit AD574A. The AD574A is a 12-bit successive-approximation analog-to-digital converter with 3-state output buffer circuitry for direct interface to an 8- or 16-bit microprocessor bus. A high precision voltage reference and clock are included on-chip, and the circuit guarantees full-

rated performance without external circuitry or clock signals [1].

The figure (Fig.1) shows the proposed the first workplace dedicated for training of dynamic and static testing procedures. The upper part on the Fig.1, allows to perform dynamic tests based on the FFT and probabilistic analysis. The lower part allows students perform static AD converter tests. Both parts are controlled by the card PCI 6251. The NI PCI-6251 is a high-speed measure card with two 16-bit analog outputs (2.8 MS/s); 24 digital I/O; 32-bit counters, correlated DIO (8 clocked lines, 10 MHz); analog and digital triggering. The main deal of this measure card is realize FFT measuring and setup basic conditions of ADC DUT2.

Measuring working place allows to perform three laboratory tasks.

1. The objective of the first task is to measure ADC characteristic by the static testing method.
2. The second working task is impenletation of dynamic testing methods using FFT analysis.
3. The objective of third laboratory tasks which can be performed remotely is assessment of the ADC behaviours under various working conditions adjusted through the control input. The final ADC characteristic under selected working conditions is being tested by dynamic method using the second working stand.

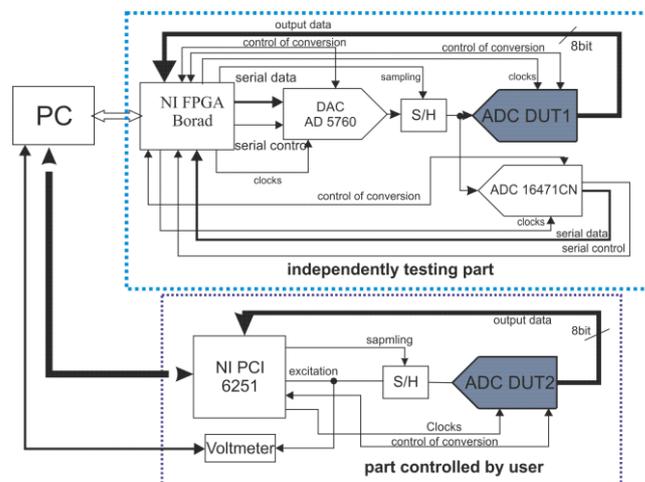


Fig. 1 Layout of the measuring workplace

The static method testing methods is based on the looking for the DC voltage at the input of ADC DUT1 when probabilities of the neighboring codes k , $k+1$ are close to 50%. The task of the implemented FPGA is performing of the algorithm which looks for the right transition level $T(k)$ at the input of ADC DUT1 for any code value k . The digital code k is transformed into analog stimulus value by the DA converter AD 5760. The excitation analog signal is connected at the inputs of two AD converters first tested ADC DUT1 and second one reference AD converter ADC 16471. The static test method requires measurement of excitation voltage with the higher accuracy as ADC DUT1. The measuring ADC brings digital value representing the excitation DC voltage $T[k]$ back to the FPGA circuit. The testing procedure is performed independently by FPGA circuit. It controls digital value at the input of excitation DAC iteratively until the probabilities of two neighboring codes are quite equal. At the end of the iteration procedure transmits FPGA circuit at the PC probabilities of the last iteration cycle and corresponding DC voltage from the reference converter ADC 16471. By using this circuit we reduce time of testing and power of PC processor.

The reference AD converter ADC 16471 is $\Sigma\Delta$ ADC with resolution 16 bit and low nonlinearity error. Longer conversion time is not an obstacle in the testing procedure.

NI FPGA board by National Instruments is used As FPGA circuits. NI FPGA board contains Xilinx XC3S500E-4FTG256C with 10,476 logic cells. The downloading and debugging of the configuration program is performed through USB-based FPGA/CPLD interface. The maximal clock frequency of the inputs/outputs connection is 50MHz. The FPGA circuit create clock signal, sampling signal and collect digital data from the ADC. The acquired data are later transmitted to the PC where the data are recorded in a file. The recorded files are available for successive elaboration by the appropriate dynamic tests defined by standards [2], [5]. There is no possibility of the unauthorized control FPGA circuits by the user. FPGA is programmed and operative alone.

The second working task is accomplished by the stand, where AD converter under test (ADC DUT2) is stimulated by the harmonic signal with adjustable amplitude and frequency. Signal generated by the PC is converted in the analog form by the analog board NI PCI 6251. Maximum differential nonlinearity of ADC in the NI PCI 6251 card defined by manufacturer is ± 1 LSB and integral nonlinearity is 64 ppm of range.

The stimulating DA converter has higher resolution and its nonlinearities are lower as expected nonlinearities of the tested AD converters.

Third working task is devoted for the training of the ADC implementation under various working conditions. The working stand is shown in Fig.1 Working modes are selected remotely through the other outputs of DAQ NI PXI 6533 card at the ADC DUT2 and is depicted by the dashed line. The FFT testing utility is used for the evaluation of ADCV characteristics under changed working conditions. The card allows to set up control signals of the various modalities at the appropriate control inputs of tested ADC DUT2. The user has possibility to study how various

modalities of ADC could be settled. The possible nodes for selection are:

- input offset and gain
- switching of 8 or 12 bit operation mode
- selection for unipolar and bipolar mode of conversion.
- input analog voltage range
- chip select node (CS)
- read/convert node (RC)
- sampling frequency for sample and hold circuit

User fully controls ADC DUT2 by the input control bits. The program obtain several preprogrammed modes of working ADC, also there is possible to create own working modes.

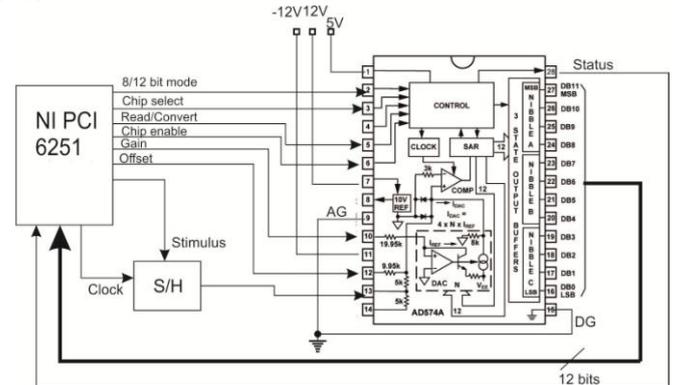


Fig.2 Schematic second part of working stand

The DAQ card NI PCI 6251 allows to generate stimulus signal of various forms of the stimulus signal which are popular for new unstandardized testing methods. Besides standardized sine signal DAQ allow to generate signal with ramp and triangle form. The stimulus signal parameters like frequency, amplitude and signal slope could be changed by user. It allows students observe spectrum of the various signals and vice versa to measure distortion of them.

3. CALCULATION OF BASIC TEST CHARACTERISTICS OF ADC UNDER TEST.

The acquired data and recorded in the PC allows to calculate basic ADC characteristics like INL, DNL characteristic and THD, SINAD, ENOB. This parameters are computed according to the IEEE standard test method for Analog to Digital converter [2], [5].

In case of statical method FPGA circuit find for any code $k=(0,1,\dots,2^{N-1})$ two voltage levels V_2, V_1 around $T[k]$ where for each voltage the file of the output data is recorded. The probabilities of the occurrence of k for both voltages shod be higher and lower than 50%. The transition level $T[k]$ is calculated by equation (1)

$$T[k] = \frac{(0.5-p_1[k])}{(p_2[k]-p_1[k])} \cdot (V_2 - V_1) + V_1 \quad (1)$$

Here the $p_1[k]$ is probability of occurrence of code k which is lower than 0.5 and is acquired for the input voltage V_1 . Probability of the k from the second data record $p_2[k]$ is greater than 0.5 and corresponds to the voltage V_2 on the input of ADC DUT.

Integral nonlinearity of the ADC is according to standards [2], [5] defined as

$$INL[k] = \frac{T[k] - T_{id}[k]}{Q} \quad (2)$$

where $T[k]$ is obtained from the FPGA and T_{id} is ideal transition level and Q is kvantisation level. DNL characteristic is then computing as follow

$$DNL[k] = \frac{w[k] - Q}{Q} \quad (3)$$

where $w[k]$ is width of code bin k .

Taken into account terminal definition DNL must be corrected by the mean value.

$$INL[k] = \sum_{i=1}^{N-1} DNL[i] \quad (4)$$

In case of FFT testing method will be computed THD , SNR and $SINAD$ parameters.

$$THD = \frac{\sqrt{\sum_{h=2}^m X_{rms}^2(f_h)}}{X_{rms}(f_1)} \quad (5)$$

where $X_{rms}(f)$ is effective value of harmonic frequency f . Next parameter which user can obtain from the program is $SINAD$

$$SINAD_{dB} = 20 \log \frac{A_{rms}}{eff.value_of_noise} \quad (6)$$

where A_{rms} is amplitude of stimulated sine signal in the spectrum. By equation (6) is computing effective number of bits $ENOB$. This paramater can be computed by next equation from [3]

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (7)$$

4. PROGRAM FOR ADC NONLINEARITY TESTING

The program on the PC server is devoted for the control of the working stand and interfacing blocks. The program was developed in the LabVIEW environment and allows authorised users - students – remote control of the testing procedure. It consists of three subprograms

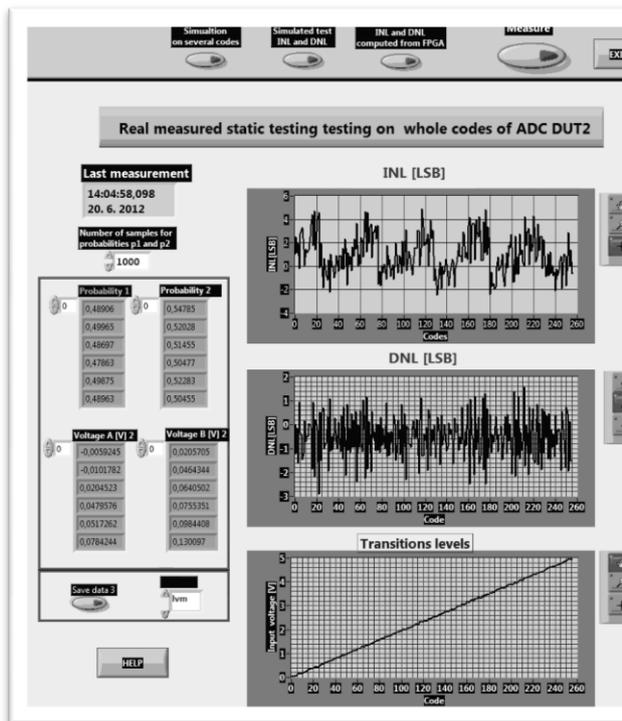
The first program for testing ADC measures the real transition levels acquired from the FPGA circuit. Routine of the static test is executed in FPGA using the on board control program. The procedure of the transfer of the calculated values $T[k]$ to PC will be accomplished when FPGA the static test of ADC is finished. The main advantage of such software management is significant reducing of the testing procedure duration.

Moreover the ADC DUT1 is tested with the maximal conversion rate. Measured transition levels are calculated

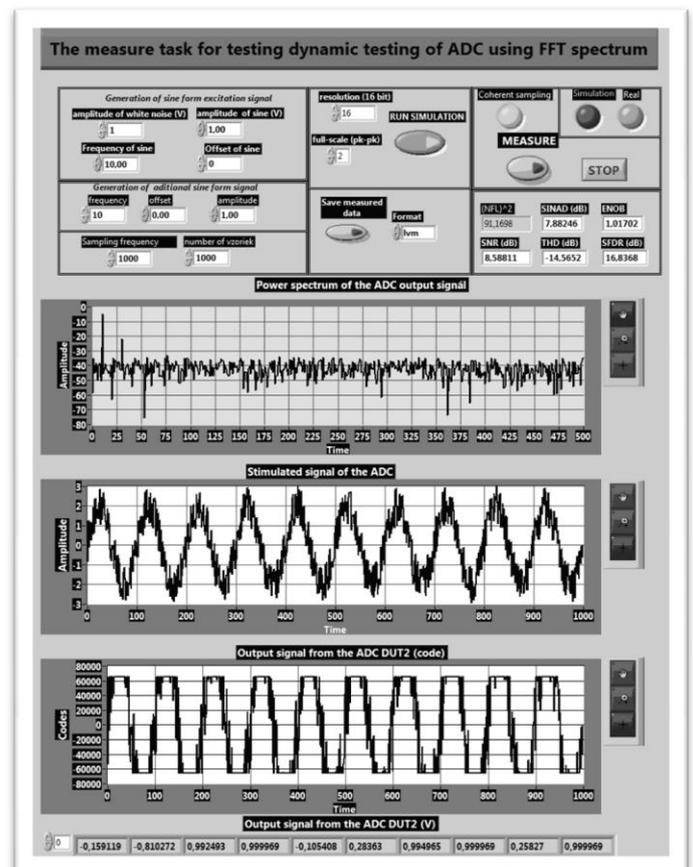
according to the formula (1) and at the end of the testing procedure the acquired transition levels are sent to PC. The PC creates the final transfer characteristic, which is displayed on the front panel of the PC screen. Besides representation of the AD characteristic in the form of the transfer characteristic the program will calculate functional parameters $INL[k]$ and $DNL[k]$ according to the definitions (2),(3) using its terminal definition. ADC nonlinear characteristics from the front panel allow students to compare various form of the functional representation of the ADC behaviors. In parallel to this utility the measured transient code levels are recorded in a file. The displayed functional characteristic on the server the measured functional characteristics together with the recorded file of the code levels are available for students with the authorisation for remote access on their clients' PCs. The students can calculate other ADC error parameters from the recorded file on the base of the definitions from the standards like SNR , etc.

The second subprogram performs dynamic FFT tests of ADC DUT2. It generates harmonic signal in the digital form which is converted in analog signal by the NI PXI 6533 card.. The subprogram acquires the digital data from the ADC DUT2 output. User has the possibility to observe final power spectrum of the tested signal and calculate corresponding integral parameters THD , $SINAD$ and $ENOB$ according to their definitions (5),(6),(7). The subprogram allows to change amplitude and frequency of the tested harmonic signal. It allows students to observe sensitivity of the ADC characteristics on the stimulus signal frequency. The displayed panel on server PC display not only measured integral parameters but as well as the whole power spectrum with the possibility to select the window function. Another utility of the subprogram is FFT test for the modeled ADCs with chosen resolution and programmed nonlinear distortion by the polynomial function. (Fig.2). User can chose between ADC testing based on the real signal records from the output of ADC DUT2 or from data simulated by the modeled ADC with nonlinear distortion. Another utility serves for the data saving and the zooming of plots. Access to the panel for dynamic AD tests with real ADC DUT2 or simulated one is accessible for authorized user via Internet using Remote access of the LabVIEW.

The both subprograms do not allow users to influence obtained data from the tests remotely. They will have possibility just to change number of samples for computing DNL and INL . If user want to measure new nolinear characteristics there will refresh time. User will have the possibility to work with the dynamic test program using ADC simulator in advance off line as for the preparation of test on the remote laboratory stand where the simulator will be a part of the teaching materials. The front panel of the line simulator and front panel of n the distant server will be the same. The simulating utility is additional possibility implemented on the server PC controlling the working stand.



a) Front panel in LabVIEW for the static testing of a simulation static test of ADC



b) Front panel in LabVIEW for dynamic testing of ADC

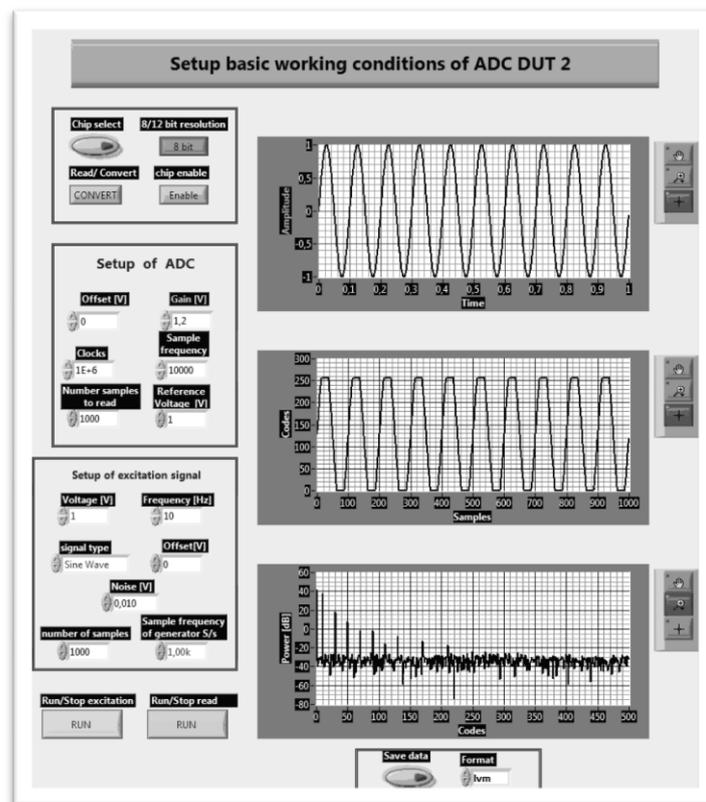


Fig.2 Front panel in LabVIEW for the setting of ADC working conditions

The third subprogram allows to change the working modalities of the ADC DUT2. Successively, there is possibility to measure the corresponding error characteristic by the dynamic testing method. Subprogram gives possibility distant users to change working nodes of the ADC DUT2 (voltage range, unipolarity or bipolarity etc.) without acknowledge of corresponding pins even with changes of the clock and sampling frequencies. The set of adjusted parameters together with their default values utilized in the basic test in the second subprogram will be on the disposal for the users. Their basic description what will be a part of this control program.

In addition the user will have access to the program generating stimulus signal. Subprogram allows remote/local users to change superimposed signal noise or to add real distortion to the tested harmonic signal. The dynamic tests will be accomplished by the second subprogram. The FFT plots and resulting testing parameters together with adjusted control parameters will be available for remote/local user on the common panel for the dynamic ADC tests. In addition the recorded data will be available and downloadable for remote user. It will offer possibility to test other ADC parameters not foreseen in the testing programs.

Recorded data of the static test and recorded digital output signal from the dynamic tests are available for download in the form of xls data for successive elaboration in Microsoft Excel environment.

5. ACCESS TO THE WORKPLACE

Access to the workplace is created in the programming environment LabVIEW. Working stand will be one of testing stands dedicated for laboratory exercises in the course of electronics. Other laboratory stands which can be controlled remotely are: The stands for testing of operational amplifiers, differential amplifiers etc. All mentioned laboratory stands have been already developed. Remote control of those laboratory stands were developed in LabVIEW and is available through any web browser using remote panel utility from LabVIEW.

In LabVIEW is used web publishing tool. The tool create html web page with control panel of program. Every program is converted to html page. Running of programs is executed by program which uses function semaphores.

The semaphore is a way to limit the number of task that can simultaneously, it is similar to a multiplex of running of programs. Every program take a several part of run time. The input parameters and output results are available for the user. The proposed solution gives better exploitation of PC. Next figure shows the structure of the program using semaphore. Each icon represent one subprogram. Every program is running necessary time for test DUT and process data. User see control panel where data refresh only when semaphore run concrete program.

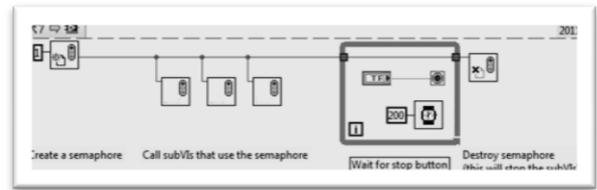


Fig. 3 Program for control of whole work stand

User has to install LabVIEW Plug-ins to Microsoft explorer only, which are available on web page of laboratory stand. The Microsoft explorer is preferable web browser for stabile remote control of the prepared laboratory stands.

5. CONCLUSIONS

Presented laboratory stand gives to user practical skills about working of AD converter. AD converter is available for performing basic ADC remote tests. Working stand will be used in the laboratory training in the course of Nonlinear electronics, Instrumentation at the Faculty of Electrotechnics and Informatics. Access to the described Laboratory Workplace is open permanently authorized users. Authorization of users is the first step based on the approval; of the responsible teacher of the courses..

The system allows monitoring activity of students enrolled in the course. Results of monitoring and answer on short questioner give possibility teacher to evaluate students attending virtual laboratory.

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