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ACQUISITION OF DATA FROM ADC USING FPGA

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Abstract: The paper presents the implementation of analog data acquisition system, in particular controlling with a 6-channel ADC converter AD7656 via the FPGA Xilinx Spartan 3 series. The procedures for data sending from the ADC to the FPGA buffers, their conversion and subsequent transmission to TigerSHARC DSP are described. The digital representations of ADC analog input signals are sent to the FPGA through three lines of serial interface at the physical layer compatible with standard SPI. After processing in the FPGA they are sent to the DSP, with the participation of the lines in standard LVDS. The paper discusses the properties of related interfaces, standards, procedures and control of ADC issues as well as algorithms of FPGA configuration program and functions implemented in this system. Selected results of functional testing are shown.

Keywords: ADC control, ADC output data handling, interface, electrical power quality.

1. INTRODUCTION

On-line analysis of power quality in electrical power system is associated with the need for fast acquisition and processing of data collected from the tested system. The power quality analyzers offered for this purpose enable the determination of multiple parameters. Unfortunately, usually it is not specified, according to which algorithms they are operating and what standards are the basis for their calculation. For example, we have indicated a few different definitions of THD coefficient, concerning estimation of waveform distortions [1], a few definitions of voltage unbalance or some approaches related to power theories.

In addition, the results of measurement obtained with various kinds of analyzers in some cases seem to be differing substantially.

The Department of Marine Electrical Power Engineering of Gdynia Maritime University undertook a research project to develop an estimator/analyzer of power quality in which the relevant parameters are determined in accordance with the standards [2], [3], [4], [5] and [6].

Measurement tracks (Fig.1) of signals from the power system contain typical input circuits including complex of voltage dividers, galvanic separation systems and anti-aliasing filters. The voltage signals are fed to the inputs of ADC's (analog-to-digital converter) AD 7656 (Analog Devices).

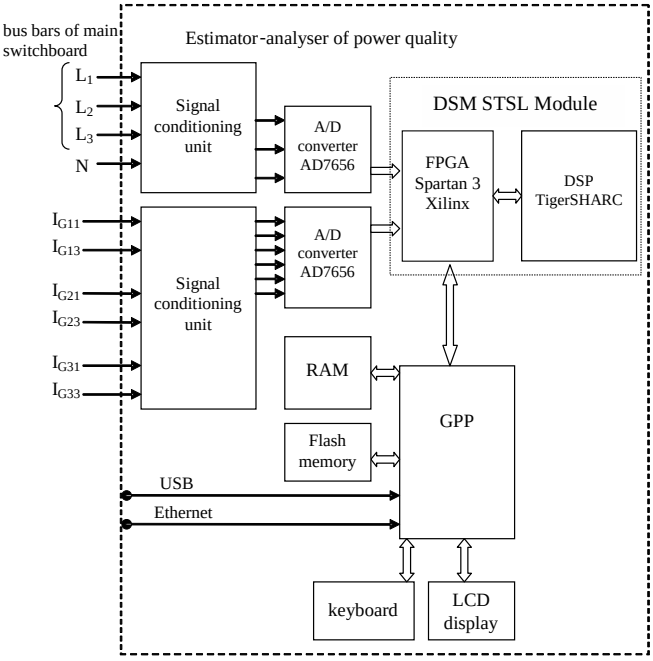

Fig.1. Estimator/analyzer configuration.

Operation of determining the value of individual parameters to assess the electrical power quality takes place in the DSP (Digital Signal Processing) processor ADSP TS-201 TigerSHARC (Analog Devices).

The DSP processor communicates with external systems via a custom protocol Link Port in which data are exchanged in 128-bit frames, using the LVDS interface. It has no native support for SPI protocol. On the second hand, the AD7656 chip has a high speed parallel and serial interfaces, allowing the devices to interface with microprocessors or DSPs, but not with ADSP TS-201.

Due to the lack of compatibility between ADC output interfaces and DSP communication port, i.e. Link Port, the FPGA Spartan 3 (Xilinx) was used as an intermediate device. Besides providing communication between ADC and DSP system the FPGA device also mediates the exchange of information with the GPP (General Purpose Processor) LPC3250 microcontroller (ARM926EJ-S core), which implements the user interface features, such as support for the keyboard, graphic display, exchange of data on USB and Ethernet ports.

2. ADC AND DSP COMMUNICATION FEATURES

The AD7656 contains six 16-bit, low power, fast, successive approximation ADCs, all in the one package [7].

The AD7656 feature throughput rates up to 250 kS/s. Its inputs contain low noise, wide bandwidth, track-and-hold amplifiers that can handle input frequencies up to 12 MHz. The AD7656 can accommodate true bipolar input signals in the ±4×VREF range and ±2×VREF range. The AD7656 also contains an on-chip 2.5 V reference (Fig. 2).

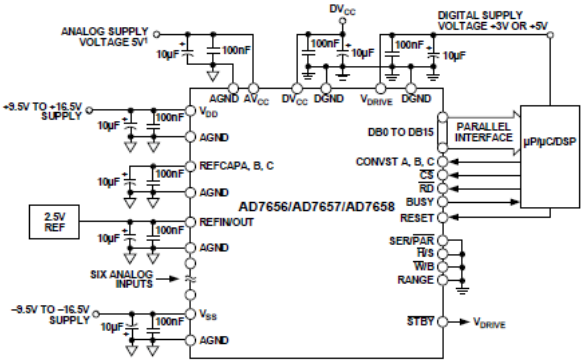

Fig. 2. The configuration of AD7656 device [7].

The conversion process and data acquisition are controlled using CONVST signals (Fig. 3) and an internal oscillator. Three CONVST lines allow independent, simultaneous sampling of the three ADC pairs (channels 1-2, 3-4 and 5-6). The rising edge of CONVST initiates simultaneous conversions on the selected ADCs. The conversion time is 3µs. The BUSY signal on the ADC output goes low to indicate the end of the conversion. The conversion results from the simultaneously sampled ADCs are stored in the output data registers.

Although the parallel interface t_{ACQ} acquisition time (Fig. 3), i.e. time required to output all six 16-bits words (from V1 to V6) from ADC registers, is only about 700ns, because of the complicity of ADC output connection lines, there was decided to use serial interface. Then only three interface lines are required instead of 16 printed paths.

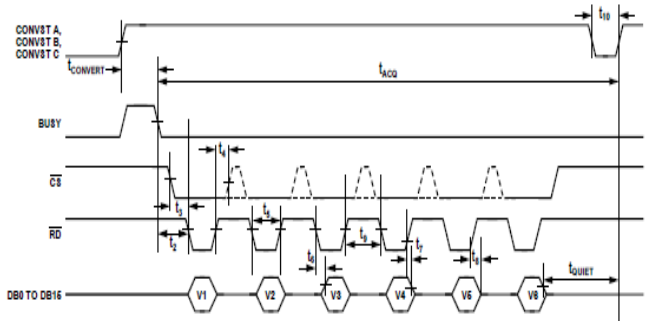

Fig. 3. The ADC registers data output procedures through parallel interface [7].

The three-line serial interface applied in AD 7656 chip is compatible with standard one-line SPI serial interface. It is fully reversible [7,8]. One of the devices connected by interface fulfills functions of the Master, issues a clock signal SCK and manages the lines Slave Select (SS_N) serving to activate one of the other devices (slave). The SPI consists of signal lines: Serial Clock (SCK), Master Out Slave In (MOSI), Master In Slave Out (MISO) and the Slave Select line (SS_N). The data in both directions are transmitted in 8-bit frame, from MSB to LSB. Data transfer is synchronized to rising or falling edge clock (depending on configuration), and their set-up on the slope opposite to the sending data. The SCK frequency used to control of data transfer can reach a few MHz, depending on given application. Figure 4 shows the signals in the SPI lines.

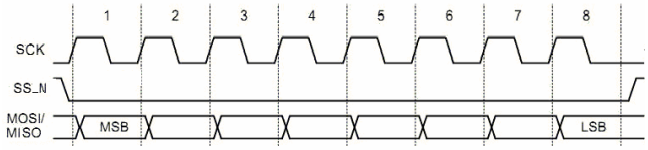

Fig. 4. The waveforms in the SPI interface lines.

In serial interface mode of AD7656 three DOUT pins (Fig. 5), DOUT A, DOUT B, and DOUT C are available. Data can be read out from ADC using one, two, or all three DOUT lines. Figure 5 shows six simultaneous conversions and the read sequence using three DOUT lines. Also in Figure 5, 32 SCLK transfers are used to access data from the AD7656, however, two 16 SCLK individually framed transfers with the signal can also be used to access the data on the three DOUT lines.

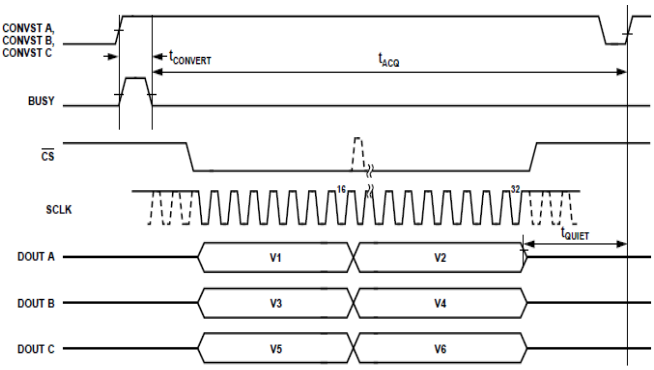

Fig. 5. The signals in AD7656 serial interface lines [7].

TigerSHARC [9,10] is a 128-bit processor, designed to perform operations on floating-point and fixed-point numbers, bears the double sets of ALU units for both types of operation, the internal memory of 24Mb DRAM, integrated circuits I/O, 14 channels of DMA, 4 internal bus for fast exchange of data between memory and the peripheral circuits and other CPU. The TigerSHARC processor has four Link Port circuits full-duplex type that can operate in parallel. These ports use in physical layer the interface LVDS (Low Voltage Differential Signal) [11], in which the information (in 128-bit frames) is sent using low voltage differential signal in the symmetrical copper cables in the system loop. The LVDS protocol enables data transmission speeds of up to 4 Gb/s with very low power consumption. Link port can be configured to exchange data on one or four interface lines. Figure 6 shows the signals on lines of LVDS interface.

As it is described above, both interface standards differ significantly and the only way to provide data exchange between ADC and DSP is to apply an intermediate device.

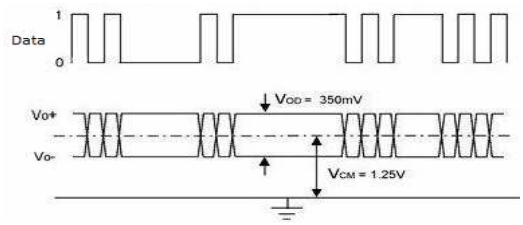

Fig. 6. The signals in LVDS interface lines [11].

3. FPGA FEATURES AND CONFIGURATION PROGRAM ALGORITHMS

In considered system, to provide the acquisition in TigerSHARC of data obtained from AD7656 the FPGA (Field Programmable Gate Array) XCS1000 Xilinx Spartan 3 [12,13] was used. In Figure 7, the FPGA circuit to the ADC and DSP devices interface connections are shown. Attached digits indicate the number of lines in respective bus.

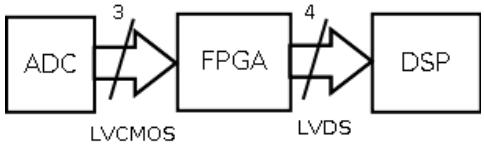

Fig.7. ADC and DSP interface buses in the measurement track.

The FPGA is a large-scale integration system, used to create high-speed digital circuits for specialized logic functions. The power consumption of these systems is much smaller than for standard digital systems and processors. For these systems, as well as for processors, the change of implemented feature requires software changes to the FPGA. Capacity of these systems reach to 8 million gates, with up to 500 inputs/outputs and a single cell propagation time of less than 1ns. FPGAs have a regular structure based on the same or very similar CLB teams. XC3S1000 device contains one million gates, 17 280 logic cells (CLB), 24 hardware multipliers, 432kb Block RAM memory, 120kb of Distributed RAM memory, 4 DCM clock waveform synthesizers, up to 175 differential I/O lines and 391 asymmetric line in I/O blocks (IOB). The CLB blocks are the basic built-in logic elements, which may perform additional tasks, such as function of shift registers. Each block CLB consists of four Slice elements. These elements provide communication throughout the entire FPGA and can meet different logic functions. Each Slice element has configurable input and output. It can be programmed to any logical function for the four input variables. The structures located inside Slice element, called Logic Function Generator, are the main resource for implementing logic functions (Look-Up Table programming techniques). Through their combination e.g. the shift register or part of the distributed memory (Distributed RAM) can be configured. Each CLB can implement ROM (capacity 128x1b), SRAM (capacity 64x1b or 2x32x1b or 4x16x1b). I/O blocks allow the two-way exchange of data through I/O pins and cells of the CLB. The Spartan 3 I/O are designed to work with different voltage standards thanks to software configuration and have the analog voltage comparators, which can act as differential input/output (balanced). Each I/O block also has a pull-ups and pull-down resistors, which can be freely activated. These resistors allow the use of different signal standards, such as LVDCI_15, LVDCI_25, GTP_DCI, HSTL_I_DCI, LVDS_25_DCI or SSTL18_I_DCI [13].

In general, the configuration program organizes the connections network among selected circuits of FPGA and then the device works autonomously as every hardware device. In considered project the basic task fulfilled by the FPGA is the conversion between differing in physical layer standards of ADC and TigerSHARC interfaces as well as different formats of frames transmitted by both links.

For handling of ADC SPI interface, the respective FPGA lines were configured as LVCMOS25 and for TigerSHARC as LVDS_25 (Fig.7). The output data from ADC are available at one time on three lines DOUT A, B, C (Fig.5, Fig.8). On the 1st line the ADC conversion results are transmitted in sequence from input channels 1 and 2, on the 2nd line - from channels 3 and 4 and on 3rd line - data from channels 5 and 6. The transfer of all data requires 32 SPI SCK cycles, but in case the only three channels are needed and when the input signals are connected to the channel inputs 1, 3 and 5 - to transfer such data the only 16 SPI SCK cycles are necessary. When the SPI SCK frequency is equal to 16MHz the transfer of three 16-bit words from ADC takes approximately 943 ns. The A/D conversion takes about 3 μs, so full ADC conversion cycle with output of digital data requires in considered situation about 3,95 μs, it means the maximal frequency of A/D operations is above 253 kS/s (Fig.8). Such result is possible because other operations performed in FPGA, connected with data transmission to TigerSHARC, are implemented parallel in time with A/D conversion. The data from three FPGA buffers BUF have to be overwritten to eight RAM blocks (it takes about 480ns), because of configuration of four-line LVDS interface connecting FPGA with TigerSHARC Link Port. The transmission through Link Port requires approximately 160ns.

The time-dependencies shown in Figure 8 illustrate the location of individual operations made during the A/D conversion cycle. More explanations to the procedures realized in FPGA are presented in algorithm in Figure 9. The conversion cycle begins every 4μs with CONVST going high, generating in FPGA. After the digital data in cycle n of conversion are completed and ADC line BUSY goes low, FPGA clock SPI SCK starts pulling data V1, V3 and V5 (16-bit words) from DOUT registers (in ADC) to BUF buffers (in FPGA). After 16 cycles SPI SCK clock stops and data are shifted from three BUF to eight RAM. Then the state of output line ACK from TigerSHARC is examined. If it is high, FPGA issues 100MHz clock managing data transfer from FPGA RAM to TigerSHARC on four differential lines of LVDS interface.

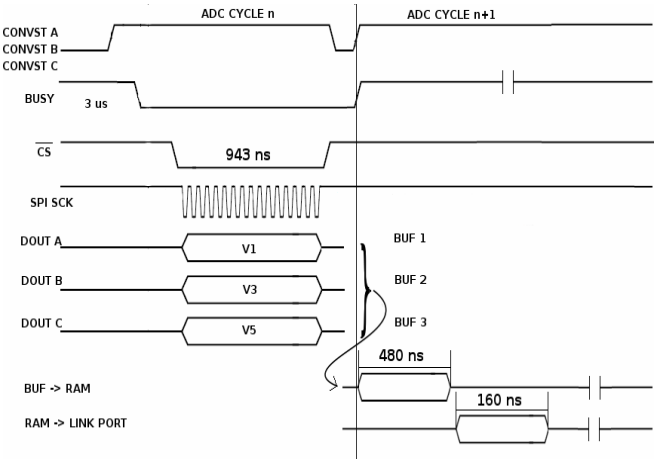

Fig. 8. ADC data handling during A/D conversion.

The operations performed in FPGA during A/D conversion (BUSY=1) take time less then 1μs. They are performed in parallel with another A/D operations in next A/D cycle, otherwise it would be not possible to obtain the assumed frequency of the A/D conversion.

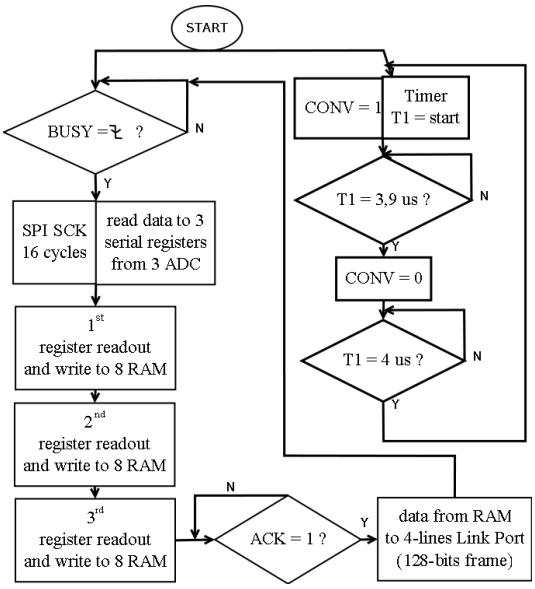

Fig. 9. Algorithms performed in FPGA.

4. FINAL REMARKS

The developed estimator/analyzer of electric power quality gives some options of the device operation for choice by the user. These options concern a kind of analysis (voltage monitoring or monitoring of powers/currents distribution), mode of operation (estimator/analyzer), and also a kind of power system and number of generators working in parallel. The designed implementation of measurement channel in Estimator mode allows to acquire the data from three ADC's at 250kS/s from each, as was assumed at the start of project. However, in practical realization, because of TigerSHARC program, the value of ADC conversion frequency equal to 210kS/s was set. Now, the program is under optimization procedure to obtain the instrument assumed operation frequency.

For the functional tests of measurement channel, the three phase power signal generator Chroma Programmable AC Source Model 6590 was used. The performed tests among the others consisted of generating of signals with known harmonic content in three voltage signals. This allows the evaluation of correctness of calculations THD coefficient processed in TigerSHARC DSP. The reference and calculated coefficients (expressed in %) differed in third decimal place.

Described above algorithms concerns the Estimator mode for voltage monitoring. The second mode of instrument operation is Analyzer of currents and power. Then the A/D conversions are performed in different conditions, the required A/D frequency is 25kS/s only, so all processed connected with ADC data handling, performed in FPGA, are not critical as in Estimator mode.

Another tests were connected with maximal SPI SCK frequency. In technical data of AD 7656 it is given as 18MHz [7]. After numerous experiments the SPI SCK frequency equal to 16MHz was set.

In designed instrument the configured FPGA fulfills many functions, sometimes critical for all instrument functioning. The implementation of these functions with standard digital circuits entail a much greater demand for power supply. The data conversion and communication tasks performed in FPGA are crucial to the operation of the entire device.

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