XVIII IMEKO WORLD CONGRESS
Metrology for a Sustainable Development
September, 17 – 22, 2006, Rio de Janeiro, Brazil

FULL FLASH LOGARITHMIC ADC ARCHITECTURE

Roberto Lojacono[1], Arianna Mencattini[1], Marcello Salmeri[1], Silvia Sangiovanni[2]

[1] Department of Electronic Engineering, University of Rome "Tor Vergata"
Viale del Politecnico, 1 – 00133 - Roma, Italy
Ph.+39-06 7259-7494
[2] Department of Electrical Engineering,University of Rome "La Sapienza"
Via Eudossiana, 18 - 00184 Roma, Italy
Ph+39-06 44585 509
e-mail [lojacono, mencattini, salmeri]@ing.uniroma2.it; silvia.sangiovanni@uniroma1.it

Abstract: The advantages of a signal processing in the logarithmic domain are recently pointed out by some authors [1,2]. On the other hand, suitable logarithmic input amplifiers are available in the literature. The traditional logarithmic amplifier configuration based on a voltage operational amplifier with a diode connected transistor in its feedback loop, which displays a significantly reduced bandwidth at lower signal levels, was modified replacing the operational amplifier by a transconductance feedback amplifier. This solution overcomes the said problem completely and offers constant-bandwidth operation throughout the full signal range [3]. Some authors have proposed algorithmic architectures for the hardware realization of logarithmic Analogue to Digital Converters (ADC) [4,5]. This paper presents a fully analogue architecture of logarithmic ADC. The proposed architecture represents a logarithmic version of the calliper rule based linear ADC recently proposed [6,7]. The main feature of this architecture is the small number of reference resistors needed, namely $3*2^{n/2}$ instead of 2^n, being n the number of bits of the binary converted sample.

Keywords: logarithmic ADC, subranging ADC, calliper rule.

1. INTRODUCTION

Logarithmic procedures are widely used in communications, instrumentation and hearing aids, among other application areas, where it is needed to increase the dynamics of the input signals [1,2]. The input logarithmic conversion was recently improved since the classical input analogue logarithmic amplifier has been replaced by a transconductance feedback amplifier. This solution overcomes the said problem completely and offers constant-bandwidth operation throughout the full signal range [3]. Also in the measurement field, when the detection and measure regard low amplitude signals and the signal to noise ratio must be optimised, this kind of procedure becomes very useful [8]. These logarithmic procedures is until now mainly used in the analogue domain and the logarithmic A/D conversion was introduced firstly in the communication field. However, recent improvements in the logarithmic A/D conversion [9] allow the possibility of the use of these converters also in the field of digital measurements, especially for the spectrum analysers. These instruments traditionally give the values of the measurements in logarithmic domain giving the logarithmic ratio to the reference level in Neper or dB . Also the problem connected with the alias has been satisfactory resolved. Some authors have proposed algorithmic architectures for the hardware realization of logarithmic Analogue to Digital Converters (ADC) [4,5]. The present paper proposes a new kind of A/D full flash or subranging logarithmic converters. These converters, implemented by a fully analogue hardware, are based on the calliper rule. This fact allows the use of a small number of reference resistors, namely $3*2^{n/2}$ instead of 2^n, being n the number of bits of the binary converted samples.

2. MODIFIED THEORY

Following the theory already presented [6], which was explained by using a length measurement example, we apply directly the modifications involved in this new proposal.
We consider a set of N exponential scales which have the marks, represented by the x coordinate along the scale axis, given by this formula:

$$x_{k,u_i} = (u_i)^k \qquad ;k = 1,2,.....; \quad i = 1,...,N \tag{1}$$

Now an application of the logarithm in both the sides gives:

$$\ln\left(x_{k,u_i}\right) = k \cdot \ln\left(u_i\right) \tag{2}$$

In this way all the given scales become linear having the steps equal to $\ln(u_i)$. Due to the presence of the ln function, all these steps are prime each other. We can suppose that, in the general case, a set of values of the exponents k, namely $\{\tilde{n}_i\}$ exists so that

$$\tilde{n}_i \cdot \ln\left(u_i\right) \equiv \tilde{n}_j \cdot \ln\left(u_j\right) \quad for\ all\ i, j = 1,...,N \tag{4}$$

Where the symbol "≡" means "corresponds in terms of our accuracy" and will be replaced in the following by a simple "=". Now:

$$\tilde{n}_i \cdot \ln\left(u_i\right) = M \quad , \ i = 1,2,...,N \tag{5}$$

Recalling that the $\ln(u_i)$ are mutually prime, condition (5) is verified when

$$\tilde{n}_i \ln(u_i) = \prod_j^N \ln(u_j) = M \quad , \; i = 1,2,...,N \tag{6}$$

So we have that the following quantity:

$$\frac{n_i \cdot \ln(u)_i}{\prod_j^N \ln(u_j)} = 1 \quad , \quad i = 1,2,...,N \tag{7}$$

can be assumed as the "Basic Unity" (BU) of this measurement system. However, this is a "virtual unity", very small with respect to the u_i, which not exists physically. Nevertheless, as happens in the caliper, the measurements can be performed with an accuracy related to this unity. This simply considering the $\tilde{n}_i$, given by direct observation, and some of their differences. From (4) it follows that:

$$\tilde{n}_i = \prod_{j \neq i}^N \ln(u_j) \tag{8}$$

Expression (8) means that also the $\ln(u_i)$ must be integer (in terms of BU), as can be easily proved. Indeed the $\tilde{n}_i$ are integer, so that the sentence is surely valid for $N = 2$. An induction procedure over N shows that if we have a system of order N and the related u_i, $i = 1,2,...,N$ that are integer, also a further $(N+1)^{th}$ length, inserted in the preceding system to obtain a system of order $N+1$, must be integer.
Now:

$$\prod_{i=1}^N \tilde{n}_i = \prod_{i=1}^N \prod_{j \neq i}^N \ln(u_j) = \left(\prod_{j=1}^N \ln(u_j) \right)^{N-1} \tag{9}$$

in such a way that:

$$\prod_j^N \ln(u_j) = M = \sqrt[N-1]{\prod_i^N \tilde{n}_i} \tag{10}$$

and finally, from (2), the unknown values of the lengths $\ln(u_i)$ can be determined in terms of BU as:

$$\ln(u_i) = \frac{M}{\tilde{n}_i} \; , \; i = 1,...,N \tag{11}$$

The caliper rule, logarithmic caliper rule in this case, can be regarded as a particular case of this theory [6,7].

3. THE LOGARITHMIC CALIPER RULE

The caliper rule can be considered a particular case of this theory. We can create a logarithmic version of this rule by considering two scales, fix and mobile, having steps: $\ln\left\{\frac{L}{n}\right\}$ (fix scale) and $\ln\left\{\frac{L}{n+1}\right\}$ (mobile scale) respectively. This structure can be used in determining the logarithm of a quantity X. To this purpose, the mobile scale is shifted of a quantity X, in respect to the fix one, and the first alignment of the markers of the two scales is observed, in such a way that:

$$\log X = k_2 \cdot \ln\left\{\frac{L}{n}\right\} - k_1 \cdot \ln\left\{\frac{L}{n+1}\right\} =$$

$$= k_2 \cdot \ln\left\{\frac{L}{n}\right\} - k_1 \cdot \ln\left\{\frac{L}{n\left(1+\frac{1}{n}\right)}\right\} = \tag{12}$$

$$= (k_2 - k_1) \cdot \ln\left\{\frac{L}{n}\right\} + k_1 \ln\left\{1+\frac{1}{n}\right\}$$

Where k_1 and k_2 represent the number of steps of the two scales (mobile and fix respectively) from the origin to the said first alignment. In the last member of (12), the difference $(k_2 - k_1)$ represent the characteristic c_a and the second term represent the mantissa m_a of the logarithm of X. This separation will be very useful in simplifying the output circuitry of the ADC, as will be shown in section 4.

4. APPLICATION OF THIS THEORY TO THE ADC'S

a) – Linear case

As already presented in a previous paper (6) for the linear case, an electrical version of the caliper rule can be realized by using two voltage scales provided with two resistive voltage dividers. An explanatory scheme of this said circuit is shown in figure 1.

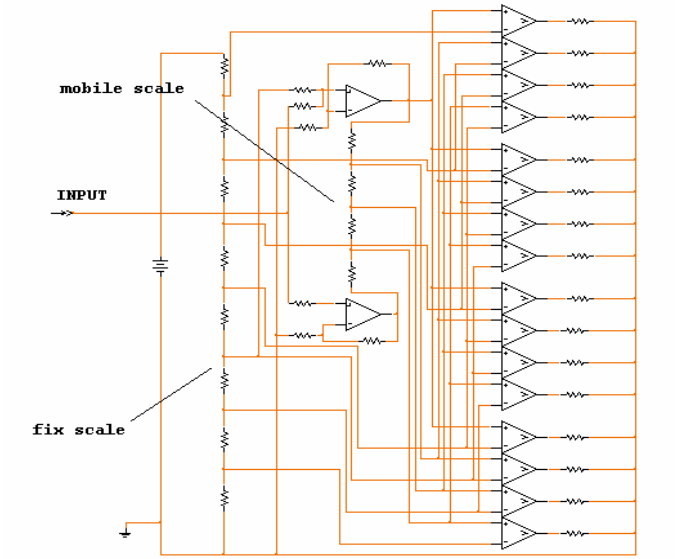


Fig. 1. Scheme of the voltage version of the caliper: the input comes from the hold capacitor and drives the mobile scale by the OP-Amp couple; the coincidence of the markers is detected by using some comparators, as happens in the full-flash ADC.

Note that the fix scale is doubled (8 resistors) in respect to the mobile one (4 resistors) in order to obtain all the possible comparison of the markers. Also the driving voltage of this last scale is doubled. The upper Op-Amp of the couple which drives the mobile scale operates a sum of the input voltage and ¾ of the voltage across 4 resistors of the fix scale. Since the mobile scale contains four resistors, the

same voltage is divided by 3 (i.e. "n") in the fix scale and by 4 (i.e. n+1) in the mobile scale. Thus the caliper rule is realized in this linear case.
We operate the driving of the mobile scale as in figure 4. Here the mobile scale is directly driven by the sample-hold input circuitry. This means that the hold circuit becomes a multi-hold circuit.

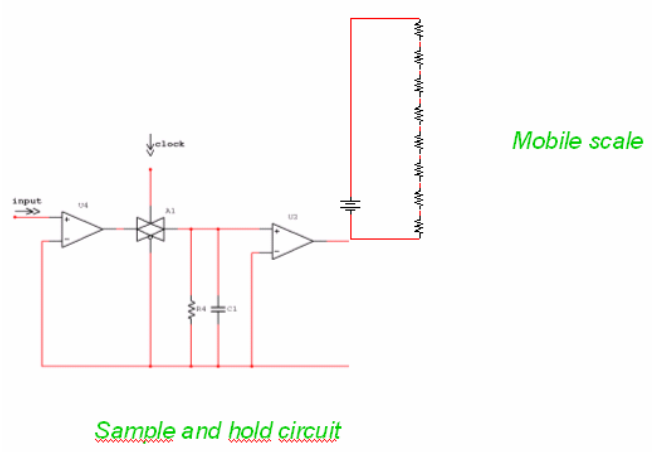


Fig. 2. Driving of the mobile scale by the last op-amp of the sample-hold citcuit.

The effect of the integration of the mobile scale in the track and hold circuit is that the held signal is split in several levels by the "mobile" scale. These levels are compared with the levels of the "fix" scale by the comparators which realize the thermometric scale. When two levels of the two scales coincide, a comparator changes state. A rule of thumb to determine the number of resistors required in realizing an n-bit word length by this architecture is:

$$N = 3 \cdot 2^{n/2}. \qquad (2)$$

This means that for a full flash ADC with 10-bit word length minus than hundred resistors are required (instead of the 1024 of the traditional full-flash architecture). However, to obtain the thermometric scale to be converted in binary, 1024 comparators are requested. A 16-bit full flash structure requires about 768 resistors only (instead of the 65536 of the traditional full-flash architecture) but, again, 65536 comparators. The logarithmic version of the proposed ADC here presented drastically reduces also these numbers.

b) – Logarithmic case

Our present converter is logarithmic. The hardware implementation of this kind of converter requires the realization of the two voltage scales having the steps used in developing the above formula (12) . By indicating with V_0 the ratio $\frac{L}{n}$ of and with V_{fix} and with V_{mob} the driving voltages of the fix scale and the mobile scale, respectively, we have that:

$$V_{fix} = n \cdot \log\left\{\frac{L}{n}\right\} = \log\left\{V_0^{\,n}\right\} \qquad (15)$$

and

$$V_{mob} = n \cdot \log\left\{\frac{L}{n+1}\right\} = n \cdot \log\left\{\frac{L}{n\left(1+\frac{1}{n}\right)}\right\} = \qquad (16)$$

$$= \log\left\{V_0^{\,n} \cdot \frac{1}{\left(1+\frac{1}{n}\right)^n}\right\} \cong \log\left\{V_0^{\,n} \cdot \frac{1}{e}\right\}$$

The supply voltage of the fix scale must be doubled, as in the linear case. So that, assuming as logarithmic transducer the scheme of figure 5, the supply circuit of the two scales becomes as in figure 6.

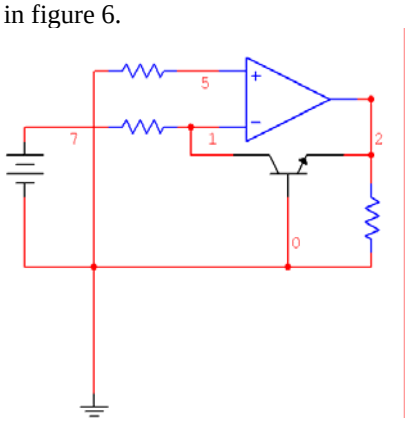
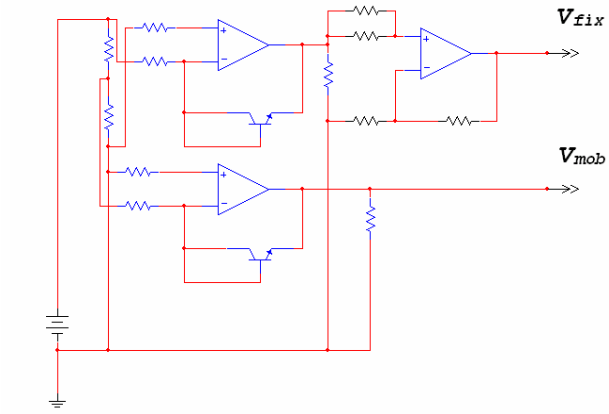


Fig. 3 – Scheme of the logarithmic transducer.



F

Fig. 4 – Supply circuit of the two scales: the voltage V_{fix} drives the fix scale and the voltage V_{mob} drives the mobile scale.

Applying the caliper rule we can realize some schemes of principle of logarithmic ADC architectures. An example, directly derived from the linear architecture above recalled, is given in figure 7.
A SPICE simulation of this converter, when the input signal is a pure sinusoid, is shown in figure 8.
However, following formula (12), we can realize architectures which reduce also the number of required comparators. Here the main problem is to obtain a convenient accuracy. A scheme of principle of a converter which gives the characteristic and the mantissa of the

logarithm of the input is shown in figure 9. The main characteristic of this architecture is that we have two mobile scale and one fix scale. The comparison of the first mobile scale and the fix scale gives the characteristic. This operation is very similar to the "folding". However, in our case this "folding" is carried out on the reference voltage instead of the input signal. The comparison between the two mobile scale gives the mantissa. Here three comparators give a thermometric scale of the characteristic and sixteen comparators give thermometric scale of the mantissa. In this case, by further converting the output of the comparators present in the scheme in binary, two bits of characteristic and four bits of mantissa can be obtained for the logarithmic binary output. A traditional full flash which gives the same number of bits requires 48 comparators. The operating mode of this architecture is similar to the "subranging" but also in respect to this last architecture we have a reduced number of resistors, switches and comparators.

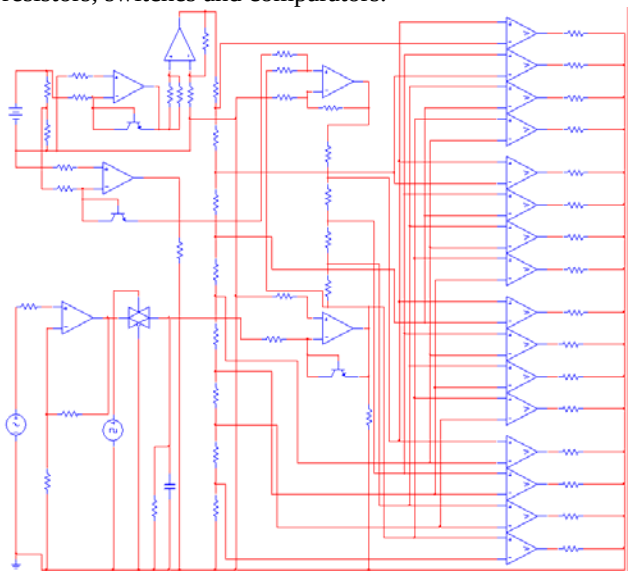


Fig. 5. A direct implementation of the logarithmic caliper ADC.

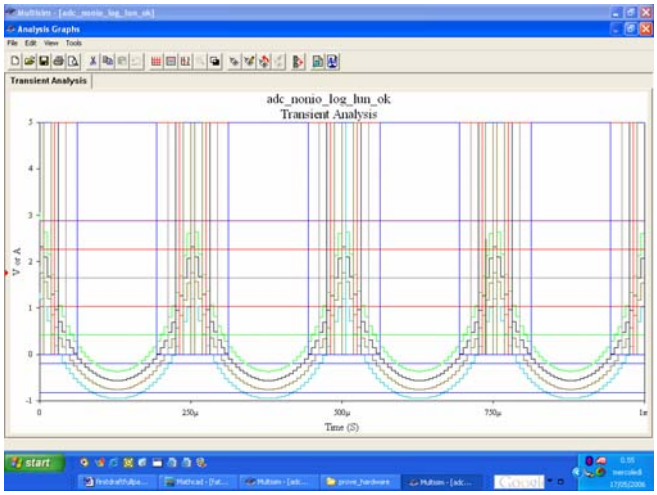


Fig. 6. Spice simulation of the logarithmic converter of figure 5: the horizontal lines represent the voltage levels of the fix scale; the sinusoidal input signal is firstly converted in logarithmic form and then split in some levels by the mobile scale; the vertical lines correspond to the change of state of the comparators.

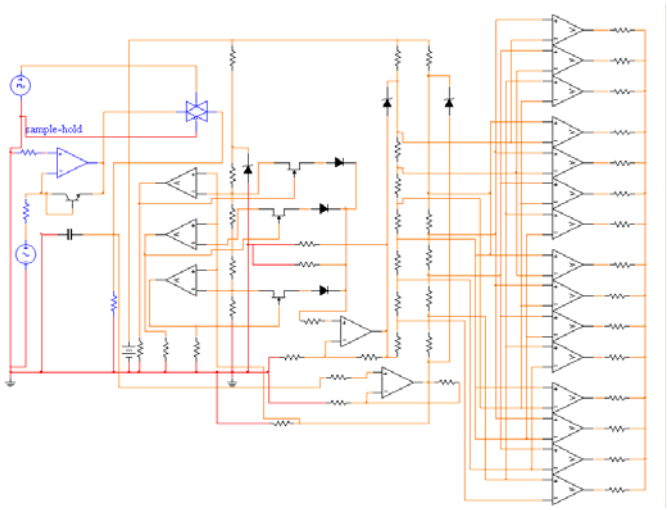


Fig. 7 - An example of simple scheme derived from the proposed theory. Three comparators (left side of the scheme) give the characteristic of the logarithmic output; sixteen comparators (right side) give the mantissa.

5. EVALUATION OF THE PERFORMANCE OF THE PROPOSED ARCHITECTURE

Planar resistor, as realized in the IC's technology is simply depicted in fig.1,

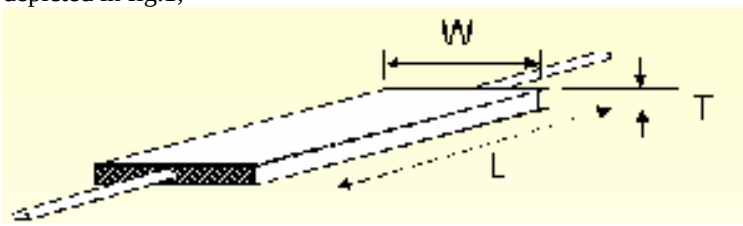


Fig. 8 – Simple realization of a planar resistor.

The resistance of this kind of planar resistor, often realized as a polysilicon thin film, is given by

$$R = \rho \cdot \frac{L}{T \cdot W} \cdot \qquad (17)$$

As said above, to realize a resistive n-bit converter, a string of 2^n well matched resistors must be available. The matching behaviour of those resistors, which we think here as arranged in a linear array, is influenced by several important parameters. These parameters are the spread in sheet resistance, lithography and etching errors, contact resistance, and alignment errors. Lithography and etching errors lead to statistical and deterministic deviations of resistor ratios from the desired value. The precision of converters based on the string principle is independent of the resistance value. The absolute value of the single resistor can fluctuate in a range of about 30% from one wafer to another. Statistical deviations from this value are large for small structures and become smaller if structure size increases. Increasing the resistor size, which reduces the mismatch due to the above cited causes, must be carried out with care because of the increasing influence of deterministic deviations for larger structures. Thus, gradient errors with respect to the resistor core depend on height, orientation, and slope of the spread in sheet resistance.

More recent technologies, used for “system on chip” (SoC) realizations, employ n-well resistors. The sheet resistance accuracy of n-well resistors is similar to that of the polysilicon resistor. However, the sheet resistance of the n-well is much larger than that of polysilicon. This makes the n-well resistor attractive for circuits which require large resistances. Also in this case, the gradient errors said above occur. Here we simply consider first order gradient errors in a linear array of resistors.
If we consider a first order gradient in the realization of the linear array of resistors, the voltage reference scale appears to be as:

$$v(k) = \frac{k \cdot R + \sum_{j=1}^{k} \varepsilon(k)}{2^n \cdot R + \sum_{j=1}^{2^n} \varepsilon(k)} \cdot V_{bias} \qquad (18)$$

where R is the nominal resistance of the single element of the cascade and $\varepsilon(k)$ is the gradient of the realization process which we can simply represent as (4):

$$\varepsilon(k) = \frac{\alpha \cdot k \cdot R}{2^n} \qquad (19)$$

In this way, the last resistor of the chain is altered by a factor α. These expressions are used in calculating the effective bits of an ideal ADC, a “classical” ADC and the proposed one respectively.
The used formula is :

$$enob = \frac{20 \cdot \log\left\{\frac{V}{\sqrt{2} \cdot rms[error]}\right\} - 1.76}{6.02} \qquad (20)$$

where V is the maximum value of the input signal. This input signal is shown in figure 10 and has constant “probability density function” (PDF). This choice is coherent with the statistic commonly used in evaluating the quantization error in the ideal case. This choice also avoids the dependence of the calculated effective bits on the amplitude and frequency which occur applying an input sine wave, due to the particular form of the PDF of this last signal [9]. The figure 9 shows the deviation from an ideal linear voltage reference scale induced by the first order gradient effects modelled in (18) and (19).
For the new architecture under investigation, the same expression (19) of the gradient and of the resistor array shape (linear) is assumed. Clearly, since the number of the resistors is greatly reduced, also the effect of process gradient over the voltage reference scale and the “mobile” scale is reduced. As an example, the figure 11 compares the effects the above nonlinearity, in terms of effective bits, for the “classical” full-flash realization and the proposed one. The behaviour of both the structures is compared with an ideal ADC response. Three values of the coefficient α are considered, namely .01, .03, .05 and the simulation is performed for three word lengths: 10 bit, 12 bit and 14 bit respectively. The simulation has been carried out by a MATHCAD program.

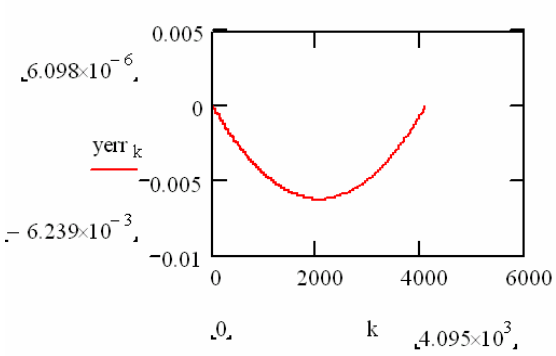


Fig. 9. – Error of the reference voltage scale of a “classical” full flash ADC (12 bit) induced by the process gradient.

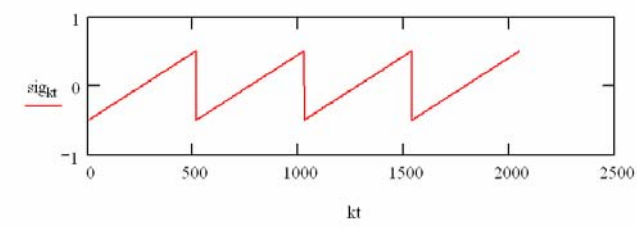


Fig. 10. Input signal used in determining the effective bits of the proposed architecture.

4. CONCLUSION

An innovative theory, already proposed and applied to the realization of reduced complexity ADC architectures [6] has been modified to obtain the realization of logarithmic ADC. This modified theory allows the possibility of a simple separation of the characteristic and the mantissa of the logarithm. This fact greatly reduced the number of comparators in the thermometric scale. The reduction of the number of resistors in the voltage reference scale id an intrinsic property of these caliper rule based realizations. It follows that the application of this theory allows the possibility of realization of logarithmic converters for large word lengths.

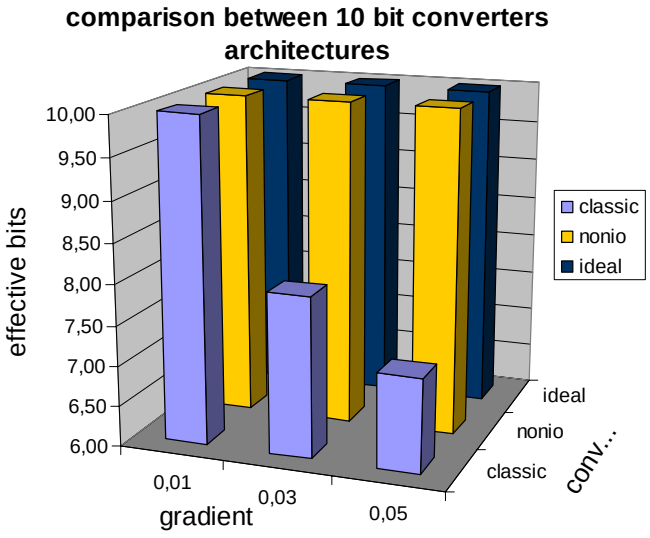


Fig. 11-a) comparison between 10-bit architectures.

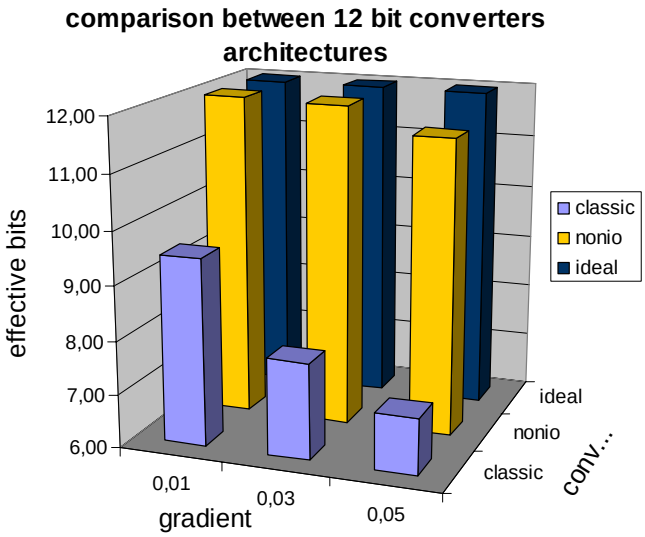


Fig. 11-b) comparison between 12-bit architectures.

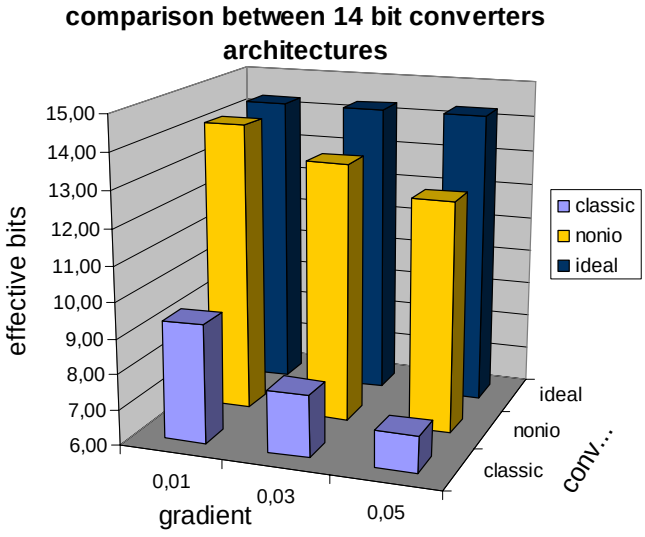


Fig. 11-c) comparison between 14-bit architectures.

REFERENCES

[1] Adams, R.W.: "Filtering in the log domain". Presented at 63rd, AES Conf., New York, May 1979, Preprint 1470

[2] Wilson, B.; Al-Gahtani, M.:"Improved logarithmic converter based on a transconductance feedback amplifier", Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium onVolume 1, 6-9 May 2001 Page(s):651 - 654 vol. 1

[3] Frey, D.R.: "Log-domain filtering: An approach to current-mode filtering", IEE Proc. G, 1993, 140, pp. 406-4 I6

[4] Guilherme, J.; Franca, J.E.:" New CMOS logarithmic A/D converters employing pipeline and algorithmic architectures", Circuits and Systems, 1995. ISCAS '95., 1995 IEEE International Symposium on, Volume 1, 28 April-3 May 1995 Page(s):529 – 532

[5] Francesconi, F.; Maloberti, F.:"A low power logarithmic A/D converter", Circuits and Systems, 1996. ISCAS '96., 'Connecting the World'., 1996 IEEE International Symposium on, Volume 1, 12-15 May 1996 Page(s):473 - 476

[6] R. Lojacono, "Reduced Complexity Full-Flash ADCs**"** Proc. Of 10th Workshop On Adc Modelling And Testing,12-15 September 2005, Gdynia and Jurata, Poland.

[7] Lojacono R., *Italian Patent n° RM 2005 A000086, 28/02/05*

[8] Hill, D.A.; Haworth, D.P.: "Accurate measurement of low signal-to-noise ratios using a superheterodyne spectrum analyser", IEEE Transactions on Instrumentation and Measurement, Volume 39, Issue 2, April 1990 Page(s):432 – 435

[9] Sangiovanni Vincentelli, A.; Re, M.; Lavagno, L.; Cardarilli, G.C.; Lojacono, R.;"Analysis of the quantization noise effects on the SQNR behaviour in analog to digital conversion" ISCAS '99. Proceedings of the 1999 IEEE International Symposium on Circuits and Systems, Volume 2, 30 May-2 June 1999 Page(s):334 - 338