XVIII IMEKO WORLD CONGRESS
Metrology for a Sustainable Development
September, 17 – 22, 2006, Rio de Janeiro, Brazil

ADC LOOK-UP TABLE BASED POST CORRECTION COMBINED WITH DITHERING

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Abstract: The main purpose of this paper is to present the external correction of analog to digital converters (ADC) integral nonlinearity and quantization noise based on the look up table method combined with the averaging filter and dithering method. The low code frequency component of integral nonlinearity (^{LCF}INL) is reduced by the error table of the look up table method, the high frequency part (^{HCF}INL) by sine wave dithering signal mainly.

Keywords: integral nonlinearity (INL), look up table method, dithering

1. BASIC INFORMATION

Development of digital communication systems evoke increasing requirement on the ADCs parameters especially in the range of sampling rate and wide-band linearity. This effort is linked with the reduction of the integral nonlinearity (INL) of ADCs, which influence distortion of the processed signals. Several methods were designed to reduce INL, such as Bayesian filtration, Voltaire filtration or Look up table method, applied in this topic experiments.

Integral nonlinearity is defined as the error between ideal and the real decision level for codes *k*, measured after offset and gain error correction. More often used definition is expressed like a ratio error between ideal and real decision level for each code and quantization step Q [1].

Integral nonlinearity is a function of two parameters, code bin *k* and slope signal *s* (2). Experimental results shows, that the impact of the signal derivations of the order higher than one do not enhance ADC modeling. In this case, integral nonlinearity can be defined using two dimensional function (1), where:

$$INL_Q(k,s) = \frac{\varepsilon(k,s)}{Q} \tag{1}$$

$$s = k(i) - k(i-1) \tag{2}$$

The quantization step Q could be defined according to [1] as (3):

$$Q = \frac{1}{(2^N - 1)} \sum_{k=0}^{2^N-1} W(k) \tag{3}$$

The INL can be modeled as a sum of high frequency (^{HCF}INL) and low frequency (^{LCF}INL) code component, static or dynamic according to the concerning frequency of signal (slope signal) [5][2].

The high frequency code component ^{HCF}INL is modeled by differential nonlinearity characteristic of used ADC, especially its important peeks.

Taking in account dynamic signal with slope *s* the low code frequency component could be expressed as two dimensional polynomial function of actual signal code *k* and slope *s* (4):

$$INL(k,s) = \prod_{i=0}^{I} \prod_{j=0}^{J} B_{i,j} k^i s^j \tag{4}$$

The model of the ^{LCF}INL(k) used further is for maximal order of *I=J=2* for dynamic (5) and static case (6). Here the first coefficient express offset, second the gain error and the other nonlinearities:

$$^{LCF}INL(k,s) = B_0 + B_1 k + B_2 k^2 + B_3 s + B_4 ks + B_5 s^2 \tag{5}$$

$$^{LCF}INL(k) = B_0 + B_1 k + B_2 k^2 \tag{6}$$

The ^{LCF}INL code component of integral nonlinearity for average slope s=0,3094 is shown in *Fig. 1.*

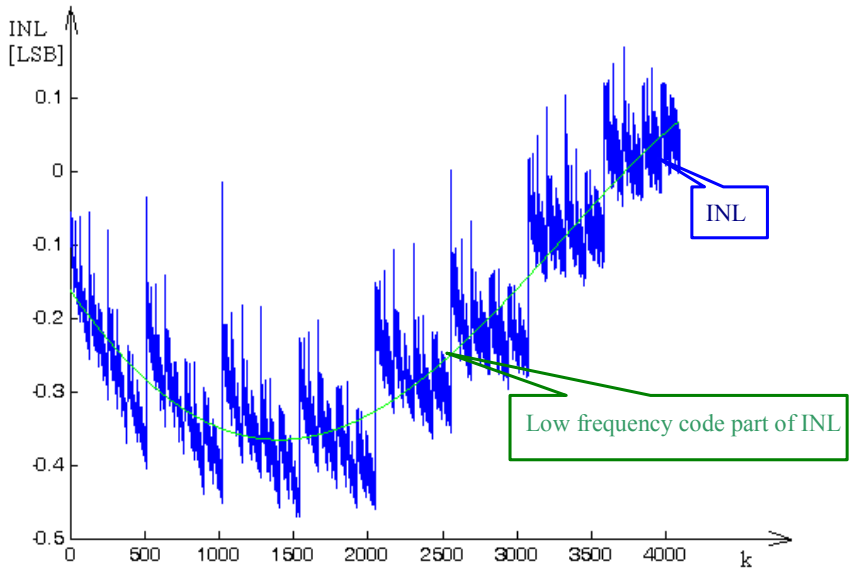

Fig. 1. Integral nonlinearity of Lab-Pc-1200 and low frequency code component for average slope s=0,3094

Look up table method (LUT) exploits for addressing the error table the actual and the previous signal samples to correct incoming signal. The value of the sample is $k_x(i)$ and the difference $k_x(i)$- $k_x(i-1)$ determines the actual slope $s(i)$.

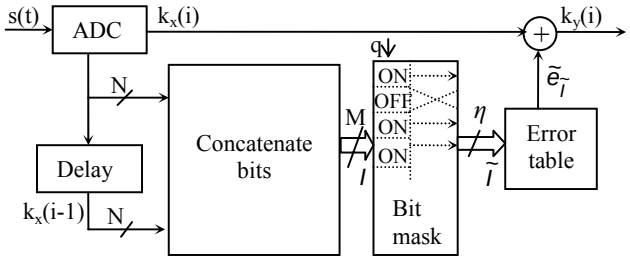

Fig. 2. The Look up table method

The LUT structure in *Fig. 2* was presented in [3]. This structure actual N-bits ADC input word $k_x(i)$ is concatenated together with the previous input word $k_x(i-1)$ in concatenate device (*Concatenate bits*). The address I with length $M = 2N$ bits is created by this way. The full addressing space represented by $2N$ bits can by reduced by the *Bit mask* to the address $\tilde{I}$ with length η bits, which addresses the *Error table* of size 2^{η}. The INL of ADC can be visibly declined using the right *Error table* definition. The content of the *Error table* is the rounded value $\tilde{e}(k,s) = round\{INL_Q(k,s)\}$ obtained in the testing phase. The huge volume of error levels can be reduced to the acceptable level by suitable *Bit mask*. The reduced address $\tilde{I}$ at the output of the concatenate block is a masked function of k ,s $\tilde{I} = \varphi(k,s)$. The mask contribution is clearer in determination of slope, where highest bits of the slope signal are very rare. Output of the *Error table* $\tilde{e}_{\tilde{I}}$ together with the distorted output word forms output value $k_y(i)$ in the correction block by the following way:

$$k_y(i) = k_x(i) + \tilde{e}_{\tilde{I}} \qquad (7)$$

The quantization noise does not allow nonlinearity correction under the level of quantization step Q.

Averaging filter of length 2^L increases amount of the ADC levels virtually. The samples are acquired by ADC with oversampling frequency f_{os}. The sampling frequency f_s after averaging procedure meets the sampling condition (8):

$$\frac{f_{os}}{2^L} = f_s > 2 f_{\max} \qquad (8)$$

where f_{max} is the maximal frequency of the input signal. Because of averaging procedure the quantization noise decreases (9) [6] and the border of possible nonlinearity correction moves to $INL > 1/2^L$:

$$E_{kv} = \frac{Q}{\sqrt{12}\sqrt{2^L}} \qquad (9)$$

The appropriate *Concatenate* and *Bit mask device*, which adds β *($\beta=\eta-N\leq N$)* bits of slope signal to the N bits of actual sample, creates the structure with changed precision. The precision of investigated structure increase equally to the virtual variance of quantization step wide Δ [7]:

$$\Delta = 2^{-\beta} Q \qquad (10)$$

The quantization noise and the high code frequency component of INL (^{HCF}INL) of ADCs can be eliminated by adding dithering signal to the analogue signal before conversion.

The first condition for dithering process is that the *dither signal* could not correlate with the input signal. The peak to peak value of the dithering signal larger than maximal ^{HCF}INL represents second condition.

The frequency of dither signal should be set to the value f_d :

$$f_d = \frac{frequency\ of\ input\ signal\ .\ number\ of\ samples}{2^L} \quad (11)$$

This way the averaging filter suppresses the dithering signal as used in the nonsubtractive structures [4].

2. DESIGNED CORRECTION STRUCTURES

Two structures were studied to reduce INL and quantization noise of ADCs.

The first novelty of the proposed *structure 1* in *Fig. 3* deals with dynamic ^{LCF}INL model. In the case of this realization signal after moving through the ADC enters in the *Concatenate device*, in which the actual sample of size *N* bits is joined to the distance between actual and previous sample. *Bit mask* removes higher bits of joined distance (slope) to reduce size of ADC output word to *N+NOB,* which addresses the *Error table* after averaging using *Averaging filter*. This averaging filter averages 2^L samples to increase amount of the converter bits to *N+NOB+L* virtually. 2^N points of ^{LCF}INL dynamic model characteristic determines $2^{N+NOB+L}$ elements of the *Error table* created using linear approximation. The output of the *Error table* is deducted from the *Averaging filter* value created by the averaging 2^L of signal samples from the ADC. This structure does not treat the quantization noise and high frequency part of INL.

The second studied scheme (*structure 2*) utilizes the same with dynamic ^{LCF}INL model to reduce low frequency part of INL and the triangle wave dither signal to reduce ^{HCF}INL and quantization noise (*Fig. 4*). Because of nonsubtractive dithering, dither signal is suppressed by the averaging filter.

In data evolution system, digital signal from the correction device is deducted from the reference signal after averaging. To evaluate results was used the mean square error (*MSE*).

There were made few computer simulation experiments with the ^{LCF}INL dynamic model as the content of the *Error*

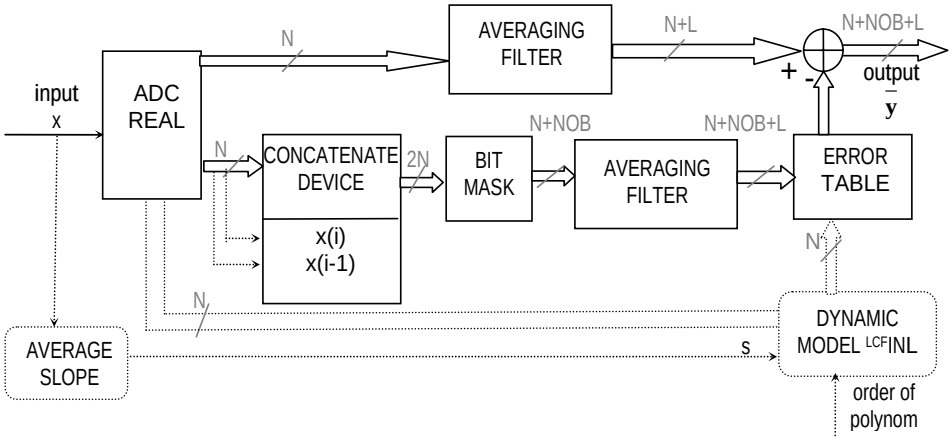

Fig. 3. Correction structure 1

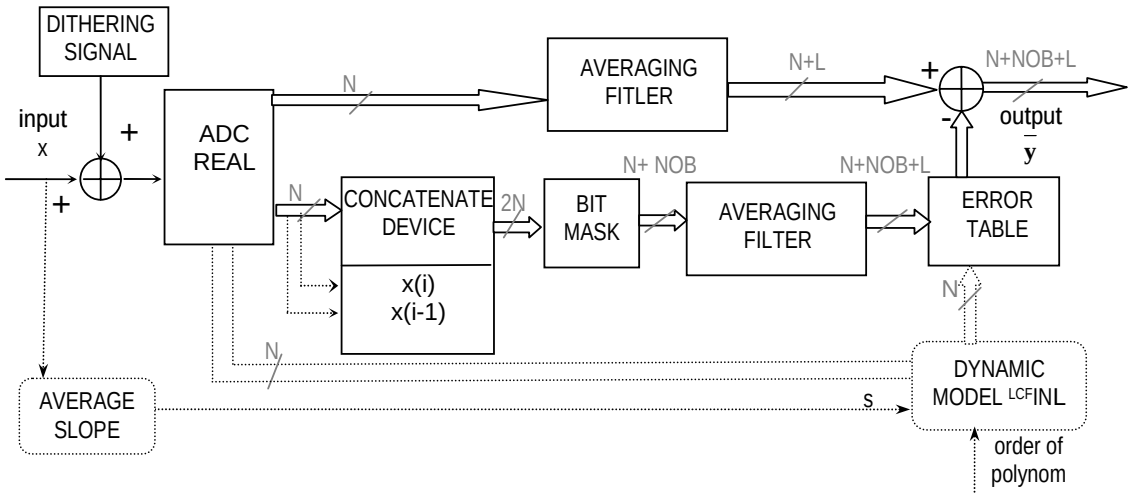

Fig. 4. Correction structure 2

table and with the triangle wave dithering signal. As a test signal was used sine wave signal, the real ADC was modeled as the ideal one with the embedded integral nonlinearity of Lab-Pc-1200 (see *Fig.1*) and its multiples.

The experiments showed, that increasing amount of averaged samples created by averaging windows of 2^L samples (*Fig. 5*) and increasing value of parameter *NOB (Fig. 6)* lead to decline of *MSE* and better accuracy of measured system.

The relation between ^{LCF}INL(k) and ^{LCF}INL(k,s) was also studied. The implementation of ^{LCF}INL(k,s) low frequency code component model as the function of slope *s* and code bin *k* instead of one parametric description ^{LCF}INL(k) offers the higher accuracy correction results as is shown in *Fig. 8*.

It was expected, that dithering can reduce high frequency part of INL and quantization noise visibly. It was used triangle wave dither signal according to the *structure 2*, with frequency set to the appropriate frequency (see expression (11)) and amplitude set to the half of quantization step. In figure *Fig. 7* is illustrated difference between *MSE* acquired using dithering *structure 2* and *structure 1* without dithering. The experiments showed that this kind of dithering propose better correction results and increase accuracy of converted signal.

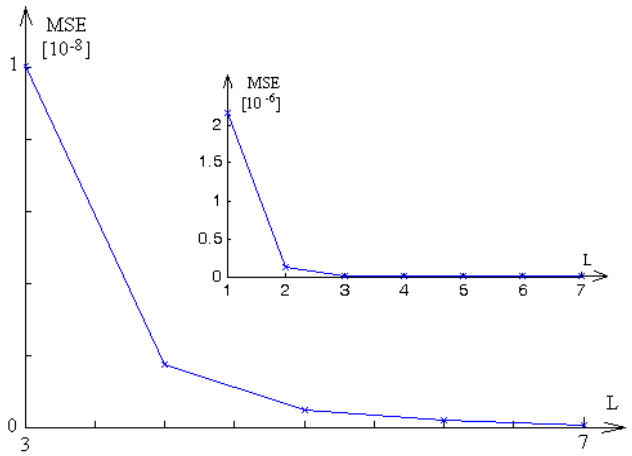

Fig.5 The correction effect of the number of averaged samples

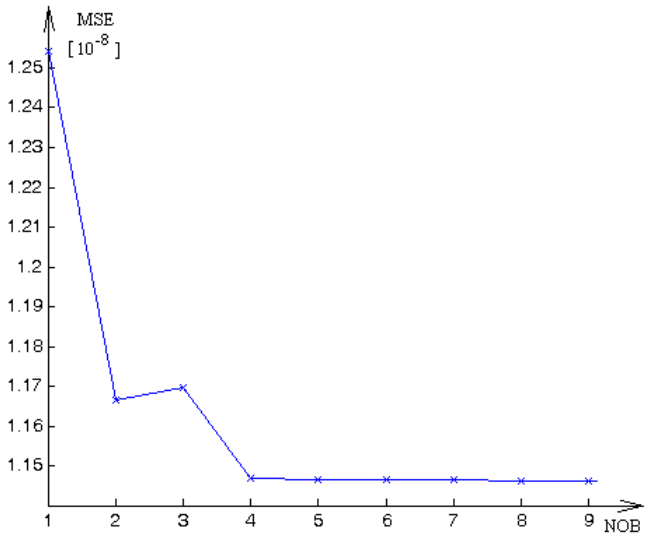

Fig.6 The correction effect of the shape of the bit mask

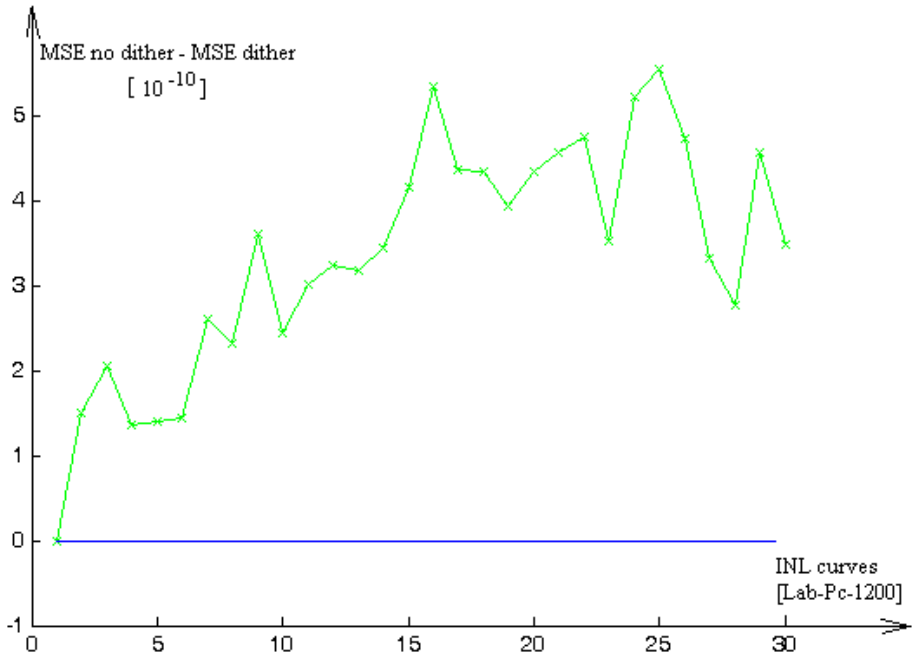

Fig.7 Comparison of the structure 1 and structure 2 correction effect

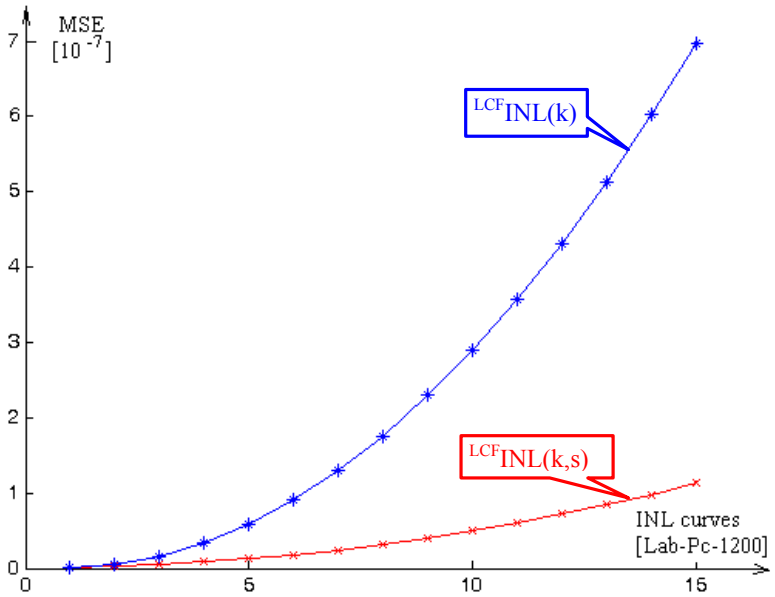

Fig.8 Comparison of the INL model dependent on the slope signal and INL dependent on the code level only

Theoretical results and results of simulation will be verified by the practical testing of the ADC embedded on PC plug-in board PC-LAB-1200 by National Instruments.

3. CONCLUSION

The main idea of the performed study was to asses contribution of the Look up table method and dithering of the correction. The proposed correction structures contribute to the higher accuracy of ADC converted signal.

Acknowledgement

This research has been supported by Grant Agency of the Slovak Republic VEGA grant. No.1/2180/05.

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