

DSP-BASED CONTROL OF THE CORIOLIS METER

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Abstract: According to digitalization trend in measurement technology, we approached to design the Coriolis meter using digital signal processing (DSP). This paper presents the results of DSP-based control of the meter resonance frequency, which is the condition for its regular operation. Procedure of data manipulation for precision digital harmonic synthesizer and phase-locked loop controller, which run in software on DSP, is presented. Digital control and measurement show advantages in flexibility, repeatability and stability of operation. Developed system for resonance frequency control shows response quickness in order of second and stability in order of 1 ppm.

Keywords: Coriolis flowmeter, digital signal processing, digital signal synthesis.

1 INTRODUCTION

The Coriolis meter is used for direct measurement of fluid density and mass flowrate [1]. Its regular and continuous operation is conditional on continuous vibration of its measuring tube at the resonance frequency. In our laboratory, a phase-locked loop (PLL) is using to control this frequency state. The PLL maintains a proper phase difference between the excitation and detection signal of the Coriolis measuring tube.

In the beginning stage of the control system development, the exciter was supplied using analog voltage-controlled oscillator, and the controller was programmed in the LabVIEW environment on PC computer [1]. This paper presents the Coriolis meter control using DSP (Digital Signal Processing) board. We used DSP with floating point numeric that assured us negligible quantisation effects. If charge and power amplifiers are excluded from control loop all stages are digital. Properties of those digital elements assured us cost-effective repeatability and accuracy. Effects of discrete time and amplitude influence static and dynamic behavior of measurement system.

2 THEORETICAL BACKGROUND

2.1 Digital synthesis of harmonic signal

Excitation of the Coriolis meter tube with low damping factor (high quality Q) requires harmonic source with high frequency resolution and stability, quick response to desired frequency and continuous phase. We can obtain a harmonic output data stream iterating simple sequence of equations

$$\psi[i] = \psi[i-1] + 2\pi \frac{f[j]}{f_s} , \quad (1)$$

$$u_s[i] = U_s \cdot \sin(\psi[i]) , \quad (2)$$

where i is iterator of synthesising loop, j is iterator of PLL control loop, f_s is sampling frequency and $f[j]$ is desired output frequency. Since phase angle $\psi[i]$ is obtained incrementally, even large jumps of $f[j]$ could not harm the phase continuity of output stream $u_s[i]$. It is also true, that output frequency changes instantaneously with changing desired $f[j]$, because output frequency is dependent of phase increment.

2.2 Discrete-time phase comparator

In multiplying phase comparator [3], we need two sinusoidal waveforms $u_i[nT]$ and $u_o[nT]$. In discrete-time domain it can be expressed as

$$u_i[nT] = U_i \cos(\omega nT) \quad \text{and} \quad u_o[nT] = U_o \cos(\omega nT + \phi) , \quad (3)$$

where U_1 and U_2 are their amplitudes and T is sampling time interval [4]. Multiplying same indexed samples of both signals leads to equation

$$u[nT] = \frac{1}{2}U_1U_0\cos(\phi) + \frac{1}{2}U_1U_0\cos(2\omega nT - \phi). \quad (4)$$

The first of the summands is time independent DC component and the second one is time dependent AC component. The component that must be derived from multiplied data set is DC component. DC component is actually measure of phase difference and its value is negative for $90^\circ < f < 180^\circ$ and positive for $0^\circ < f < 90^\circ$ (this also states for negative values of f). When f is $+90^\circ$ or -90° , value of DC component is 0. These properties can be used in design of PLL control systems.

3 EXPERIMENTS

3.1 Measuring system

The measuring system of DSP controlled model of the Coriolis meter is schematically presented in Figure 1. Construction details about its mechanical part could be found in reference [1].

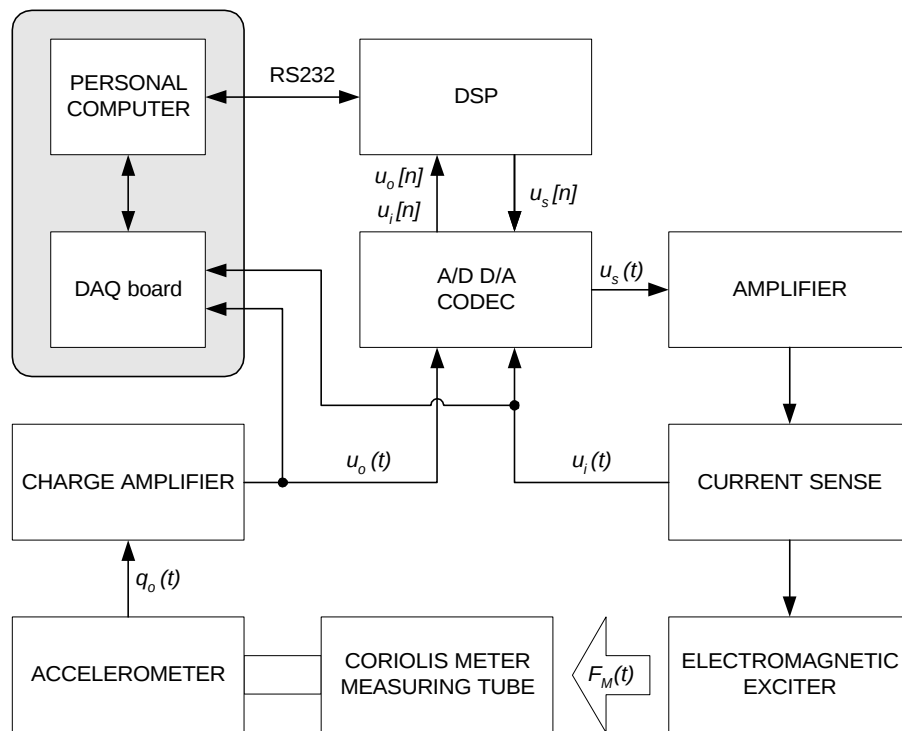


Figure 1. Block diagram of the measuring system.

Core of the measuring system is Analog Devices ADSP21061 SHARC single-chip 32-bit floating point DSP. It has 1 Mbit of on-chip reconfigurable dual ported RAM and runs on 40 MHz where it is capable of 80 MFLOPS sustained performance. Data transfer between PC runs through RS232 communication port at 115 kbit/s. Among communication tasks DSP performs real-time processing of measured data and synthesis of harmonic signal for the Coriolis tube excitation.

DSP's window to the analog world is Analog Devices AD1847 codec. AD1847 is 16 bit $\Sigma\Delta$ (sigma delta) codec, configured for two channels A/D conversion and single channel output D/A conversion. Sampling frequency is 48 kHz - the same for input and output converters. Dynamic range is better than 70 dB and signal to intermodulation distortion is typically 83 dB. Differential nonlinearity is ± 0.5 LSB.

Synthesised harmonic excitation voltage $u_s(t)$ from codec is first fed to an amplifier. Amplifier was custom made in our laboratory (low distortion, low noise, frequency range DC to 50 kHz). Amplifier converts high input impedance to low output impedance and also amplified voltage signal by gain of 3. Amplified signal is applied to the excitation coil (solenoidal type). Interaction of magnetic fields created by energised coil and small permanent magnet inside (fixed on the measuring tube) creates force $F_M(t)$. This force is proportional and in-phase with excitation current, of course stray capacitance must

be below certain value for that to be true. Current is sensed by a normal resistor that provides voltage signal $u_i(t)$ proportional and in-phase with excitation current.

A harmonic movement of the measuring tube is detected by a piezoelectric accelerometer Kistler, type 8044. Charge $q_o(t)$ from accelerometer was converted to voltage $u_o(t)$ with charge amplifier Dewetron DAQ-CHARGE, configured to gain 1 V/pC [1].

Proper operation of PLL using DSP was confirmed with reference measuring system [1] realised with National Instruments DAQ board (type PCI-6031E) and graphical programming language G in LabVIEW environment [5].

3.2 PLL controller algorithm

PLL control algorithm is designed according to findings in Section 2.2. To satisfy equation (4), two input data streams must have zero offset. In continuous time systems, we would apply high pass filter with low enough cut-off frequency. Data stream in our discrete time system is stripped, therefore discontinuous. To remove effects of finite data length windowing have to be used. Hanning window is chosen because of its simple numerical relations that led to faster computation:

$$w[n] = 0.5 \left(1 + \cos \left(\frac{n\pi}{(N-1)/2} \right) \right); \quad n = -\frac{N-1}{2}, \dots, 0, \dots, \frac{N-1}{2}. \quad (5)$$

Other windows did not show observable benefits. Equation (5) represents algorithm for coefficients of window with N samples. DC value is obtained by calculating mean value of windowed input data set. AC value is actually square root of variance of input data set. Windowed data set has DC and AC values changed. If we want to get DC and AC values of original signal we must multiply them with scaling factors (DC with 2 and AC with 8/3 before square rooting). Block diagram of DC and AC estimation algorithm is shown in Figure 2.

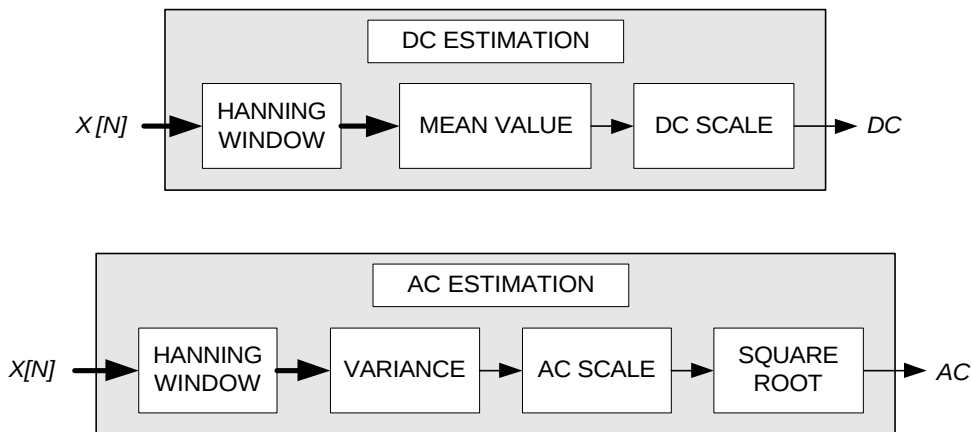


Figure 2. Computation of DC and AC estimator.

DC estimation algorithm allows us now to extract DC value of multiplied input signals, therefore AC component from equation (4) is removed. Further processing is graphically presented in Figure 3. One turn of processing loop can be also written in form of equation:

$$f[j] = f[j-1] + \frac{U_{DC}}{AC_o^2} \cdot K, \quad (6)$$

where $f[j]$ is output frequency and K regulation constant. Because U_{DC} is proportional to $U_o \cdot U_i$ and AC_o equals to U_o , increment of frequency is actually large when U_o is small (that is true far from the resonance frequency) and small when amplitude is high (that is true close to the resonance frequency). The whole PLL loop acts like integral feedback controller. Proper values of K have to be selected to assure stable operation of whole loop.

In our experiment, a time of 0,1 s is used for iteration of main control loop. That determines maximum time allowed to acquire one complete input data set $U_i[N]$ and $U_o[N]$. Number of samples N is actually determined by equation

$$N = \frac{f_s \cdot T_i}{D}, \quad (7)$$

where T_i is sample time of N samples data set acquisition and D is decimation factor that was set to 8. For rejection of conducted and radiated noise of power distribution network is advisable to choose T_i as multiple of period of power distribution network frequency (50 Hz). T_i set to 80 ms leads to $N=480$.

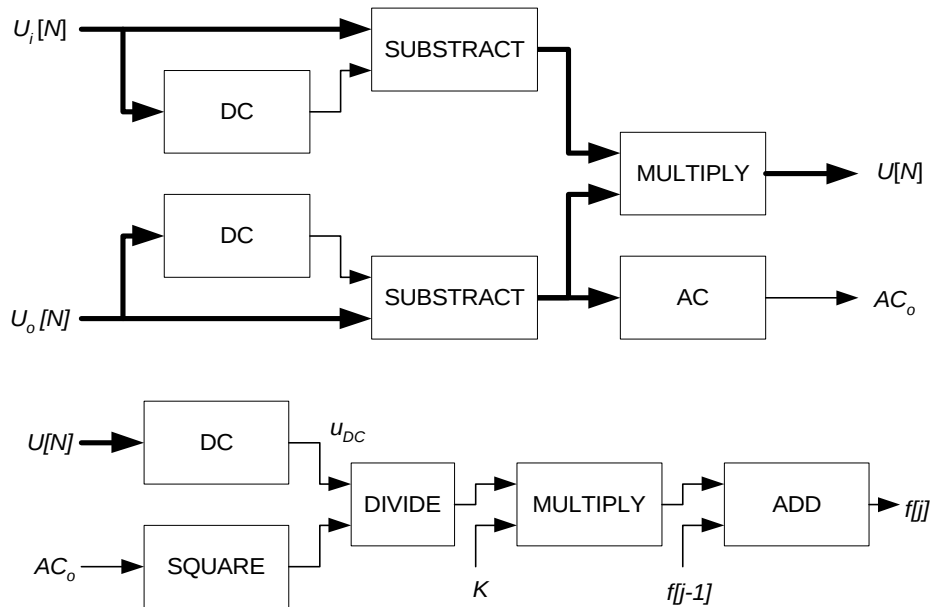


Figure 3. Numerical PLL algorithm.

3.3 PLL control system performance

At first static system performance was verified with reference phase meter. Measurements show that for proper values of K , there is a stable operation at $f = -90,0^\circ$. Phase deviation is less than $\pm 0,05^\circ$ (measured with DFT using 6 s of sampled data [1]). Measured steady-state frequency is shown on Figure 4, where dashed line represents calculated standard deviation that is 0,00012 Hz. One should note that Figure 4 has frequency range of 1 mHz.

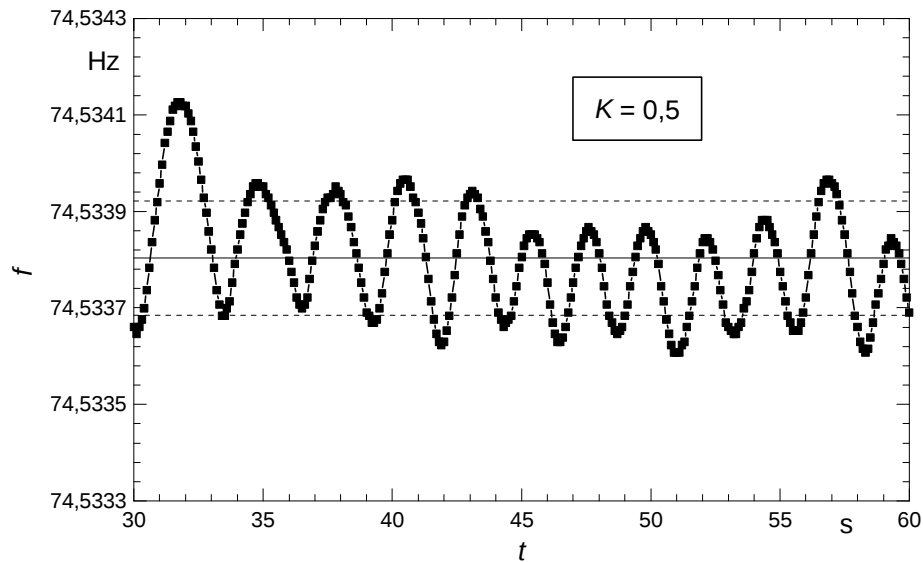


Figure 4. Measured steady-state stability of the resonance frequency control using DSP PLL.

Dynamics characteristics were measured in manner of time needed for output frequency to make first crossing of the unknown resonance frequency. The starting point is 100 Hz, so the change in

frequency is around 25,5 Hz. On Figure 5, it can be seen that control system finds unknown frequency in about 2 s. Theoretically, waveform ΔU represents $\cos(f)$ (equations (3) and (4)).

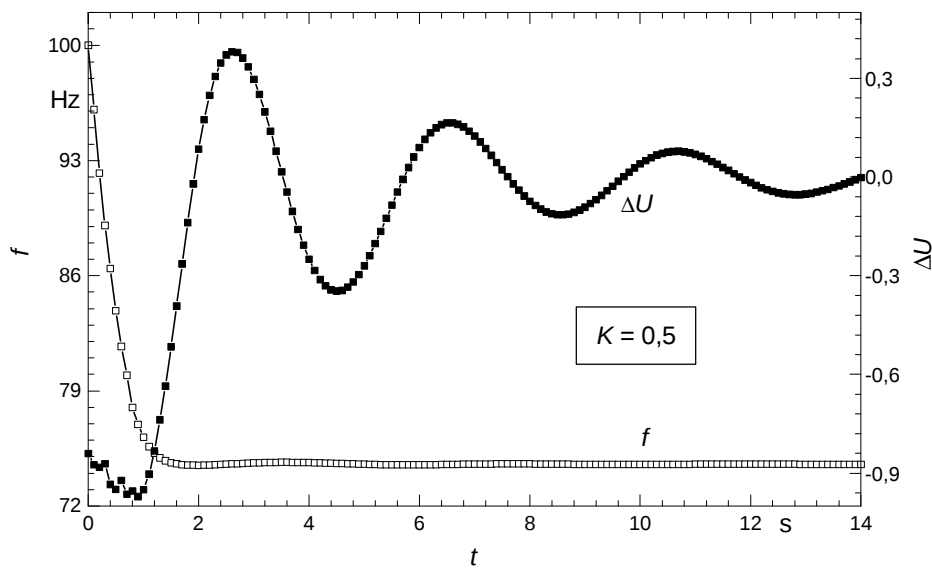


Figure 5. Measured response of PLL using DSP.

4 CONCLUSION

Use of digital signal processing in PLL design according to measured data shows significant improvements even so the same control algorithm was used as in literature [2]. We observed improvement in measured response time 3-fold and frequency stability of 30-fold!

Further improvements are expected mainly in form of optimisation of PLL quickness with use of advanced non-linear adaptive algorithm [6]. Achieved frequency stability of resonance control (1,6 ppm) is for application of Coriolis meter more than adequate and therefore further optimisation is not needed. Accuracy of floating point computation is in 0,1 ppm range, so dynamic range of floating point arithmetic for PLL control is adequate. Rapid software development is noticed since digitised signals are manipulated in manner of mathematical equations.

5 REFERENCES

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