

HARMONICS MEASUREMENT METHOD USING A DSP BASED ASIC

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Abstract: A compact, low cost harmonics measurement equipment, harmonics monitorTM, has been developed using a DSP based mixed signal ASIC. Each effective current harmonics from the basic frequency up to the 19th order harmonics and the total harmonics distortion ratio can be obtained in real time. In stead of using a conventional FFT method a 6th order, digital IIR filtering method was used for the accurate measurement. It allowed the computation to be in real time and the configuration of the main circuitry to be simplified into a single chip, thereby reducing the system cost. To compensate gain drop of ADC outputs over a continuous wide range of frequency the second order equalizing digital IIR filter was applied as well. The measurement accuracy has been realized within $\pm 0.5\%$ of full scale from the basic frequency up to 19th order harmonics frequency.

Keywords: Harmonics, Total harmonics distortion ratio, 6th order IIR filter

1 INTRODUCTION

Harmonics measurement in commercial AC power lines becomes more important to observe the degradation of power quality that is caused by harmonics generated from the amount of digital products these days. Containing Harmonics in commercial AC power lines is considered as one of environmental pollution, therefore, some regulation against it may be necessary in many countries.

There has been some precise, high performance harmonics measurement instruments using a precious FFT computational processor. However, there have little been compact, low cost and on-line harmonics monitors. To meet these requirements, we have developed a harmonics monitor using a programmable mixed signal ASIC [1]. This power metering ASIC (PMC) was originally developed for the computation of basic power metering functions. Harmonics measurement has been attempted this time as one of the additional applications.

2 ASIC OUTLINE

The block diagram of the ASIC is shown in Figure 1. This ASIC includes six, 14 bit resolution, first order δ - Δ ADC's, bit-serial DSP, and a 128 bite static RAM. The bit-serial DSP employs two programmable processors: a multiply-accumulate processor which executes metering and calibration algorithms, and a CORDIC [2] processor which computes metering output functions using division, square root, arc tangent, and vector magnitude as primitive functions. A variety of calibration algorithms [3] are employed to permit use with inexpensive sensors and therefore, reduce manufacturing cost. To achieve accurate operation over a wide, continuous range of frequencies, the ASIC measures the frequency of its input signals and adjusts filter characteristics and calibration coefficients accordingly. By changing the program, a necessary power metering function can be computed.

Except for these basic power-metering functions the computation of the specific application such as harmonics measurement can also be possible using the digital filtering technique which include high pass, low pass, and band pass filtering. The filtering method employed a high order IIR filtering technique, thereby realizing the real time measurement output.

3 MEASUREMENT ALGORITHM

Two kinds of harmonics measurement were considered: (1) each effective current harmonics from the basic frequency up to 19th order harmonics, and (2) the total harmonics distortion ratio.

3.1 6th order inverse Chebchef band pass filter

The effective current harmonics computation was executed by the 6th order inverse Chebchef band

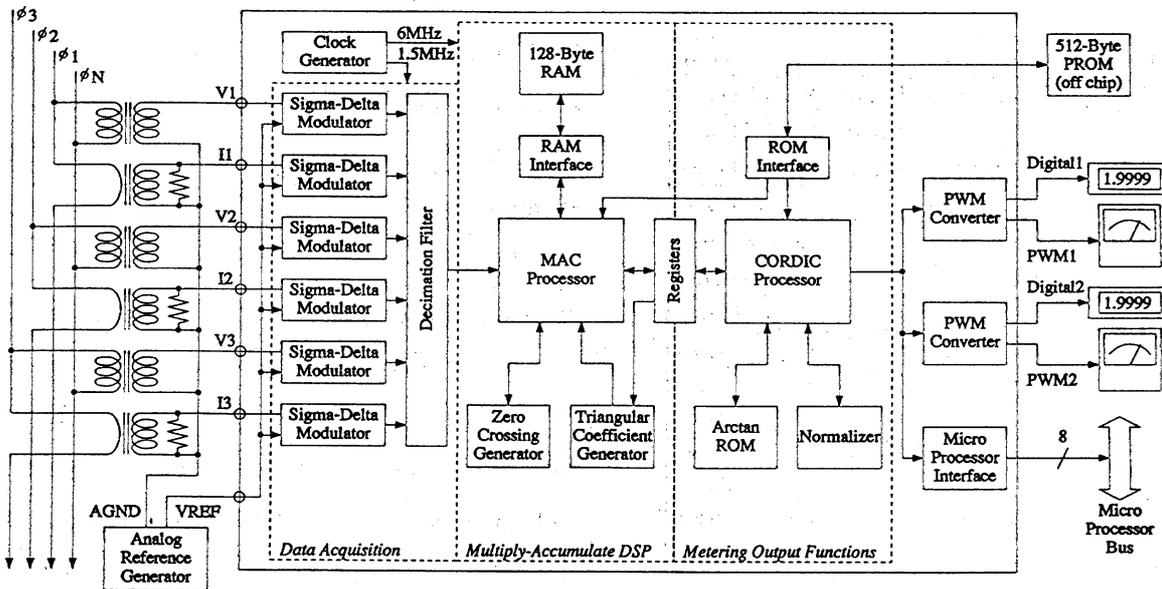


Figure 1. Block Diagram of the ASIC

pass filter (BPF). The BPF was composed of three-second order IIR filters. The transmission function $H(z)$ is written as follows:

$$H(z) = \frac{N_1 \cdot z^2 + N_2 \cdot z + N_3}{z^2 + N_4 \cdot z + N_5} \cdot \frac{N_6 \cdot z^2 + N_7 \cdot z + N_8}{z^2 + N_9 \cdot z + N_{10}} \cdot \frac{N_{11} \cdot z^2 + N_{12} \cdot z + N_{13}}{z^2 \cdot N_{14} \cdot z + N_{15}} \quad (1)$$

The filter is designed such that the signal rejection ratio over the stop band is less than -40dB. As an example the constants obtained for the 50 ± 5 Hz BPF are shown as follows:

$$\begin{aligned} N_1: & 2.956E-3, N_2: 0.000, N_3: -2.956E-3, N_4: -1.981, N_5: 9.925E-1, N_6: 1.899E-1, \\ N_7: & -3.771E-1, N_8: 1.899E-1, N_9: -1.984, N_{10}: 9.964E-1, N_{11}: 3.648E-1, N_{12}: -7.263E-1, \\ N_{13}: & 3.648E-1, N_{14}: -1.986, N_{15}: 9.967E-1 \end{aligned} \quad (2)$$

The characteristics of the 6th order inverse Chebchef band-pass filter are shown in Figure 2. In order to lower the quantum noise error, three-second order IIR filters in serial order were more effective than using a single 6th order filter. The reason is the fact that the signal ranges in each second order filter take more appropriate span than in the single 6th order filter.

In each harmonics frequency these constants must be set respectively. Each harmonics computation from the basic frequency up to 19th order frequency is performed by selecting the corresponding program stored in a ROM for the PMC ASIC. To obtain some of the harmonics in some certain period, the corresponding programs must be addressed. In actual circuit design, the programs in a ROM are selected by a CPU properly as shown in Figure 3.

3.2 Second order equalizing digital filter

The gain characteristics of the σ - Δ ADC's are inherently determined by its decimation filter. The gain drop is about -4.4 dB at 1,465 Hz, half the ADC sampling frequency. The compensation method was considered to keep the gain accuracy over a continuous frequency range up to the highest measurement harmonics frequency. The second order equalizing digital filter with the inverse characteristics against the ADC decimation filter was applied to compensate the gain drop of the ADC outputs. The 19th order harmonics against 60 Hz are 1,140 Hz. And the filter was designed such that the filter gain at 1,140 Hz equaled the inverse value against the ADC decimation filter, and that the filter gain over 1,465 Hz should be cut off. The transmission function $H(z)$ of the equalizing digital filter is shown as follows:

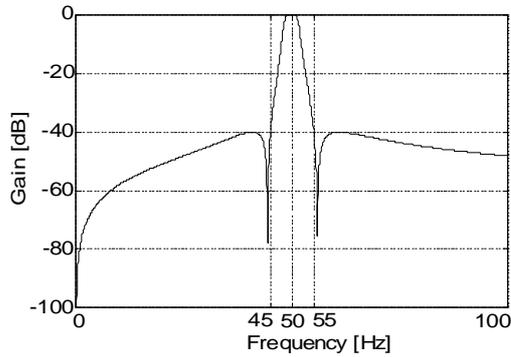


Figure 2. Characteristics of 6th order inverse Chebchev band-pass filter (50 Hz ± 5 Hz BFP)

$$H(Z) = \frac{N_1 \cdot z^2 + N_2 \cdot z + N_3}{z^2 + N_4 \cdot z + N_5} \quad (3)$$

The constants of N_i were calculated and determined as follows:

$$N_1: 1.295, N_2: 1.318, N_3: 6.467E-2, N_4: 1.318, N_5: 3.594E-1. \quad (4)$$

Characteristics of the filters are compared in Figure 4: 1) Decimation Filter, 2) Equalizing Filter, and 3) Total Characteristics. "Total Characteristics" mean the filter output of both the decimation filter and the equalizing filter. The total gain error of the filter was achieved within ± 0.5% of full scale from the basic frequency up to 1,140 Hz, the 19th order harmonics, as shown in Figure 5.

3.3 Total harmonic distortion

The ratio of the total harmonic distortion is shown in the following equation:

$$THD = \frac{((\hat{O}_2^n I_k^2) / (n-1))}{((\hat{O}_1^n I_k^2) / n)} \quad (5)$$

The denominator is equivalent with RMS current, and the numerator is RMS current rejected only the basic frequency. For the computation of the numerator, the 6th order inverse Chebchev high-pass filter [4] was used. The rejection ratio is less than -40 dB under 60 Hz and 0dB over 100 Hz.

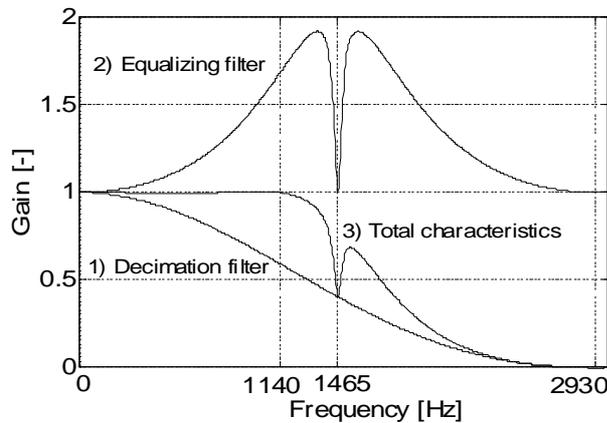


Figure 4. Filter characteristics: 1) Decimation filter, 2) Equalizing filter, 3) Total characteristics

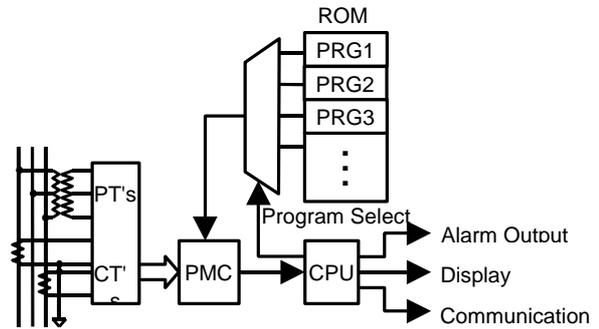


Figure 3. Circuit diagram of switching the ROM program

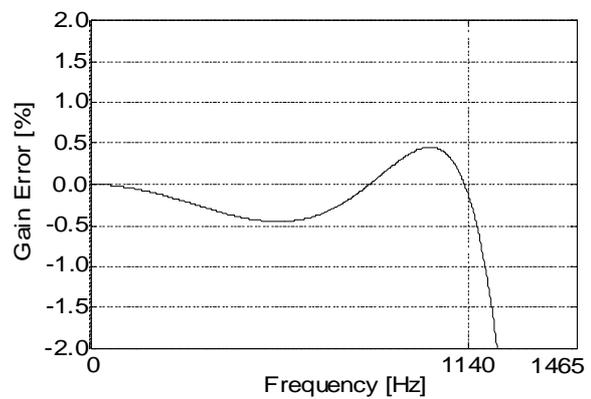


Figure 5. Gain Error Performance of the total characteristics

4 HARMONICS MONITOR, POWERCERT™

Using the digital filtering technique previously mentioned a compact, low cost, and on-line harmonics monitor was developed for energy saving, preventive maintenance of electrical equipment, and checking power quality degradation caused by switching power supplies and/or inverters. This monitor measures power and displays as instant power. In addition, voltage/current RMS value, effective harmonics value in each harmonics frequency, the direction of the harmonics current, the total voltage/current harmonics distortion ratio, and power factor can be measured and displayed selectively.

4.1 Block diagram of the harmonics monitor

The block diagram is shown in Figure 6. The PMC ASIC performs the power metering computation. On the other hand, the CPU performs switching control of the PMC programs and the interface control which includes the display, the serial output (RS-485), the analog output (4/20 mA), and the alarm output (on/off), and so on.

4.2 Specifications and electrical performance

The power line systems from three-phase three-line to two-phase two-line are covered by this monitor. The rated input voltage includes 110 V, 220 V, and 440 V in AC line. The specification and its accuracy are outlined in Table 1. The photograph of the harmonics monitor is shown in Figure 7.

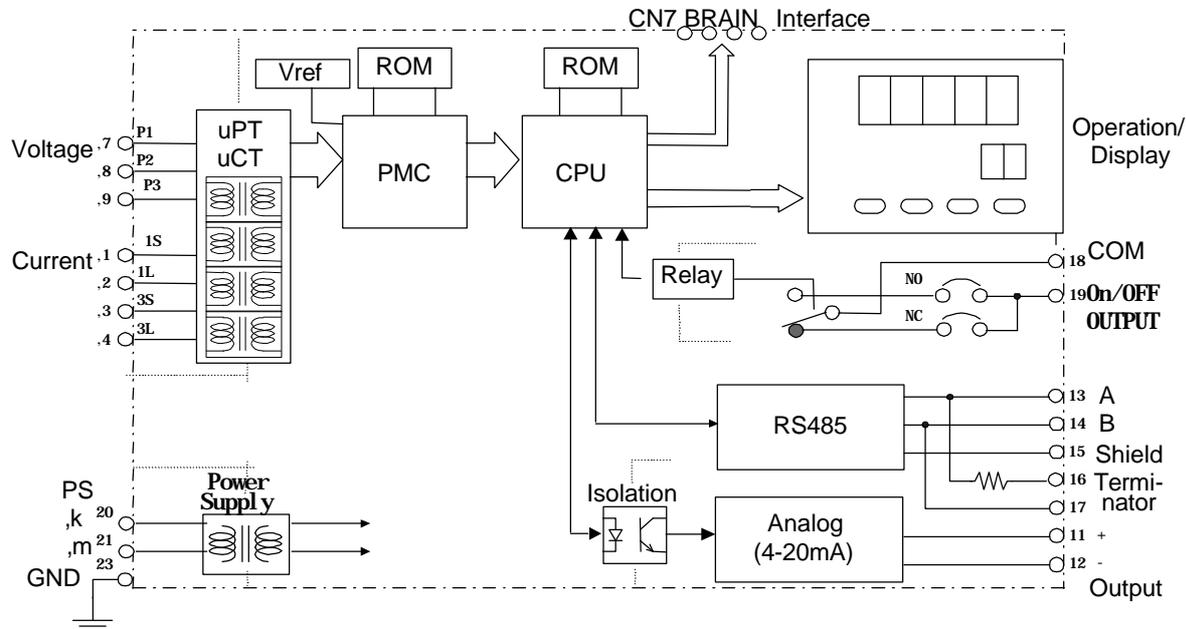


Figure 6. Block Diagram of harmonics monitor POWERCERT™

Table 1. Specification and Electrical Performance

Items	Specification	Accuracy
Power Line Systems	3-p 3-l, 2-p 3-l, 2-p 2-l	-
Rated Input Voltage	110 V / 220 V / 440 V AC	-
Rated Input Current	1A / 5 A	-
Total Harmonic Distortion	V (line to line), I (each line)	±2.5%
Effective Voltage / Current	V (line to line), I (each line)	±0.5%
Current Harmonics (each line)	1, 3, 5, 7, 11, 13, 17, 19th	±2.5%
Harmonics Current Direction	3, 5, 7, 11, 13, 17, 19th	-
Harmonics Current ratio	3, 5, 7, 11, 13, 17, 19th	±2.5%
Power, Power factor	-	±0.5%, ±2%



Figure 7. Photograph of harmonics monitor POWERCERT™
Size: 110 mm × 110 mm × 111 mm (H × W × D)

5 SUMMARY

Instead of using FFT method, the high order digital IIR filtering method has been attempted to measure harmonics. This approach is similar to analog filtering method so that a real time update can be achieved. In addition to ordinal power functions, many kinds of harmonics can also be measured only by switching program in a ROM. This approach brought us with a compact, low cost, and real time power measurement instrument.

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