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A MULTI-DSP-ARCHITECTURE FOR RAPID DETECTION OF SHORT CIRCUITS IN LOW VOLTAGE SYSTEMS

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Abstract: In order to detect short-circuits in low-voltage systems, a system was developed with several digital signal processors. The processors are housed on a DSP board, which is based on the VXIbus, and connected to one another by numerous communications pathways. These communications pathways allow for a high degree of flexibility and scalability. They are used to map the algorithmic structure on to the system. The system includes an interface board, which pre-processes, segments and distributes the data coming from the analogue-digital converters to the DSPs. This board generates a pulse with the segments, which determines the subsequent signal processing. As a result of the segmentation of the data flow, the 50Hz fundamental wave of the voltage system also remains in the segments as a disruptive DC component, and as an approximately saw-toothed signal component after its elimination. Methods are presented by which these interference signal components can be eliminated using non-linear filtering

Keywords: short circuit detection, low voltage A/D – converter.

1 INTRODUCTION AND FORMULATION OF THE PROBLEM

In electrical low-voltage systems a short-circuit can cause considerable economic damage, it is therefore both useful and necessary to quickly isolate the affected branch from the system. To date the procedures commonly used for this have had very high reaction times [2]. To avoid major damage, the short-circuit must be detected at a very early stage (t<500µs) and the affected branch switched off if the current has not substantially exceeded the rated current.

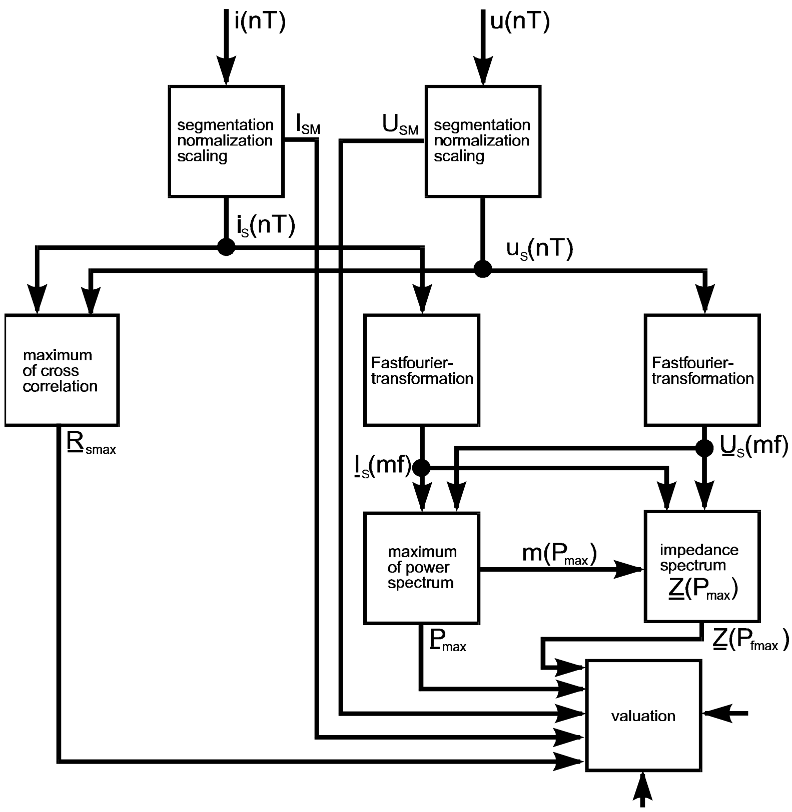

Figure 1: Algorithmic structure according to [3] for determining the parameter vector

This paper presents a concept with a number of digital signal processors (DSP), which enable a short-circuit to be detected within a time of t<500µs. This is to be made possible by spectral analysis of the conditions of the power lines in the frequency range above f>2kHz. This requires sampling the current and voltage at a sampling rate of at least 250 kSamples/s. These measured data are then used to calculate a parameter vector to assess the conditions of the power lines. The parameter vector is largely made up of the power spectrum, the impedance spectrum, the correlation between current and voltage, and the root-mean-square values of the two input quantities [2]. Figure 1 shows the algorithmic structure proposed in [3] for determining the parameter vector. In order to determine this parameter vector, it is necessary to subdivide the continuous data streams into data segments. Several such parameter vectors can be employed to assess the conditions of the power lines and thus achieve a certain level of statistical certainty. An increase in the number of parameter vectors calculated per unit time can be achieved by means of an overlapping method for generating and processing the data segments.

This definition of the problem with the specified constraints requires a system with a very high floating-point computing power. This computing power can be achieved with digital signal processors. The overlap in processing the data segments, together with the quantity of parameters to be calculated, means that the task can be distributed over several processors.

2 HARDWARE CONCEPT

The application described in the introduction requires a system that processes the data generated with the minimum delay in time. After a one-off initialization phase, the measurement data have to be processed continuously and without any loss. Continuous processing of the data at such a high data rate can only be achieved by means of concepts employing data-flow control [1]. Digital signal processing using data flow control calls for deterministic processing algorithms with fixed communication pathways, which means that, for example, iterative algorithms and dynamic data paths cannot be considered for the task. This requirement leads to a system with a structure that is determined by that of the algorithm used.

The system has been kept flexible and scalable so that various different evaluation algorithms can be tested for the application described. The core of the system, as shown in Figure 2 as a block diagram, is made up of a DSP assembly based on the VXIbus. This assembly is equipped with two type TMS320C40 digital signal processors from Texas Instruments and is also capable of modular expansion with so-called TIM modules (Texas Instruments Modules). Commercially available modules are equipped with up to two type TMS320C4x DSPs, hence the board can be extended up to a total of 14 DSPs.

Local and global memory is connected to each processor, these memory units are designed as static RAM. The local memory can only be used by the corresponding processor, and the global memory can also be accessed via a global data bus by every other processor on the DSP board. In the following text each unit on the DSP board – comprising DSP, local and global SRAM – will be referred to as a "node".

This DSP is fitted with several data pathways to permit communication and data exchange between the nodes or other assemblies. Worthy of mention are the communication ports, the VXI local bus, the global data bus and the VXIbus. The last of these is only important for the system in the development phase.

The communication ports are byte-serial interfaces Each. DSP has up to six of these interfaces especially designed for the exchange of data between the processors. It is therefore possible to classify the processors into structures of two or three dimensions. They are used on the DSP board to establish the data pathways between the individual nodes. One of these ports leads to the outside from each TIM module and each of the two permanent nodes, this makes it possible to use these data pathways for external communication as well, for example in communicating with another DSP board of the same type. The data transfer can occur via the DMA in a word-oriented or block-oriented manner. The achievable transfer rate is given as up to 60 MB/s [4] by the manufacturer. In this system the communication ports are used to map the algorithmic structure of the tasks onto the nodes.

The VXI local bus is a fast bus system mounted on the backplane of the VXIbus system. The data are also transferred in parallel on a byte-by-byte basis. While the communication ports are defined as point-to-point connections, the VXI local bus is organized as a daisy chain. This means the transmitter of the data must be always be located physically to the left of the receiver. Any bus susbscribers located inbetween have to be programmed as a bypass or a bypass and receiver. On the DSP board the data can be transferred from the VXI local bus to each node or simultaneously via so-called broadcast modi into the memories of several nodes. The achievable transfer rate for this bus system is given as up to 100 MB/s [6] by the manufacturer. In the system presented here, the VXI local bus is used to supply the pre-processed measurement data to the corresponding nodes.

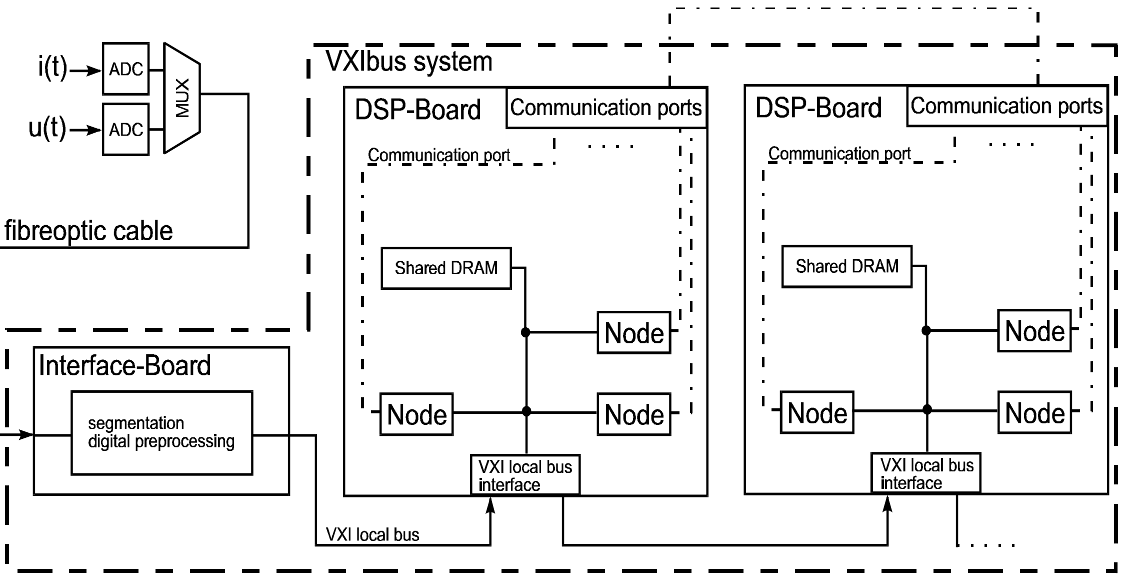

Figure 2: Schematic representation of the key structure of the short-circuit rapid detection system (block diagram)

As already indicated above, all the nodes on the board are connected via a global data bus. This means that each node can address and hence use the global memory of another node. In addition to these memories the DSP board has a central memory that can be used by very node via the global data bus. This leads to another variation in data exchange between the nodes. As is usual for such central data buses, here too, only two subscribers can exchange data at once.

Because of the numerous possibilities for coupling the DSP board with others of the same type, this system offers a high degree of scalability. Two of these boards can therefore perform the necessary calculations in parallel with the measurement data from current and voltage. The boards would then be located next to one another in the VXIbus system and be supplied with the measurement data via the VXI local bus.

An interface assembly developed by ourselves [7] functions as the data source for the DSP boards. This assembly is located in the daisy chain of the VXI local bus prior to the DSP boards. This interface board was developed in order to convert different interface standards. The VXI local bus, the communication ports and the VXIbus are mounted on the board as interfaces. A unidirectional connection can be made between any two of the interfaces. In addition, the interface board also accommodates a module that contains an FPGA (Field Programmable Gate Array), static RAM and a DSP. The data pathways on this board can be switched between the interfaces, then the data cannot be processed and the data transfer rates specified for the interfaces are almost achieved. The interfaces can also be indirectly connected with one another, then the module is incorporated into the data pathway. This enables the data to be processed while there is a flow of data. The data transfer rate is then determined by the application on the module.

The measurement data are supplied by an external measurement logger. The measurement logger is mounted outside of the VXIbus system to avoid stray pickup affecting the analogue circuit components. The data transfer from the measurement logger to the VXIbus system should take place serially via a fibreoptic cable. As the interface board on the front panel only has interfaces compliant with the standard of the communication ports, the serial data flow has to be converted. The data for the DSP board are processed with the interface board. This means that a data pathway is connected between the communication ports and the VXI local bus via the module on the interface board. The module has the task of working through the signal pre-processing algorithms and organizing the data into segments. The data segments are then transmitted as data blocks via the VXI local bus to the DSP board. The rate at which the blocks arrive at the DSPs determines the sequence for the signal processing that follows.

The data streams coming from the data loggers must be subdivided into segments for further processing. The length of the segments depends on the time requirement for detecting a short-circuit and the window length for calculating the frequency spectra with the FFT. Segment lengths of N_S=32 and N_S=64 can be considered for this system.

From each segment a parameter vector is determined which is used to decide whether a short-circuit is present. Overlapping segments are generated in order to increase the number of parameter vectors computed per unit time.

If several parameter vectors are available for each time unit, the decision on whether a short-circuit exists can be performed on the basis of several parameter vectors. This enables incorrect decisions resulting from isolated outliers to be avoided to the greatest possible extent.

3 MEASUREMENT ACQUISITION AND SIGNAL PREPROCESSING

3.1 Acquisition of measurements and decimation

An important part of the system presented here for the rapid detection of short-circuits is the component for measurement acquisition and the analogue and digital signal pre-processing. The problem described places high requirements on the measurement acquisition in terms of accuracy and speed. Current and voltage values are digitized with a 16-bit resolution. This resolution is necessary as the signals to be investigated only have an amplitude of approximately 1% of that of the fundamental wave, and the aim is to avoid an analogue filter for blocking the fundamental wave.

Higher-frequency signal components up to a max. 100 kHz are to be used for assessing the condition of the power lines. The analogue-digital converters (ADC) employed digitize the input signals at a sampling frequency of f_a=1MHz. This high sampling rate is necessary if high-order analogue anti-aliasing filters are not to be used on account of their unfavourable characteristics during transient response, and if disruptive overlap distortion is to be avoided.

The analogue circuit components for signal condition must exhibit high linearity and minimum intrinsic noise because of the ideally 96dB dynamic range of an ADC with 16-bit resolution only 56dB remains for the signal components to be evaluated. This is due to the fact that these only account for approximately 1% of the fundamental wave.

At a sampling rate of f_a=1MHz, there is not much time for extensive calculations between each two sampling values, decimation of the data rate is therefore not only useful but also necessary. Only a decimation filter with a floating average function can be considered for decimation. In contrast to other decimation methods, this type of filter has the advantage that it contributes to an improvement in the signal-to-noise ratio. In order to achieve a certain internal statistical dependence of the adjacent output values, a decimation filter is employed in which the number of sampling values used for averaging is greater than the decimation factor. In this case the sampling rate of f_a=1MHz is reduced by a factor of four to a sampling rate of f_{aD}=250kHz, with N_D=8 sampling values being used to obtain the average. According to [9], improvement in the signal-to-noise ratio can be estimated with $D_{SNR}=10\log_{10}N_D$, where a result of D_{SNR}=9dB is obtained.

3.2 Elimination of the 50Hz component

As already described, the sampled input signal is dissected into data segments and no assessment of the segment with a window function takes place at this stage to simplify the problem. The length in time of such a segment, t_s=256µs at for example N_S=64, is very small in relation to the duration of the period of the 50Hz fundamental wave, T_{50Hz}=20ms. The proportion of the fundamental wave in the segments then appears as a DC voltage offset. If the segments are reduced by their mean, a disruptive approximately saw-toothed time pattern results.

Now a method will be presented to eliminate these disruptive signal components. As the course of the interference variable may be regarded as known *a priori* and as stable in a rough approximation, it is possible to reduce this component to one curve by approximation, in which the approximated signal curve is subtracted from the measured values in one segment. If one considers the pattern of such a saw tooth, then it can be seen that curve is not linear, particularly at the peaks of the sinusoidal oscillation. In these cases linear regression would not be sufficiently accurate. A quadratic regression presented in [10] is used to compute an approximation function. This means that the course of the signal over time *y(t)* within a segment is approximately determined by:

$$\hat{y}(t) = a + b \cdot t + c \cdot t^2 \qquad (1)$$

The estimators *a*, *b* and *c* are determined by means of several help variables.

Using the estimator it is now possible to determine the corresponding estimated value for every individual measurement within the segment, and then subtract the former from the latter. This step for calculating the starting quantity, $y_S(t)$, is further clarified in Equation (2).

$$y_S\left(t_i\right) = y_i - \left(a + b \cdot t_i + c \cdot t_i^2\right) \tag{2}$$

To illustrate the effect of quadratic regression, this was employed in a simulation on a signal which corresponds as far as possible to an ideal voltage signal from a low-voltage system. A white noise with

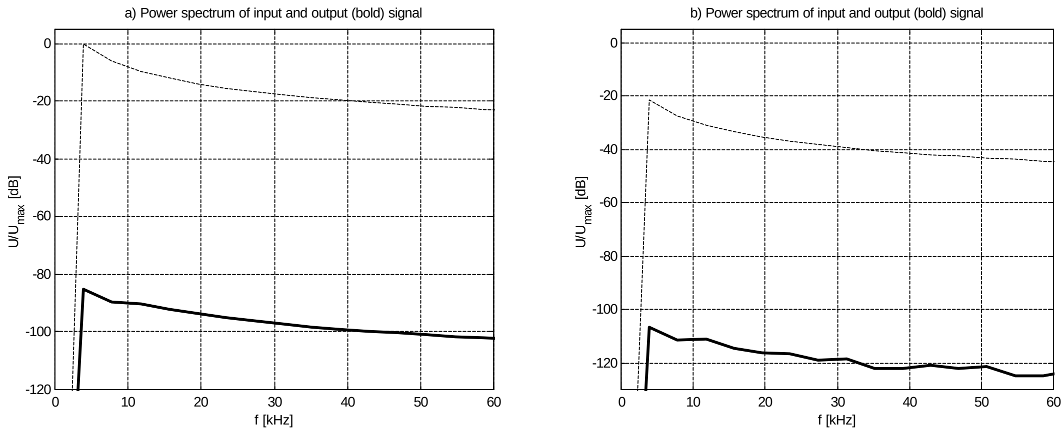

Figure 3: Power spectrum of the input signal and output signal (bold) for a segment at the position a) with a sharp rise and b) a maximum of the 50Hz fundamental wave

a signal-to-noise ratio of *SNR*=70dB was superimposed on the sinusoidal voltage. Figure 3 shows the power spectra of the signal curves in each segment before (input) and after (output) applying quadratic regression. In this case the segment length is N_S=64. The segment considered in Figure 3a) was taken from a point at which the slope of the sinusoidal oscillation is very large and hence the amplitude of the saw-tooth signal curve within the segment is also very large. For Figure 3b) a segment was taken from a point that lies at the maximum of the sinusoidal curve. At this point the slope of the curve is at its lowest and hence so too is the amplitude of the average-free signal section. In both cases the spectral influence of the interfering saw-tooth signal curve is attenuated by approximately 85dB.

Sliding regression is another variant for applying quadratic regression to the input signal. This method is applied before the data flow is subdivided into segments. Sliding regression has the advantage that it is independent of the segmentation of the data flow and no further time is lost for this signal pre-processing after segmentation. At a data rate of 250kSamples/s each measured value would merely be delayed by t_V=4µs. With this variant the proportion from the 50Hz fundamental wave can be attenuated by up to 70dB. These benefits are counteracted by a crucial disadvantage in that sliding regression presupposes a stationary fundamental wave. If a step-like change in the fundamental wave were to occur, the filter would need a lot of time to adjust to this.

When the two methods are compared, it can be seen that both are suitable for eliminating the interfering signal component of the 50Hz fundamental wave through non-linear filtration as far as possible. Because of the disadvantages of sliding regression just mentioned, the first of the two methods mentioned is given priority. When all the possibilities for parallel processing are exhausted, the time required for the computations amounts to a minimum of $3N_S$+4 command cycles for each segment.

SUMMARY

This article presents a system for the rapid detection of short-circuits in low-voltage systems. This system is based on the VXIbus and consists of an interface board for converting various interfaces, for digital signal pre-processing and for generating data segments from the continuous data flows, and of a DSP board for computing a sequence of parameter vectors for assessing the condition of the power lines. Assessment of this condition is performed by means of spectral analysis of the power lines in the frequency range above *f*>2kHz. Here, the signal component of the 50-Hz fundamental wave causes interference because of its large amplitude. Methods are introduced and discussed for eliminating these interference components by exploiting a priori knowledge through non-linear filtering.

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