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ALGORITHMIC SWITCHED-CURRENT AD CONVERTER WITH BUILT- IN SELF TEST FOR PRESSURE SMART SENSOR

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Abstract: The paper deals with the research and analysis of up-to-date system approach to SI AD conversion focused to pressure smart sensors for system integration. Built-in self-testing improves quality and reliability of analogue to digital conversion. This trend is encouraged by industrial implementation of pressure smart sensors including AD converter into sensor/actuator fieldbus driven systems.
Keywords: Algorithmic switched-current AD converter, self test, sensor

1 INTRODUCTION

In the process of a rapid development in the whole world of electronics, the man meets new opportunities for creating smart electronic circuits. Many signal processing applications require inexpensive, reliable sensors compatible with analogue circuitry. The challenge of combining sensors with the appropriate circuitry may be met by microsensors, i.e. silicon sensors with on-chip circuitry fabricated by using the same integrated circuit technology. Nowadays technologies enable a low-cost design even for application specific IC’s what has been mirrored in the growth of the use of electronics in any industrial branch.

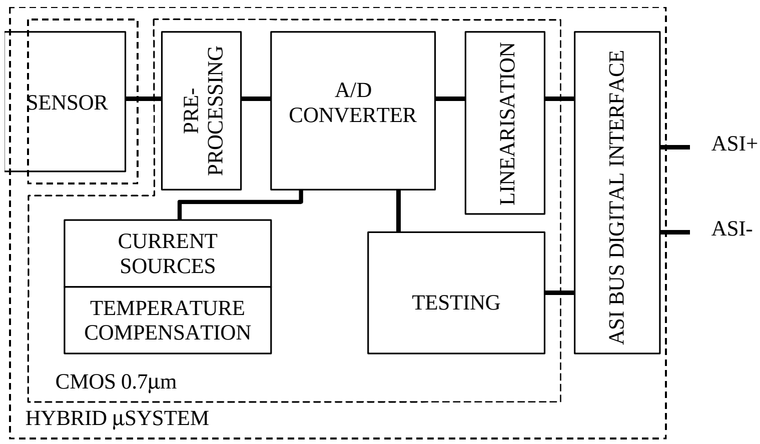

Figure 1. Basic diagram of an intelligent sensor with ASI bus interfacing

2 SENSOR

Variety of microsensors fabricated in standard industrial CMOS technology demonstrated their use as transducers of non-electrical quantities into electrical ones.

Sensors are very sensitive devices and any disturbance in the chain from sensor to the scanner can destroy the primary data.

In Fig. 1 there is situation when sensor is fabricated on extra silicon die and contacted with CMOS IC creating hybrid IC. But since both objects, sensor and CMOS IC, are fabricated on silicon, this makes it possible to create sensor on the same CMOS chip with one or two additional processing steps. Now smart sensor has been generated.

3 PRE-PROCESSING

Pre-processing is necessary in those cases when output signal from the sensor should be adapted to the input requirements of the following element. For instance those can be differential-to-single output conversion, signal amplification, voltage or current DC shift, modulation and/or voltage-to-current conversion.

Regarding to the proposed solution it is the sample-and-hold circuit with additional properties of anti-aliasing features providing filtering aliasing frequencies out of the bandpass limited by the half of the sampling frequency of the following A/D converter.

On the other hand, sensors are mostly low-frequency circuits and no high-order filter is needed in the case when the A/D conversion is done at several-order higher frequencies.

4 A/D CONVERTER

For the use in this kind of the application, oversampled ΣΔ A/D converters, flash A/D converters or algorithmic A/D converters belong among the most common used A/D converters.

Fig. 2 shows chosen solution of Redundant-Sign-Digit (RSD) (by Sweeny-Robertson-Tocher) cycling-conversion switched-current algorithmic A/D converter, which was modified from our design of pipeline A/D converter.

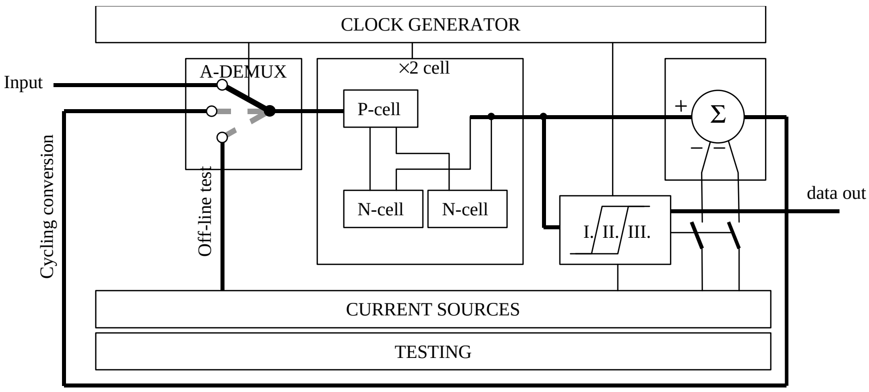

Figure 2. Schematic diagram of an algorithmic switched-current A/D converter

This modification decreased the area of the chip (Fig. 3) by the factor of *N* where *N* is the number of bits at the output of an A/D converter and therefore lowers the cost to a minimum.

One of another advantages of the RSD realization (compared to Conventional-Restoring algorithm, also called successive approximation) is that it sets minimum requirements on the comparators.

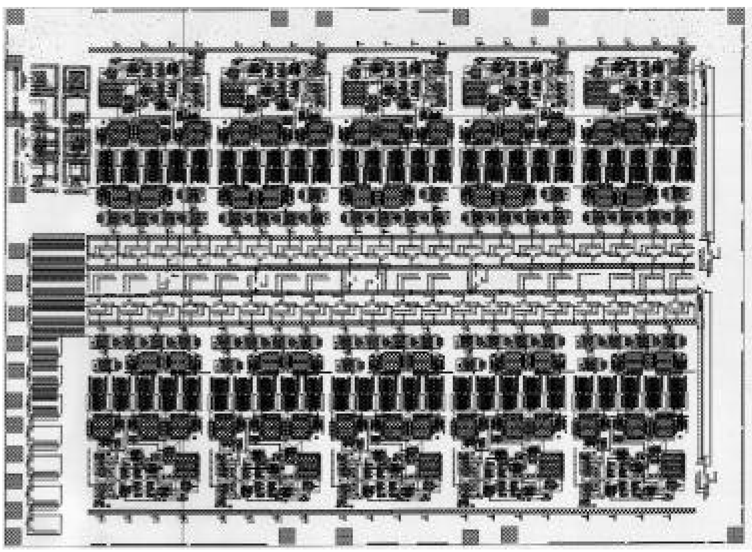

Figure 3. Decrease in area of the cycling conversion structure of the A/D converter (black-white border) compared to pipelined one

Input signal is passed into the multiply-by-two cell each N^{th} period while during the next of *(N-1)* periods the result of the subtraction is acting as the input.

After amplifying of the signal by two the result is compared with two non-critical levels splitting the operational region into three parts (called I., II., III. in Fig. 2). The advantage of such comparison is evident from Fig. 3. If the signal is close to the reference level, then it can be sorted wrongly upon the condition that the comparator levels have an offset. Then the wrong subtraction is proceeded and the signal gets out of the region.

The output from comparators gives also three values, ‘0’, ‘1’, ‘2’ those act as digitized data. A/D conversion is done from the most significant bit (MSB) to LSB while in principle the conversion can be done so long until the resolution of all operations in one cycle does not exceed 1/2 LSB.

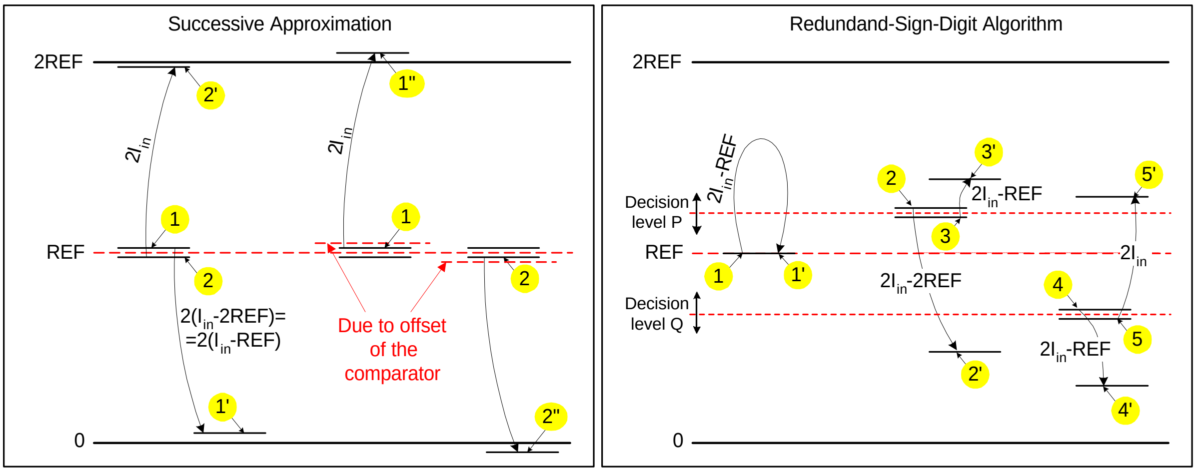

Figure 4. Principle of the restoring digital data different algorithms and the influence of the offset of the comparator

5 ASI BUS SYSTEM IMPLEMENTATION

The ASI Actuator Sensor Interface [1] forms a total way for distributed system, which is based upon bus solutions, allowing free exchange of digital or digitised information between various devices. Block diagram of an intelligent (smart) sensor system with built-in ASI bus features is shown in Fig. 5.

The ASI is applied mainly at the lowest level of a multilevel automation hierarchy. In contrast to the ongoing fieldbus standardisation, ASI concentrates on the typical requirements for connecting binary elements with a controlling device. ASI can be used as an interface integrated into an actuator, sensor, or other device and element itself, opening an option for smart (intelligent) ones. In applications that require smart actuator or sensor or other devices and elements, ASI is intended to the IC into the same possibly small housing of the actuator, sensor or element.

The ASI system is a master-slave communication system composed of a single master and up to 31 slaves. The master sends data and parameter to a specific slave. The slave passes the data to the output ports or processes the requested procedure and returns the input data or the result of the successful processed procedure to the master, respectively. Without additional external wiring the 4 bits of data exchanged cyclically can be used together with 4 bit parameter data which may be transferred to a slave acyclically. Thus, intelligent actuators, sensors or other elements may be built to realise additional features without extra costs for the communication between the master and the slaves, since the expense for the communication is constant.

Various messages can be exchanged between the master and the slaves:

- data exchange - serves for delivery and/or receiving the bit pattern to/from the data output/input of the slave
- write parameter - the bit pattern for the parameter output ports shall be transmitted to a specific slave with the write parameter
- address assignment - serves for setting of an address 0..31 of the slave with a zero address; zero address is a default address of a slave, set prior to commissioning
- commands - for requesting different functions of the slave to be processed, also a slave without an operating address can be identified and its configuration may be read.

The messages sent by the master and received by the slave are composed of six elements: start bit, control bit, address, information, parity and end bit. Similarly, ASI frame for the slave response consists of four encoded elements: start bit, information bits, parity bit and end bit. This is a universal structure applied for all slave responses modes.

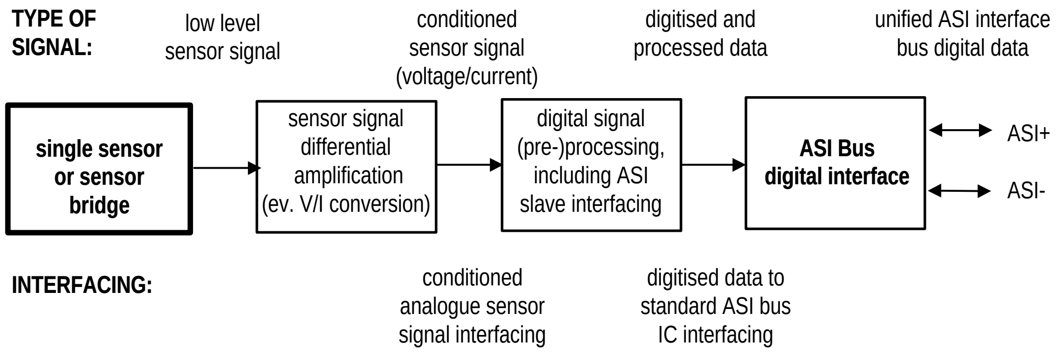

Figure 5. Basic diagram of an intelligent sensor with built-in digital signal processing and ASI bus interfacing

An ASI slave contains four input/output data bits and four parameter bits. The parameter bits are always oriented as output bits. The input/output bits can be redefined. Total 16 different configurations exist. The bits may be configured as input, output, bi-directional or tristate according to the I/O configuration code (I/O code). Identification code (ID code) of the slave is used to distinguish between different slave profiles with the same input/output code. Slave profiles exist for: free profiles, remote I/O ports, two dual-signal sensors, single sensor with extended control, dual actuator with feedback, single actuator with monitoring.

ASI has been designed especially with respect to highly reliable data transfer under heavy industrial noise and interference, all essential parameters of the ASI bus are aimed to this task. The ASI topology is the tree structure. The ASI industrial interface bus is two-wire unshielded bus determined for the binary data link and energy transfer for the operation in small and medium distributed industrial control systems with lengths up to 100 meters (this length is calculated as the sum of all trunk lines).

In technology data systems, the lowest level appears the digital actuator / sensor-to-controller interconnection. This interconnection could correspond to the higher-level SANs (small area networks), which suit complex actuators and sensors. For simple applications with binary elements, however, such SANs appear too expensive. A fitting solution should be competitive with advantages of the analogue 20 mA current loop wiring, it can be reached by ASI bus: cheapness, no need for a power supply at the actuator/sensor, and minimal space requirement. The ASI bus is operated in master-slave mode. Master type controller intermediates data connection (communication) between distributed control system and supervisor level of control, slave subsystem guarantees communication between distributed control system and single actuators and sensors.

6 TESTABILITY

Moreover, smart sensors could be designed with a self-diagnosing capability. Using for instance a conventional 4 to 20 mA analogue signalling a sensor can output only a single parameter - the measurement signal itself in analogue way. The sensor with digital bi-directional fieldbus can output multiple parameters, measurement and diagnostic data can be transmitted separately or together.

This trend further encouraged us to implement ASI bus into our design. Moreover, the ASI bus line can also drive the mode of operation of an A/D converter that was designed as self-testable. This built-in self-test (BIST) recognises between two modes: on-line test and off-line test.

On-line test is based on observing the nodal potentials inside the A/D converter during the normal mode of operation. Analogue window comparator (Fig. 6) checks whether the potential is saturated in the rail or not while when the saturation is observed, it means that the circuit is faulty.

Fig. 7 shows typical response when the fault was detected while the observing is done each third clock cycle when the output is valid.

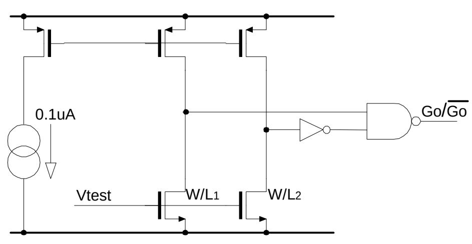

Figure 6. Analogue window comparator

Off-line test passes during test mode when the circuit is not functional.

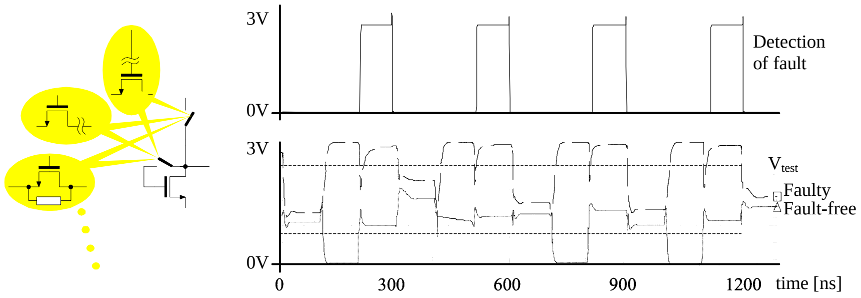

Figure 7. Detection of the faults in on-line test

7 CONCLUSION

The paper deals with the research, analysis and design of up-to-date smart sensor system focused into the ASI system integration. Proposed VLSI and hybrid IC design is operating under 3 V power supply. The system features self-testability and communication through standard ASI bus line thus satisfying criteria of the up-to-date design.

Current praxis requires ability to design any part of the distributed control system located on the ASI bus, especially for sensing the physical quantities, which can be converted or transformed to voltage or current, digitised to the digital domain. The similar task is valid for future control of the actuators. Sensor/actuator development, maintenance and programming for low-level real-time networks take into consideration various application dependent requirements to provide useful actuating and data acquisition tools. The actuator/sensor interconnection level fulfilling ASI standard enabled us to design powerful and not only binary ASI smart and intelligent units for actuating and sensing.

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