XVI IMEKO World Congress
Measurement - Supports Science - Improves Technology - Protects Environment ... and Provides Employment - Now and in the Future
Vienna, AUSTRIA, 2000, September 25-28

ADC HISTOGRAM TEST USING SMALL-AMPLITUDE INPUT WAVES

***F. C. Alegria*[1], *P. Arpaia*[2], *P. Daponte*[3] *and A. C. Serra*[1]**
(1) IT/ DEEC, IST, Universidade Técnica de Lisboa, Portugal
(2) Dip. di Ing. Elettrica, Università di Napoli Federico II, Naples, Italy
(3) Facoltà di Ingegneria, Università del Sannio, Benevento, Italy

Abstract: The experimental investigation on a histogram test for analog-to-digital converters (ADCs) using as stimulus signals small-amplitude triangular waves superimposed to variable DC levels is presented. The test allows inexpensive triangular generators to be used and a dramatic reduction of the duration of the static test for the characterisation of high-resolution ADCs. The experimental comparison of the investigated test with a fullscale wave-based test and with the standard static test for different ADC architectures highlights its effectiveness.
Keywords: ADC testing, Histogram Method, Triangular Wave.

1 INTRODUCTION

In ADC characterisation, the actual transfer characteristic is obtained by time-consuming statistical tests. In static conditions, this is mainly due to the settling time of the DC calibrator and to the requirement of an enormous amount of samples due to the need for a large multiple of the transition level number. In dynamic conditions, the histogram method, also referred as "code density test" [1]-[4], requires the repetitive acquisition of a dynamic stimulus signal with a known amplitude probability density function (pdf).

Conceptually the histogram test needs fewer samples than the standard static test. For each transition level, the standard static procedure [4] only uses the last two sample sets to compute the level value, discarding the previously acquired sets. Moreover, though the histogram requires a test stimulus with a uniform pdf (such as a linear ramp) in order to stimulate uniformly the ADC range as a whole, the practical difficulty of achieving economically highly linear fullscale generators [1] leads to the extensive use of sinusoidal stimulus [3], [4]. The sine wave nonuniform pdf creates the problem that the same INL error has a different impact on ADC performance according to its location on the transfer characteristic [5]-[6].

In this paper, a static test based on a histogram algorithm requiring a smaller sample number and a less-linear ramp generator is discussed. The linearity constraint is relaxed by exploiting triangular stimulus signals ranging only a small fraction of the ADC fullscale, superimposed to several DC levels. The small ADC range swept by the stimulus signal, together with a reduced slope, gives rise to static test conditions. In Section 2, the test procedure is described. In Section 3 and 4, results of the experimental comparison of the presented test with the IEEE 1057-94 standard static test [4], and with the traditional fullscale triangular wave test, respectively, are reported.

2 DESCRIPTION OF THE METHOD

The presented method applied in static conditions exploits three basic ideas (Figure 1): (i) adopt a histogram procedure, in order to reduce the sample number in comparison to the standard IEEE 1057-94 [4]; (ii) use a linear stimulus signal, in order to have a uniform stimulus over the ADC range overcoming the drawbacks highlighted by [5]-[6]; and (iii) employ small-amplitude waves of very slow slope, in order to approximate as much static conditions as possible.

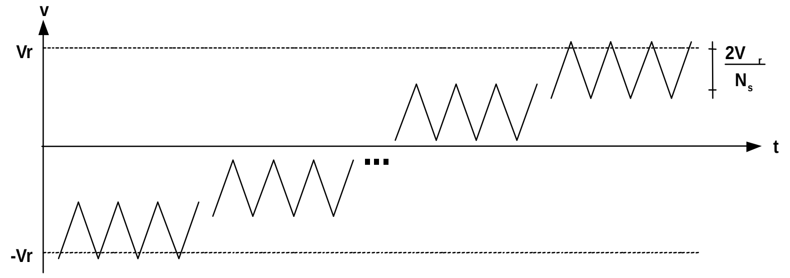


Figure 1 The stimulus signal applied to the ADC.

In particular, the procedure requires N_s steps; in each step, a small number of ADC codes are stimulated repetitively via small triangular waves. The shape of the stimulus signal is always the same in every step, but the DC level is changed step by step.

If $-V_r$ and V_r are the voltages of the first and the last transition level, respectively, the DC offset (C_i) of the stimulus signal used in the i-th step is:

$$C_i = -V_r + \frac{V_r}{N_s} + 2 \cdot i \cdot \frac{V_r}{N_s} \quad , \quad i = 0, \ldots, N_s - 1 \tag{1}$$

and the amplitude A of the stimulus signal is:

$$A = \frac{V_r}{N_s} \cdot (1 + \alpha), \tag{2}$$

where α is the percentage overdrive. Analogously as in the traditional histogram test, the ADC is overdriven in order to stimulate all the codes and to exclude the samples corrupted by noise in the extremities of the stimulus signal. In case of a triangular stimulus signal, the samples in the extremity have to be excluded also to avoid distortions due to the discontinuity in the signal derivative.

For all the codes stimulated by each of the small triangular waves, the DNL is calculated according to the histogram test procedure. Because the waves overlap, there are codes that are stimulated with two waves and for which there are two values of DNL computed. The adopted criterion was to split in half the overlapping region and use for those codes only one of the DNL values calculated. This way the values obtained near the extremities of the triangular waves are not used. Averaging both values obtained is not a good option because using samples near the extremities of the stimulus signal should be avoided for the reason presented earlier.

The transition levels are estimated from the obtained frequencies of code occurrence according to the traditional histogram procedure. The gain and the offset errors are corrected, and the DNL and the INL vectors are computed.

The use of small triangular wave gives rise to practically static test conditions, owing to the small slopes values and to the modest amount of the stimulated region of the input range.

The traditional test of a N-bit ADC requires a ramp input signal with a linearity better than $1/(2^N-1)$ of the fullscale for a 1LSB maximum error. For the presented test with N_s steps, the required linearity is $N_s/(2^N-1)$. The more are the used steps, the less severe are the requirements of linearity. This allows lower-cost triangular generators to be used.

3 EXPERIMENTAL RESULTS USING THE STANDARD STATIC TEST

The presented test was compared with the static test performed according to the IEEE 1057-1994 standard [4]. A FLUKE 5700A Calibrator with an uncertainty better than 8ppm+1.2μV was used. After terminal-based gain and offset error correction, the static INL and DNL were computed.

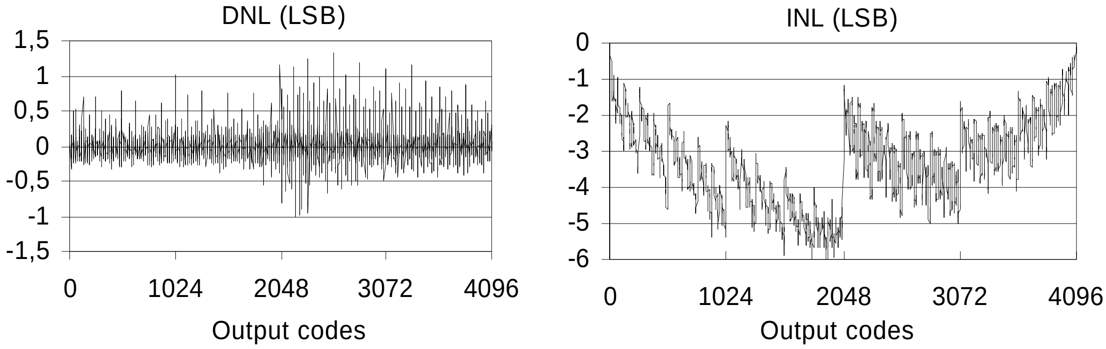
Two different acquisition architectures were investigated: a VXI waveform analyser (Tektronix VX4240), and a PC data acquisition board (Keithley DAS1600).

The waveform analyser is based on a Burr-Brown 12-bit ADC mod.603JH. The input frequency ranges from DC to 5MHz. It has 8 differential or single-ended ranges (from ±0.5 to ±100V) and a sampling frequency from 0.005sample/s to 10Msample/s. This waveform analyser was tested in the 2V range, single-ended mode, with a sampling frequency of 10Msample/s. In this range the ideal code bin width (Q) is equal to 976.8μV (1LSB).

The data acquisition board is based on a 12-bit successive approximation ADC from Burr-Brown (ADS774). It has 8 differential or 16 single-ended inputs. 4 bipolar or unipolar input ranges are available: 10V, 1V, 100mV, and 20mV. The maximum sampling frequency is 100ksample/s. The ADC was tested in the range ±1V at its maximum sampling frequency. In this range, the ideal code bin width is equal to 488μV.

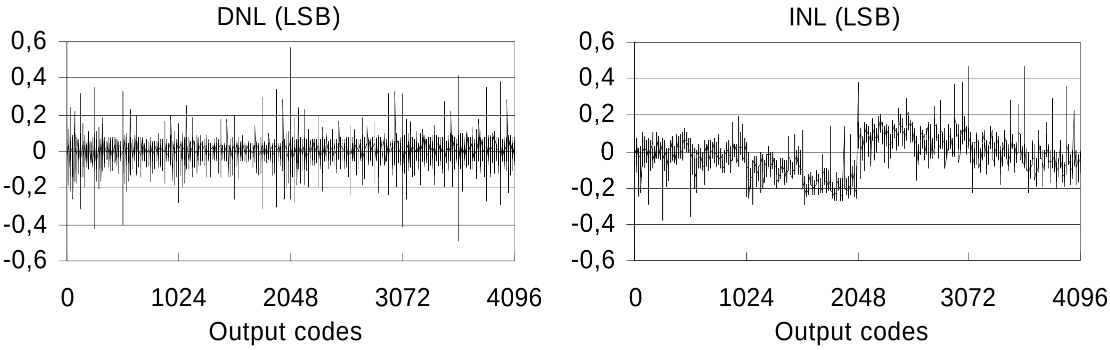
Results of the experiments on the VXI waveform analyser are presented in Figure 2. The accuracy of the estimates of the code transition levels was 0.24mV (12% of the rms noise level), since 1024 samples were acquired after each change on the DC level at the ADC input [4]. This value corresponds to 0.25LSB. A value of 2mV (2LSB) was estimated for the rms noise level of the converter and the calibrator, using the method described in section 4.5.5 of [4]. The DNL worst case is 1.3LSB and the INL worst case is 6.0LSB, as shown in Figure 2.

Figure 3 presents the result of the test for the PC data acquisition board. The rms noise level of the converter combined with the rms noise level of the generator was estimated to be 0.1mV (0.2LSB) by using the standard method described in [4]. The acquisition of records with 4096 samples assures an accuracy of 0.012LSB (6% of the rms noise level).



a) b)

Figure 2 Results of the IEEE 1057-94 standard static test performed on the 2V input range of the Tektronix waveform analyser: a) DNL; b) INL.



a) b)

Figure 3 Results of the IEEE 1057-94 standard static test performed on the 1V range of the Keithley data acquisition board: a) DNL; b) INL.

4 EXPERIMENTAL RESULTS USING TRIANGULAR WAVES STIMULUS

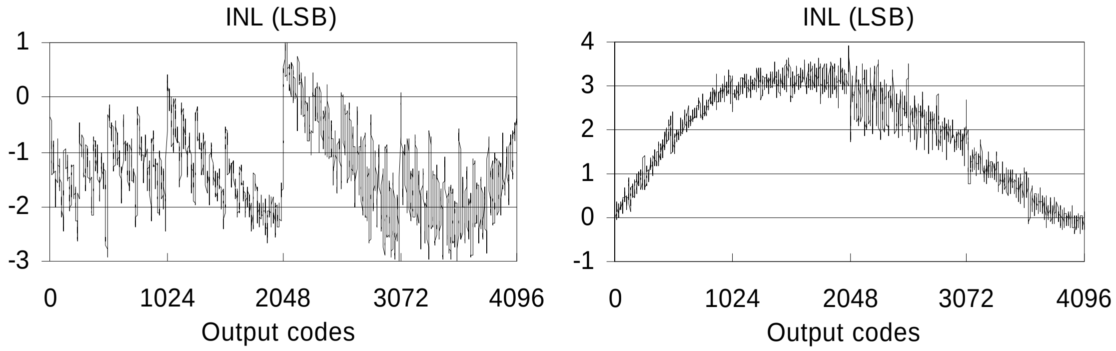
The presented test was compared also to a traditional histogram test using a fullscale triangular waveform in order to highlight the relaxation of the linearity constraints for the generator. The function generator used (Wavetek 9100) has a 25ppm frequency accuracy and 4 digits frequency resolution. For the traditional histogram test of a 12-bit ADC, a linearity better than 1/4095 corresponding to 0.024% of fullscale is required. In this section, a triangular generator with a nonlinearity not better than 0,085% will be shown to be capable of performing the same test if the input range is divided into a convenient number of intervals. In particular, for the same generator: (i) in case of a full-scale triangular voltage, the traditional histogram test will mainly measure the generator nonlinearity; (ii) in case of a decreasing amplitude of the small triangular waves, the presented test will show the influence of the generator nonlinearity disappearing and the ADC INL appearing into the final results.

4.1 HISTOGRAM TEST WITH A FULL-SCALE TRIANGULAR WAVE

For the VXI waveform analyser, a fullscale triangular wave with a frequency of 998.0Hz and an amplitude of 2.04V was used. For this amplitude, the function generator has an accuracy of 3.46mV (0.15% of output + 400μV). Ten records, each one of 200399 samples, were acquired. Consequently, the expected INL values are affected by an uncertainty lower than 0.13LSB.

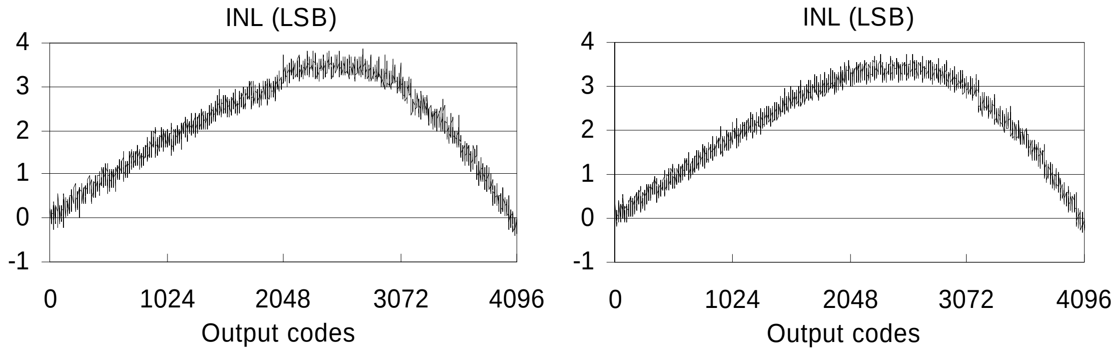
Figure 4a shows the measured INL, and Figure 4b highlights its difference with the INL obtained with the standard static test of Figure 2b. The two INL are comparable because in the histogram the input signal slope of $4 \times 2.04 \times 998.0$ V/s is quite low and should correspond to quite static test conditions for a 10Msample/s digitiser. From Figure 4b a nonlinearity of just 0,085% (3.5/4095) can be argued, analogous to the one of the triangular wave generator. The obtained curve, apart from the test uncertainty and the analyser INL, seems to be mainly due to the nonlinearity of the triangular wave generator.

This is further confirmed by the results of the experiments on the PC data acquisition board. A fullscale triangular wave of amplitude 1.1V and frequency 10.00Hz was used. The input signal slope is 4×1.1×10.00 V/s, thus also these test conditions should be considered as quite static for an acquisition board of 100ksample/s. Thirty records of 999,999 samples each one were acquired to have an uncertainty of the expected INL lower than 0.01LSB. The obtained INL results presented in Figure 5. are very different from the results of the static test (Figure 3b). The difference is highlighted in Figure 5b, where an INL trend analogous to Figure 4b, and thus corresponding again to the nonlinearity of the triangular wave generator, can be identified.



a) b)

Figure 4 Results of the traditional histogram test of the Tektronix waveform analyser with a full-scale triangular wave: a) INL; b) INL difference for the static test.



a) b)

Figure 5 Results of the histogram test of the Keithley data acquisition board with a full-scale triangular wave: a) INL; b) INL difference for the static test.

4.2 TEST WITH SMALL AMPLITUDE WAVES

For the experimental investigation of the presented method, the necessary DC levels and triangular waves were generated with the same calibrator and generator used in the fullscale triangular wave and in the standard static tests, respectively. The investigation was carried out by progressively decreasing the amplitudes of the test waves in order to highlight the relaxation of the linearity constraints on the presented test.

In the case of the waveform analyser, a first experiment by using only two triangular waves, each one with the same frequency of 998.0Hz, the same amplitude 1.05V, but opposite offsets of –1V and +1V, respectively, was carried out. In this way, each wave stimulated half ADC range. The guaranteed minimum amplitude of the stimulus signal is 1.048V: the signal amplitude 1.05V, minus the amplitude accuracy 1.975mV (0.15% of output + 400μV), minus the offset accuracy of 9.2μV (8ppm of 1V plus 1.2μV). The overdrive is then equal to 48.2mV (1.048V – 0.999755V). The resulting input signal slope of 4×1.05×998.0 V/s can be again considered as corresponding to static test conditions. 100 records of 10019 samples were acquired for each wave applied to the waveform analyser. A histogram was computed for each of the waves. The expected INL values have an uncertainty lower than 0.13LSB. The obtained INL, calculated for all codes stimulated by each of the two waves, is reported in Figure 6.

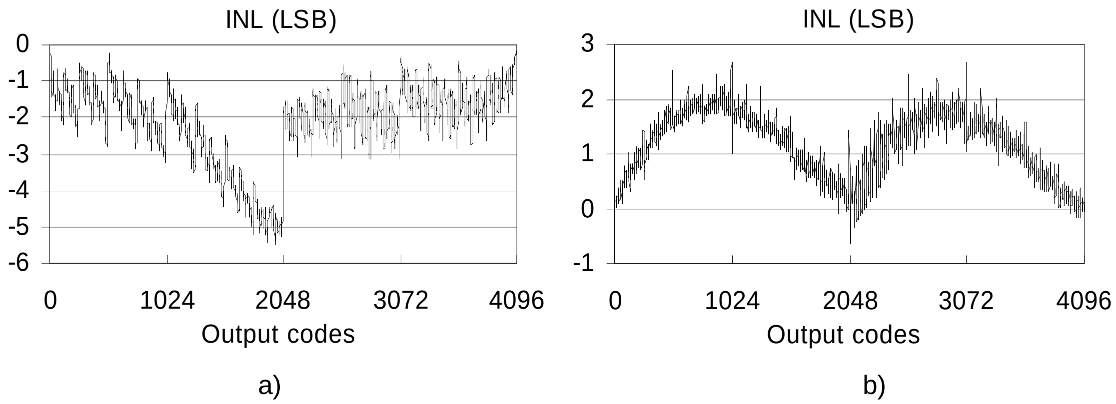


Figure 6 Results from the small amplitude waves test of the Tektronix waveform analyser with 2 triangular waves: a) INL; b) INL difference from the static test.

The difference with the static test results, reported in Figure 6b, highlights again the generator nonlinearity, but now split in two parts, one in each half of the ADC range. The peak has now a value of approximately 1.75 LSB, while in the test with one triangular fullscale wave it reached 3.5LSB. The effect of the nonlinearity of the generator is decreased by half according to the generated amplitude of the stimulus signal.

In Figure 7, results of the test performed with 10 triangular waves, each with amplitude of 220mV and frequency of 998.0Hz is reported. Ten records of 50099 samples were acquired. It can be seen that the effect of the nonlinearity of the calibrator is further reduced, this time approximately by a factor of 10. An analogous pattern of the INL difference between the static test and the low frequency sinusoid histogram test (not presented here due to lack of space) is appearing.

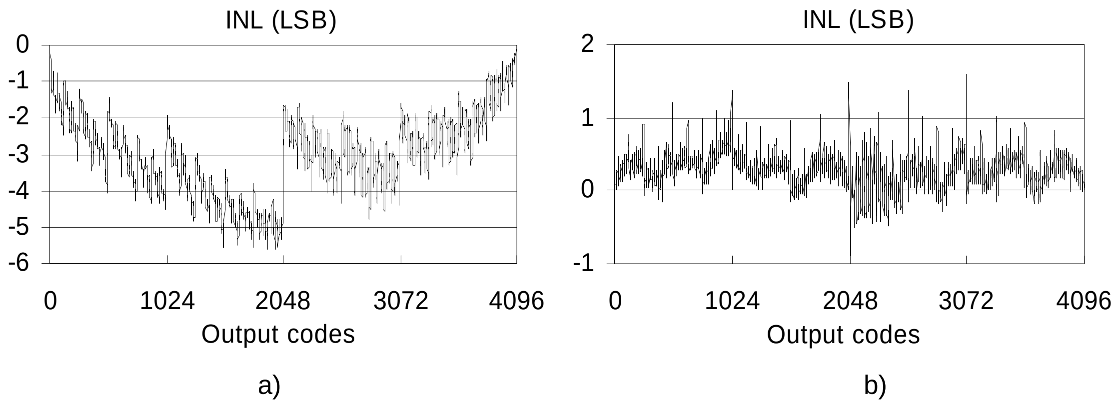


Figure 7 Results of the small amplitude waves test of the Tektronix waveform analyser with 10 triangular waves: a) INL; b) INL difference from the static test.

It becomes clear that the use of several small amplitude waves allows the triangular waves to be employed as stimulus signal, because the effect of its nonlinearity is substantially decreased.

For the experimental conditions of section 3, the duration of the static test is 7 hours. This small amplitude waves test is carried out in approximately 11 minutes, corresponding to a significant reduction of the testing time.

In the case of the PC data acquisition board, analogous investigations were carried in order to validate the presented method for a different type of acquisition system and ADC architecture. The example of Figure 8 highlights the results obtained with 80 triangular waves, each one with an amplitude of 60mV and a frequency of 998.0Hz. The differential input of the board was used to add the triangular waves to the DC offset generated by the calibrator. Three records of 99999 samples each one were acquired (23,999,760 total samples) leading to an uncertainty, in the expected INL, lower than 0.01LSB.

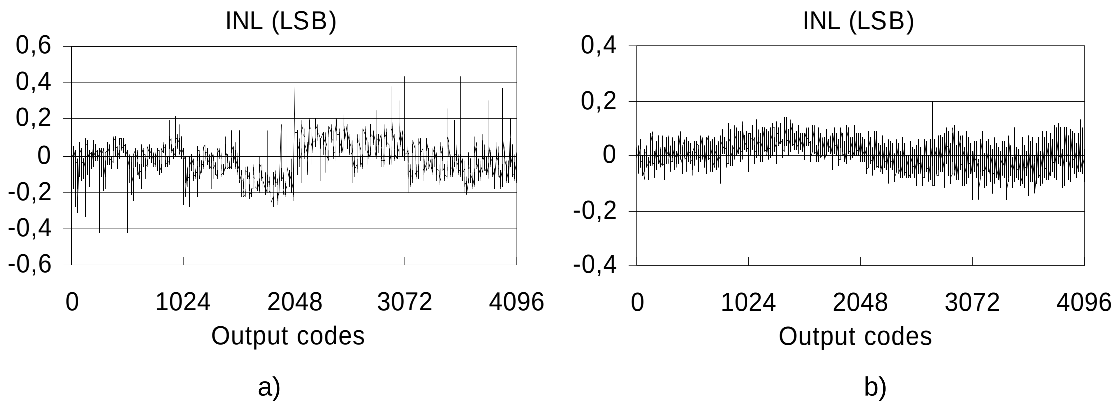


Figure 8 Results of the small amplitude waves test of the Keithley data acquisition board with 80 triangular waves: a) INL; b) INL difference from the static test.

Figure 8b shows how the effect of the triangular wave nonlinearity was greatly reduced. These results are approximately the same obtained with the traditional histogram test with a low-frequency sinusoidal stimulus for this board. Again a significant reduction of the testing time in relation to the static test was achieved. The static test took approximately 6 hours and the test with the method proposed took 5 minutes.

5 CONCLUSIONS

Experimental results of an ADC testing method, based on the histogram test using small amplitude triangular waves with a variable DC level of the stimulus signal, were presented. They show the validity of the method at low frequencies and its potential to substitute traditional ones. In particular, a quasi-static test can be performed (a) in a very small fraction of the time consummation required by the standard method in [4], (b) with a linear ramp generator avoiding drawbacks highlighted in [5]-[6], and (c) with inexpensive generators even for high-resolution ADCs.

The main drawback of this test arises from the acquisition of a small number of samples per period when input signal frequency approaches the sampling frequency.

REFERENCES

[1] Joey Doernberg, Hae-Seung Lee and David A. Hodges, “Full-speed testing of A/D converters”, IEEE Journal of Solid-State Circuits, vol. SC-19(6), pp. 820-827, December 1984.

[2] Linus Michaeli, “The fast method for correction of systematic errors of ADC histogram measurements”, X IMEKO World Congress, vol. 5, pp.40-47, Prague, September 1986.

[3] Linus Michaeli, “Fast dynamic methods of the systematic error autocorrection”, Proc. of 5-th IMEKO TC-4 Int. Symp., pp.247-249, Vienna, April 1992.

[4] IEEE Std. 1057-1994, IEEE standard for digitising waveform records, The Institute of Electrical and Electronics Engineers, Inc., New York, December 1994.

[5] Nicola Giaquinto, Amerigo Trotta, "Fast and accurate ADC testing via an enhanced sine wave fitting algorithm", IEEE Trans on Instrum. and Meas., IM-46, pp. 1020-1024, August 1997.

[6] Diego Bellan, Arnaldo Brandolini, Luca di Rienzo, Alessandro Gandelli, "Improved definition of the effective number of bits in ADC testing", Comp. Stand. & Interf., CSI-19, pp. 231-236, September 1998.

AUTHORS:

(1) Instituto de Telecomunicações / DEEC, IST, Universidade Técnica de Lisboa, Lab. Medidas Eléctricas, 1049-001 Lisboa Codex, Portugal, Phone Int ++351 218418490, Fax Int ++351 218417672, E-mail: falegria@alfa.ist.utl.pt, WWW: http://lx.it.pt/falegria, acserra@alfa.ist.utl.pt, WWW: http://deec.ist.utl.pt.

(2) Dip. di Ing. Elettrica, Università di Napoli Federico II, via Claudio 21, 80125 Naples, Italy, Phone Int ++39 081 7683170, Fax int ++39 081 2396897, E-mail: arpaia@unina.it, WWW: http://remlab.dis.unina.it.

(3) Facoltà di Ingegneria, Università del Sannio, Piazza Roma, 82100 Benevento, Italy. Phone Int ++39 0824 305817, Fax Int ++30 0824 21866, E-mail: daponte@unisannio.it, WWW: http://lesim1.ing.unisannio.it.