Implementation and Application of SOPC-Based Pulse Interpolation Technology

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Abstract: When Pulse interpolation technology emerged and was introduced into flow calibration device, the volume is reduced , furthermore, the calibration time is shorten, so calibration efficiency is improved greatly.However, pluse interpolation technologies is difficult and complex to implement, and in this paper a simple, stable and multi-function method is presented.
Keywords: Pulse Interpolation, SOPC, NIOS II, Flow Meter, Calibrating Device

1. Introduction

At present, most flow meter calibration is using volumetric method. Generally, when using standard device calibrating those flow meters that output pulses, the internal counter can just count the integral pulses which represent the fluid flow, rather than the incomplete pulses, in this case, measurement error is inevitable. Of course, the error can be reduced by collecting more pulses, but need larger calibration equipment, and longer measurement time. When pulse interpolation technology is introduced into flow calibrating device, calibrating the large flow device with small standard device has become actual, measurement time and equipment size are reduced and the accuracy is improved. According to the principle, the paper presents a SOPC-Based method for implementing double-timing method pulse interpolation and verifys the design scheme. This method not only obtain the resolution but reduce the development cycle. Comparing to using SOPC, it's difficult and complex to implement the pulse interpolation technology with general method. The implementation based on SOPC is faster and more stable.

2. Basic principles

There are three methods of pulse interpolation technologies, included Double-timing method, Quadruple-timing method and Phase-locked method. In this paper we used the Double-timing method. Fig.1 is Double-timing method principle.

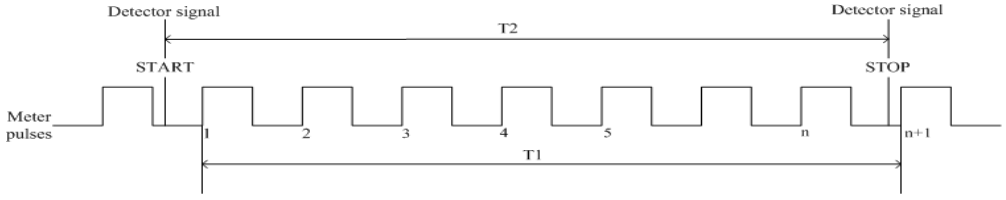

Fig.1 Double-timing method

Where
T1: is the time-interval between the first meter pulse following the first detector signal and the first meter pulse following the last detector signal;
T2: is the time-interval between the first and last detector signal;
n: is the total number of complete meter pulse.
The interpolated number of pulse is then given by

$$n' = n\frac{T_2}{T_1}$$

To obtain a resolution better than 0.01%, the period of the, i.e. the time T2(see Fig.1), shall be at least 20000 times greater than the reference period tc of the clock used to measure the time-intervals.
That is

$$T_2 \geq 20000 \times t_c$$

that is

$$n \cdot \frac{1}{f_m} \geq 20000 \cdot \frac{1}{f_c}$$

therefore

$$n \geq \frac{20000}{f_c} f_m$$

Where
f_m: is the maximum frequency of flow meter pluse(Hz);
f_c: is the reference clock frequency;(HZ);
n: is the minimum number of pulses collected during the calibration.

From Fig.1, we can get the timing sequence of T1 Timer, T2 Timer and n counter enable signal, as shown in Fig.2.

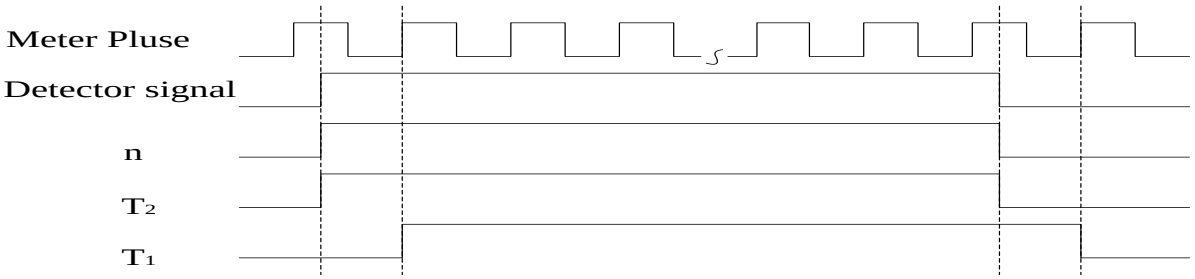

Fig.2 Timing sequence of enable signal

3.System Framework

Fig.3 shows the system framework, the chip used in this scheme is EP2C5T144C8N, Altera Cyclone II FPGA series.

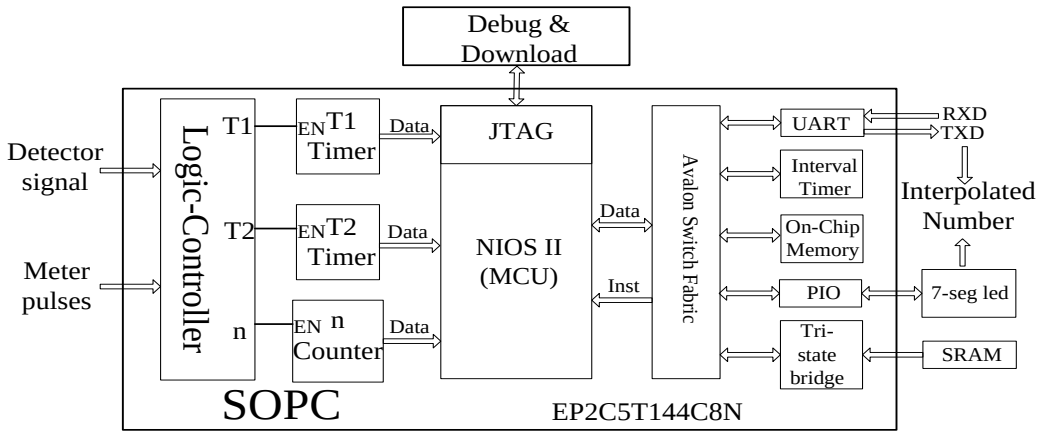

Fig.3 System Framework

In Fig.3, Detector signal is the start and stop signal of calibration. Meter pluses is the output-pluses of flow meter. 7-seg led, SRAM and UART are the peripheral circuits for FPGA.

Logic-Controller module provides the control signals T1, T2 and n in Fig.2. T1 Timer and T2 Timer are timing modules. NIOS II is a embeded CPU which process the data from timing module. Avalon Switch Fabric, Interval Timer, On- chip Memory and Tri-state bridge are necessary modules when NIOS II working.

4. Functional Module

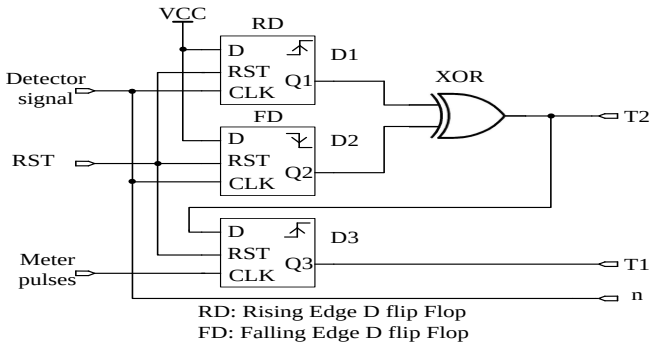

Fig.4 Logic Control Module

Fig.4 is the internal schematic circuit diagram of the Logic-Controller in Fig.2, D_1 and D_3 are positive edge D flip-flop, D_2 is negative edge D flip-flop, VCC is 3.3V, T_2, T_1, n are connected to EN port of T_1 Timer, T_2 Timer, n counter.

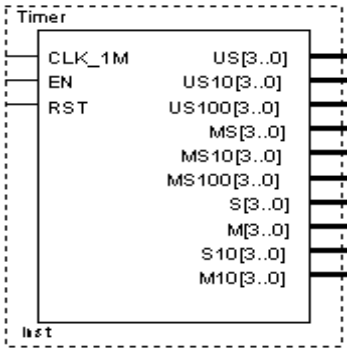

Fig.5 T1/ T2Module

Fig.5 is the internal schematic diagram of the Timer module in Fig.2. The Timer module can time max to 99min 59sec 999ms999us. Reference clock is 1M hz.

5. Simulation

Simulation Environment:
Operating system: Windows XP;
Device: EP2C5T144C8N;
Software: Quartus II 7.2; NIOS II IDE.

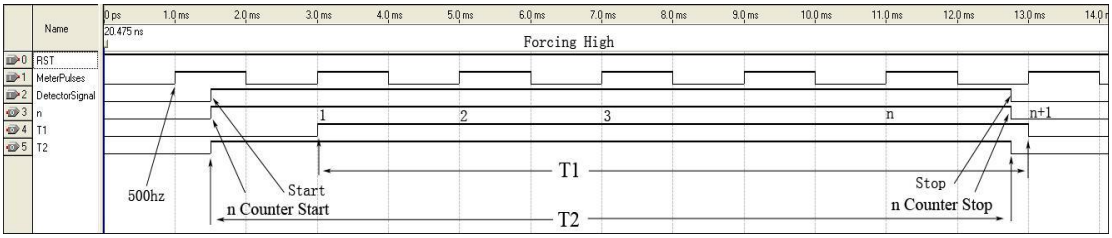

Fig.6 Simulation wave of logic control module

Fig.6 is the simulation waveforms. Here DS(Detector signal)is set to 11.25ms, virtual flow-meter pulse frequency is 500hz. , Contrast Fig.2 and Fig.6 , it can be seen that the waveform timing is correct. For the high FPGA clock frequency(50M hz), the signal transmission delay is far less than the system required response time(<1uS), the response time is almost 0, in summary, the enable signals generated by Logc-Controller can be used to control the timer and counter.

6. Experiment

Experimental platform:

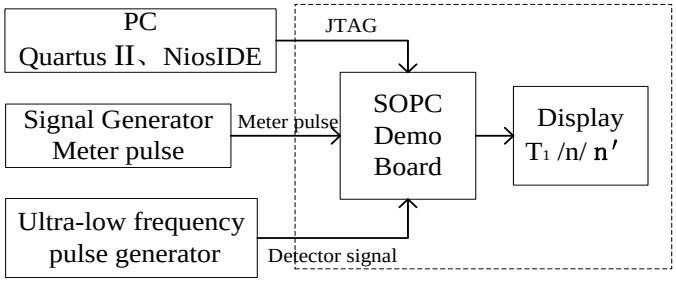

Fig.7Experimental platform

Table. 1 measurement result

DS	T_1	T_2	n	n′
10s	10043233	10042091	4911	4910.44
30s	30010994	30011401	15103	15103.20
60s	59887964	59890617	29486	29487.30
90s	89985408	89984207	42203	42202.44

Where

DS: Detector signal, Meter pulse frequency is 100hz.

According to the principle of Double-timing method pulse interpolation technology, as shown in Fig.1 and Fig.2, it can be seen that

1. the value of $|T_2-T_1|$ should be less than 2 times pulse period;
2. The value of T_1 is close to T_2, and equals to DS roughly;
3. n is close to DS * pulse frequency, and the value of | n-n'| should be less than 2.

By calculating the experimental data of above table, experimental data meet the three conditions. So, the above analysis, software simulation and experimental results, show that the proposed design is correct and feasible.

7. Conclusion

Through software simulation and experimental test, we can get the conclusion that the scheme proposed in this paper of SOPC-Based pulse interpolation technology is correct and can be physically realized. Compared to traditional implementation methods, this scheme not only

retain the full functionality of the old method, but has its own characteristics, such as longer calibration time, lower cost, easier to implementation and more stable, therefore the scheme proposed in this paper can be available for practical application.

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