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METHOD OF DIGITAL CIRCUITS NOISE IMMUNITY MEASUREMENT USING A STANDARD NOISE SIGNAL

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Abstract – Noise sources in digital circuits and a general method of noise susceptibility measurement were described. The new method of dynamic noise immunity measurement for digital circuits using a wideband white noise generator with possibility of noise bandwidth reduction has been presented. The simulation models were prepared in COMSIS environment both for wideband and narrowband stimuli (Gaussian white noise signals). The experimental results of investigations confirming the effectiveness of the proposed method have been reported and discussed.

Keywords: digital circuits, dynamic noise immunity, noise.

1. INTRODUCTION

Noise has become as important a metric as timing or power in the design of digital integrated circuits (ICs). Unwanted spurious signals commonly having pulse shape are conducted into the logic devices by transmission, supplying and grounding lines. They can cause the changes in logic states of the devices and faulty working of whole digital systems. Noise immunity can be generally defined as the tolerable signal to noise ratio needed to achieve a desired level of device performance. The low and high states noise margins are measures of the extent to which a logic circuit can tolerate noise or unwanted spurious signals and strictly depend on input and output voltage (current) characteristics of digital circuits.

Therefore noise can have the following effects:

- data loss (or metastability) in latches and flip-flops or other storage circuits,
- speed degradation leading to setup time violations (or speed increase leading to hold time violation) due to the Miller effect,
- additional power dissipation due to propagation glitches,
- misfiring of sensitive circuits toa state from which a recovery is not possible.

Unwanted changes or delay of switching processes (or their blocking) are caused by noise pulses with a given amplitude and a duration longer than acceptable or by noise pulses with a higher amplitude than permissible for a given duration. The effectiveness of interfering signals is determined by their energy used for discharge of circuit and load capacitances and for state changes of switched transistors depended on logic circuit technology.

The energy required per logical operation which can be considered as an intrinsic figure of merit has been recently dramatically reduced. The minimum energy per logical operation w_m is proportional to the mean intrinsic time for execution of a logical operation t_{av} and to the mean power P_{av} delivered by supply over the time interval t_{av}

$$w_m = P_{av} t_{av} \quad . \tag{1}$$

The measurement of dynamic noise immunity as a measure of the extent to which a logic circuit can tolerate noise is still very important due to smaller and smaller noise margins on transfer characteristics of logic circuits.

2. NOISE SOURCES IN DIGITAL CIRCUITS

Noise in digital circuits can come from many different on-chip sources. For the purposes of these considerations based on noise to real semiconductor devices, eg. MOS, the following general noise sources should be taken into account:

- thermal noise of all resistances in circuits (the noise within the channel and all interconnections containing resistances),
- noise effects of switches and other elements (1/f noise of the charge carriers in the surface states of the channel and shot and generation-recombination noise),
- substrate coupled-noise,
- noise deriving from internal and external crosstalk.

The most damaging noise sources are crosstalk between adjacent switching wires, charge redistribution in static and dynamic logic gates and power supply fluctuations. All these noise sources can interact to destabilize stored logic values. Low switching noise (current spikes) is obtained by keeping the supply current as constant as possible (eg. by drawing the current from the power supply through current sources – current sreering logic CSL). The scaling of transistor sizes contributes to an increase in the capacitive coupling coefficient of a given wire and in consequences to much larger noise voltages being induced in deep sub-micron designs.

Apparently, due to package parasitics, noise at the supply lines can be the major contributor to substrate-coupled

disturbances. Supply lines interact with the substrate mainly through the substrate contacts. A digital switching device induces currents to the substrate through the depletion capacitances of junctions. The amount of noise injected is larger the larger the device and the faster the transients.

Noise transmitted to the device by output terminals are commonly current pulses or transient waveforms. Noise injected by supply lines are usually voltage pulses with opposite polarity than biasing voltage and comparable amplitude.

3. NOISE IMMUNITY MEASUREMENT

Noise immunity on disturbances conducted by the transmission line is measured in the frequency range to some hundreds of MHz (Fig. 1). The transmission device embodies the properties of interconnections between the two digital circuits in a logic chain and those of the output of the transmitting and of the input of the receiving circuit. In the bulk current injection the current injection probe is an ordinary current transformer; in the voltage injection the capacitance coupling is used [1].

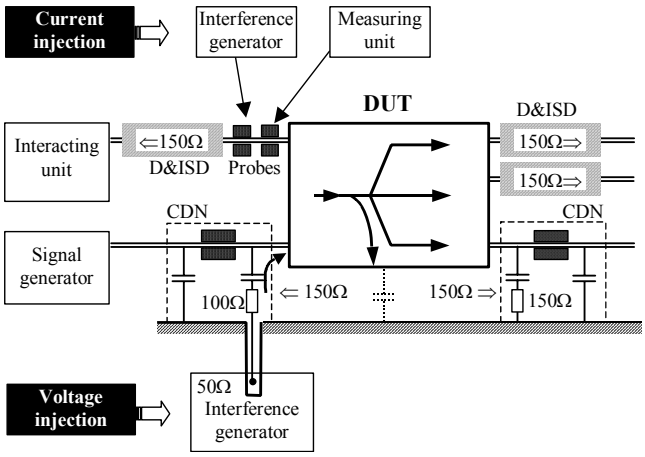

Fig. 1. Measurement system for devices susceptibility to interference (DUT – device under test, CDN – coupling-decoupling network, D&ISD – decoupling and impedance stabilizing device)

Choosing a stimuli for the noise immunity measurement one should take into consideration a level, shape, duration and also an energy of a signal. The rectangular shape of pulses is the most often used in noise immunity measurements [2]. In the present paper the Gaussian white noise signal application is proposed to determine the dynamic noise immunity of logic circuits.

2. DESCRIPTION OF THE METHOD

Influence of internal and external noise on a logic circuit can be considered as random stimuli. Therefore the application of a Gaussian noise signal with constant power spectral density for noise immunity measurement fulfils the working conditions of real devices [3].The method enables investigations of dynamic noise immunity of logic devices which result in the range of proper voltage levels of Device Under Test (DUT) in a presence of spurious signals with a constant power spectral density. DUT is stimulated by wideband or more narrowband Gaussian white noise (Fig.2). Such a signal can be more adequately referred to real

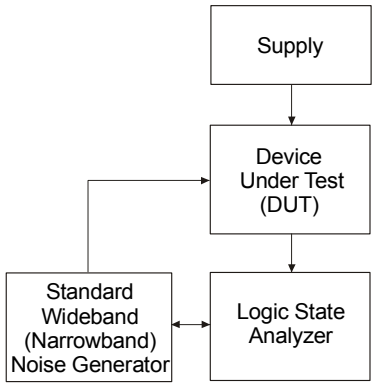

Fig. 2. General block diagram of the set up with standard noise generator for the dynamic noise immunity measurement of digital circuits

disturbances. For the wideband noise stimulus its bandwidth should contain frequencies higher than the threshold frequency of DUT with the lower limit as low as possible. Then the level of noise is increased till the change of the logic state will occur. The noise level corresponding to the logic state change expressed in the power spectral density units can be established as a measure of dynamic noise immunity of DUT. It should be determined in the close relation to the precisely fixed noise bandwidth of the stimulus. For such a measurement a wideband standard noise generator with spectrum containing frequencies higher than the transmission frequencies of DUT have to be used. For very speed logic circuits such generators should have greatly sophisticated structures.

The modification of the method rely on the limitation of noise bandwidth [3]. Now the maximum frequency of given limited noise bandwidth is lower than the threshold frequency of DUT and the noise bandwidth contains the frequency responding to the reciprocal of the propagation time of DUT. The product of given noise bandwidth and noise level expressed in power spectral density units related to a logic state change can be assumed as a measure of dynamic noise immunity of DUT.

The propagation time is referred in the frequency domain to the reciprocal of the DUT's transfer function band and decides on a transmission speed. The stimulus with spectral components having such frequencies enables testing of DUT for the worst case conditions.

3. SIMULATIONS AND MEASUREMENTS

To verify the effectiveness of the method the simulations have been carried out in the environment COMSIS v. 8.6 (IPSIS) software [4]. Two simulation models of DUT have been applied. The model containing a threshold detector and a wideband white noise generator is shown in Fig. 3. Voltage type of DUT was chosen in the model (Fig. 3) with the stimulus as rectangular clock pulses w_r and pseudorandom binary pulses *sbs*. Both these waveforms

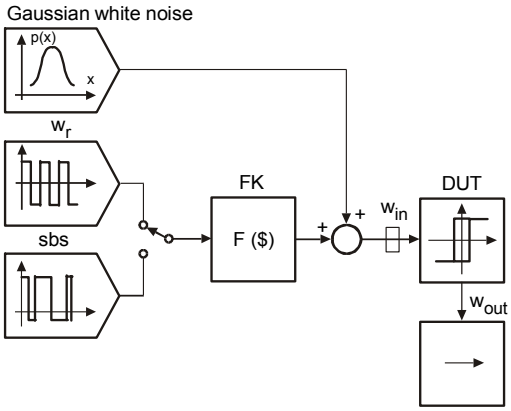

Fig. 3. The block diagram of the simulation model for noise immunity investigation : DUT – Device Under Test, w_r - rectangular waveform, sbs - pseudorandom binary signal, FK – adjustment of the $F(\$)$ function level, w_{in} - input signal ($FK(w_r)$ + Gaussian white noise or $FK(sbs)$ + Gaussian white noise), w_{out} - output signal

were changed into positive polarity pulses (block FK) and added to Gaussian white noise. The level of the noise could be precisely adjusted. Such a signal was introduced into the input terminal w_{in} of the DUT.

The graphical display screen from the COMSIS with the selected results is shown in the Fig. 4 and 5. The upper frequency of the white noise bandwidth was 200 MHz, the relative level of noise 2, 3 and 4 dB, respectively, for the consecutive iterations and the detection levels for the threshold device 0.4 V (logic "0") and 3.3 V (logic "1"). The arrows on the bottom waveform (Fig. 4) indicate the logic state changes caused by the superimposed white noise.

The simulations (Fig. 5) were performed with the following parameters: the bandwidth of white noise signal – 325 MHz (the cut-off frequency of the device equals 318 MHz), the voltage of low logic state PR1 = 0.75 V (during logic state changing from high H to low L), the voltage of high logic state PR1 = 2.1 V (during logic state changing from L to H). According to the producer specification for the DUT SN74LVC06 (Texas Instruments) the low state level L was settled to 0.55 V, the high state H to 2.3 V - both to the input and output terminal of the DUT. The number of processed points of simulation (NOP) was assumed 100 and the time step (TS) equal 0.055 ns.

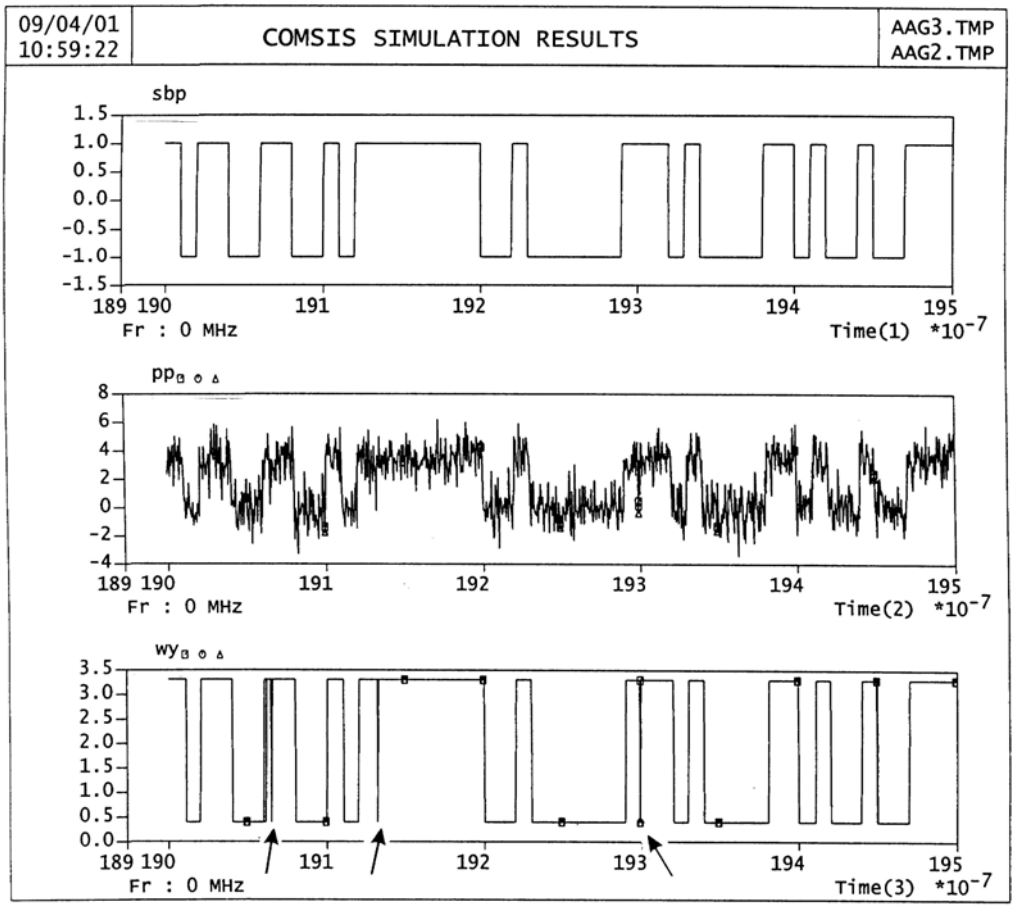

Fig. 4. Selected results of simulation in the COMSIS software

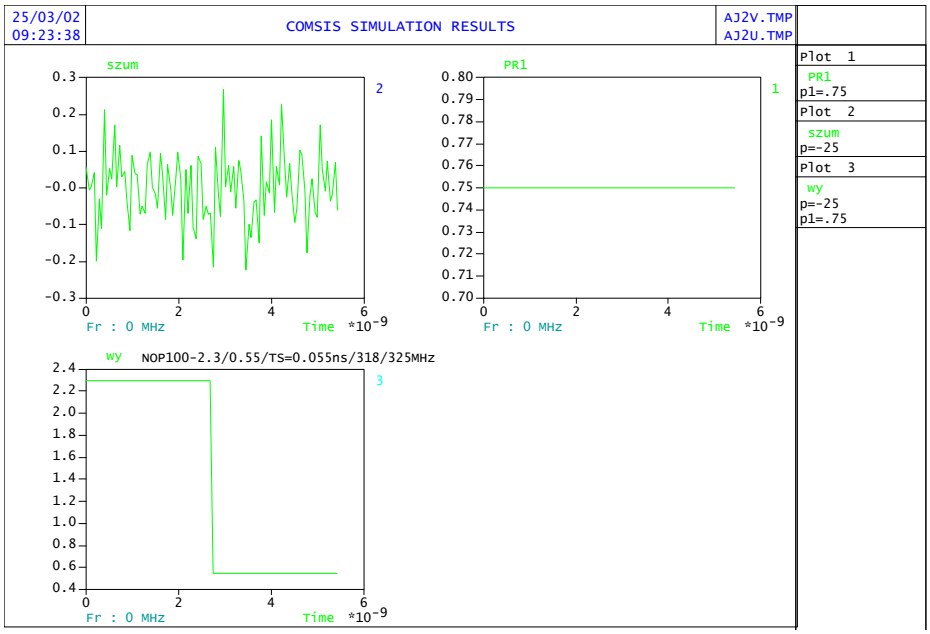

Fig. 5. Simulation results during switching DUT from level H to level L after input stimulation by white noise with the power level –25 dB (PR1 = 0.75 V)

The model shown in Fig. 6 enables verification the modified method of noise immunity measurement for the given noise bandwidth. It includes the appropriate bandpass filter with assumed noise bandwidth of the stimulus, attenuation outside the band and the type of approximation (Bessel, Butterworth, Tchebyschev, Cauer filter).

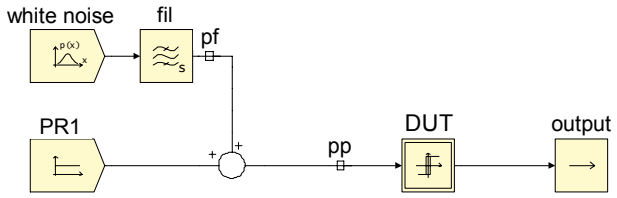

Fig. 6. Block diagram of the simulation model with limited noise bandwidth: fil – bandpass filter, pf – noise signal at the filter output, pp – input signal of DUT (white noise + PR1)

For comparison purposes the simulations for the model in Fig. 6 were carried out also for the device SN74LVC06 having propagation time 3.9 ns (equivalent of the frequency 256.4 MHz) and the cut-off frequency 318 MHz. The highest frequency of the noise bandwidth (filter) was settled on 257 MHz and the lowest frequency was varied. The approximation by the Cauer filter was chosen (maximum slope, high effectiveness both the transmission as the attenuation - from - 0.5 dB to – 40 dB). For the noise bandwidth from 4 to 257 MHz and simulation parameters as in Fig. 5 the noise power level required for switching was equal p = - 9 dB. However, for the much narrower noise bandwidth – from 154 to 257 MHz the DUT was switched by the power power level p = 7 dB and for the bandwidth 244 – 257 MHz p = 35 dB.

The dependence between the level of noise power spectral density needed for logic state switching and the bandwidth of a stimulus signal for slow digital circuits (UCY7400) and more faster CMOS devices is shown in Fig. 7.

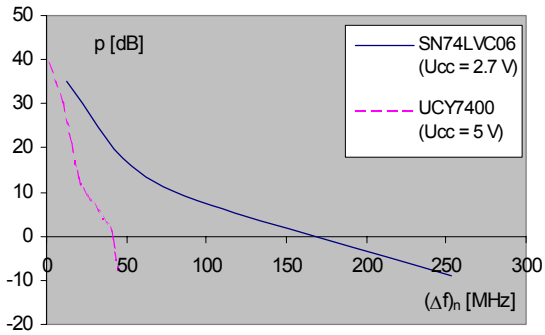

Fig. 7. Level of noise power needed to logic state switching of DUT versus noise bandwidth

The achieved results confirm that the narrower bandwidth of noise stimulus the higher level of noise power is necessary to switch the logic state of DUT. It results from the described mechanism that an appropriate energy (in the experiment an energy of noise stimulus) is needed for a logic state switching. In the case of a wide noise bandwidth the level of noise power spectral density necessary to logic state changing is relatively low.

4. CONCLUSIONS

The experiments confirmed the possibility of dynamic noise immunity measurement for logic circuits according to the assumptions accepted in two patent submissions [3]. The effectiveness of this new method with noise stimulus signal limited to the adequate bandwidth was justified. The further investigations should also inject disturbing noise signal to other termination of ICs.

The possibility of smooth power adjustment of noise stimulus signal enables, especially for CMOS circuits, parametric evaluation of the noise power influence. The simultaneous influence of power supply energy should been also considered in the laboratory measurements. The quantitative relations can be achieved by the detailed modelling of physical and electrical properties of a measured digital circuit

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