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INFLUENCE OF DVM'S INPUT PARAMETERS ON DVM-BASED HIGH-OHM RESISTANCE COMPARISON

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Abstract – Establishment and maintenance of resistance standard traceability is one of the main tasks of Primary Electromagnetic Laboratory (PEL) within the Faculty of Electrical Engineering and Computing of the University of Zagreb. For the purpose of accurate resistance standards comparison a digital voltmeter (DVM) based method has been designed and realized. When measuring resistance standards greater than 10 MΩ capabilities of the method are restricted due to influence of DVM's input parameters: input DVM's resistance, input offset current and input capacitance. Determination of DVM's input parameters and their contribution to the overall high-ohm resistance comparison uncertainty has been presented in this paper. The possibility of use of DVM-based method for gigaohm value resistors comparison has also been investigated.

Keywords: high-ohm resistance comparison, DVM's input parameters.

1. DVM-BASED RESISTANCE COMPARISON METHOD

1.1 General

The group of resistance standards in PEL consists of twelve resistors ranging from 1 mΩ to 100 MΩ. Building high-ohm resistance standard base up to 10 GΩ has provoked the development of new comparison method in high-ohm measurement field, based on modified existing comparison method [1] using two digital voltmeters HP 3458A (in further text DVM). Operational basics of this method for two resistance standards comparison are shown in Fig. 1. R_1 and R_2 are compared resistors connected serially, U is applied voltage, $U_{m1}=U_1(1+p_1)$ and $U_{m2}=U_2(1+p_2)$ are the voltages being measured with two DVMs designated as DV1 and DV2, where p_1 and p_2 are relative errors of the voltmeters 1 and 2 respectively. Determination of the resistance ratio has two steps, indexed as a) and b) in Fig. 1. At position a) the voltage across R_1 and the total voltage of the series are measured with the voltmeters triggered simultaneously (using GET command) via IEEE-488 bus connected to the PC. Next step interchanges resistors position and the voltage measurement is repeated. Now the voltmeter DV1 measures voltage drop across the resistance R_2, and voltmeter DV2 is only controlling permanence of voltage supply. Using symbols given in Fig. 1 the ratio r of the resistances R_1 and R_2 is

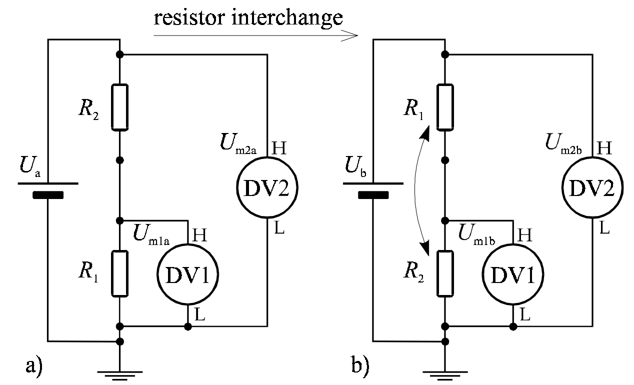

Fig. 1. DVM-based resistance comparison method. Using two voltmeters the effect of current drift during measurement is quite nullified.

expressed as follows:

$$r = \frac{R_1}{R_2} = \frac{U_{m1a}}{U_{m1b}} \cdot \frac{U_{m2b}}{U_{m2a}}, \qquad (1)$$

$$r = \frac{U_{1a}}{U_{1b}} \cdot \frac{U_{2b}}{U_{2a}} \cdot \left(1 + p_{1a} - p_{1b} + p_{2b} - p_{2a}\right), \qquad (2)$$

$$r = r_0 \cdot (1 + \Delta p), \qquad (3)$$

where r_0 is *true value* of ratio of R_1 and R_2, and Δp associated relative error obtained from (2). If the resistances R_1 and R_2 are equal, the relative error Δp depends only on the relative error instability of the voltmeters, since they measure the same voltages in both positions. The instability of the HP 3458A voltmeter's relative error is found to be less than 0,05 µV/V during 1 hour measurement, and thus much affects measurement uncertainty of the 1:1 comparison method. If the nominal resistance ratio is $r = 10$, the relative error of the ratio corresponds to the change of the DV1 relative error when measuring different voltages from its two measuring steps. So produced non-linearity error of the DVM over the measuring range has to be separately measured.

1.2 High-ohm resistance comparison considerations

If compared resistors are greater than 10 kΩ, interconnection wire resistance of few milliohms can be definitely neglected. A special care is taken for interchanging resistors R_1 and R_2 to avoid leakage currents

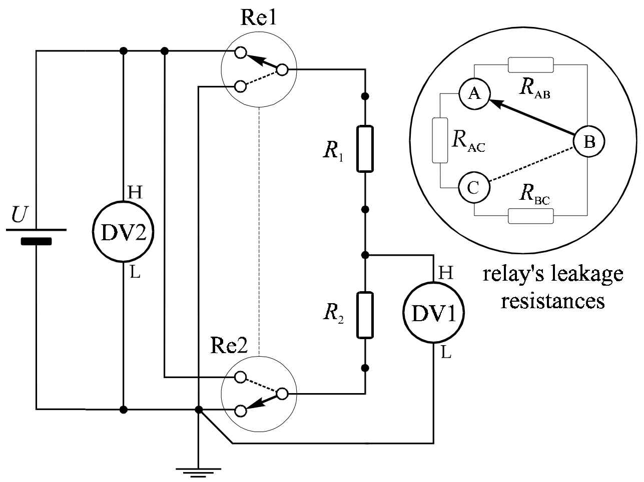

Fig. 2. Realization of resistors interchange in high-ohm resistance comparison method. Leakage resistances between the relay's terminals do not affect measured resistance ratio.

of the relays used. It is evident from Fig. 2 that the relay's leakage resistance R_{AC} acts in parallel with the voltage source, and leakage resistances R_{AB} and R_{BC} are either in parallel with the voltage source or shunted by the relay's contact. Therefore they have no influence on determination of resistance ratio. Interconnection cables among R_1, R_2 and DV1 should be as short as possible and properly shielded and grounded.

2. ANALYSIS OF INFLUENCE OF THE DVM'S INPUT PARAMETERS

2.1 Input resistance of DVM

The resistance comparison method described above using two voltmeters has been designed in PEL for determination of any resistance ratio from 1 to 10, with respect to the largest voltage drop of 10 V across one of the resistors. At 10 V measuring range the HP 3458A voltmeter exhibits very large input resistance, about 10^{12} Ω according to the manufacturer's data and the published papers [2,3,4]. Input resistance R_{V1} of the DV1 is shunting firstly resistance R_1 at position a), and then resistance R_2 at position b), as shown in Fig. 3. Input resistance of DV2 is parallel with the voltage source and will not be taken in consideration. It is assumed that the input resistance R_{V1} varies during measurement, and that compared resistors are stable. Hence, in accordance with positions a) and b) in Fig 3 following expressions could be written:

$$R_{V1a} = R_V, \tag{4}$$

$$R_{V1b} = R_V \cdot (1 + p_{RV}), \tag{5}$$

where p_{RV} is assigned to the relative input resistance change of DV1 between two measurements being taken. In further analysis the voltmeters non-linearity errors will be ignored. Using the symbols from (1) to (5) the ratio r of the resistances R_1 and R_2 is now calculated:

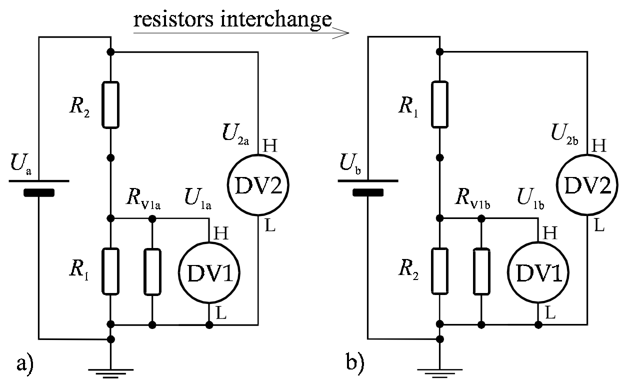

Fig. 3. Position of DV1's input resistance during two-step resistance comparison.

$$r = \frac{R_1}{R_2} = \frac{U_{1a}}{U_{1b}} \cdot \frac{U_{2b}}{U_{2a}} \cdot \left[1 + \frac{p_{RV}}{1 + m \cdot (1 + p_{RV})} \right], \tag{6}$$

where m is substitution for:

$$m = \frac{R_V}{R_1 \| R_2}. \tag{7}$$

Simplifying (6) the final relation is given:

$$r = r_0 \cdot (1 + X), \tag{8}$$

where X represents the relative error of the ratio r due to influence of the DVM's input resistance. Generally, from (6) the following is concluded. If compared resistors are of values greater than the input resistance of the DV1 ($m \le 1$), the relative error X corresponds to the instability of input resistance R_V during measurement process, in view of the fact that comparison of R_1 and R_2 is done intermediately over the smaller "third" resistor, namely R_V. More expected case is when $m >> 1$; then X aims at zero, in other words the influence of input resistance instability p_{RV} on the relative error X is reduced with the factor m (Fig. 4). It is obvious from (6) that when the input resistance of the shunting voltmeter DV1 is constant during measurement (thus $p_{RV} = 0$), the influence of the voltmeter's input resistance is

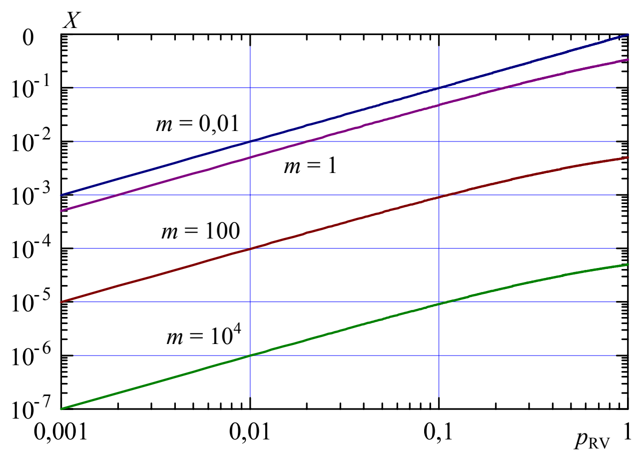

Fig. 4. Relative error X of the resistance ratio due to instability p_{RV} of DV1's input resistance.

completely nullified regardless of its value. Since very large input resistance of digital voltmeter's amplifier between "high" and "low" terminals cannot be considered stable because of internal amplifier leakage current paths and possible temperature drift, input resistance should be estimated by means of value and related instability for the specific measurement period.

2.2 Internal current of DVM

Input amplifier stage of the HP 3458A digital voltmeter shows signs of small current sources on both input terminals, thus producing resultant *input offset* current flow into the measuring circuit, as shown in Fig. 5. Let the DVM's internal current I_S varies during resistance comparison with the relative instability p_{Is}:

$$I_{Sa} = I_S , \tag{9}$$

$$I_{Sb} = I_S \cdot (1 + p_{Is}) . \tag{10}$$

The influence of the input offset current has been analysed with assumption of constant voltage supply and stable DVM's input resistance, and voltmeters non-linearity errors not taken into account. Using (9) and (10), the voltages measured at position a) and b) lead to the new equation for the ratio of the compared resistances:

$$r = r_0 \cdot \left[1 + \frac{I_S}{I_R} \cdot \frac{r_0}{r_0 + 1} \cdot \left(\frac{r_0 - 1}{r_0} + p_{Is} \right) \right], \tag{11}$$

$$r = r_0 \cdot (1 + Y_S) , \tag{12}$$

where r_0 is true value of ratio as quoted in (3) and (8), and I_R substitutes $U/(R_1+R_2)$. It is understandable from (11) that the instability p_{Is} of the voltmeter's input offset current influences the relative error Y_S significantly when the ratio $r = 1$ is measured. In that case the instability p_{Is} is reduced with factor $I_S/2I_R$, where I_R is the current through the series of the measured resistors. If the ratio increases to $r = 10$, the relative error Y_S becomes enlarged as a result of unbalanced impedance of the circuitry "seen" by DVM's internal current source at positions a) and b). The value of the input offset current of the HP 3458A digital voltmeter is stated as $I_S < 20$ pA, and for more accurate high-ohm resistance comparison should be experimentally determined.

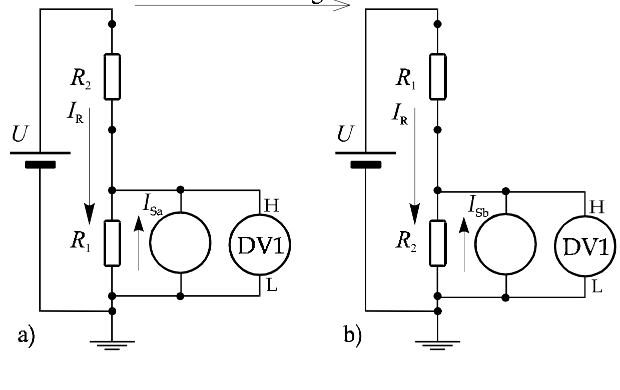

Fig. 5. Input offset current of the DVM flows into the measuring circuit increasing the relative error of the resistance ratio.

One example could be interesting. Let the measured resistors are of 100 MΩ, and total voltage of the resistance series is 10 V. Then, the shift of the DVM's input offset current of only 1 pA will affect resistance ratio with 20 μΩ/Ω in relative error budget.

2.3 Input capacitance of DVM

Time constant *RC* of voltage measured with DV1 across particular resistor determines a voltage stationary state settling period needed to achieve an accurate reading without significant time drift. As shown in Fig. 6, the input capacitance C_V of the DV1 is connected in parallel with the resistance R_1 and is charged through the resistance R_2. Interchange of the resistances positions does not affect the time constant of the input capacitance charging, as it is a function of parallel connection of R_1 and R_2. The voltage readings of the DV1 in both positions display exponential curve u_V parametrically expressed with equation:

$$u_V = U \frac{R_1}{R_1 + R_2} \cdot (1 - e^{-\frac{t}{(C_V \cdot R_1 \| R_2)}}) . \tag{13}$$

The parasitic capacitance C_C (avoided in (13)) of the shielded cable connecting DV1's input terminals and the measuring point must be summed up to the DV1's input capacitance in order to estimate true value of the time constant. A suitable example will demonstrate the capacitance problem. Measuring high-ohm resistances of 10 GΩ using DVM with C_V = 200 pF will produce the charging time constant of 1 s. Mathematically, if the measured voltage time drift should not exceed relatively 10^{-5}, it is necessary to wait 12 time constants before measurement begins, hence 12 s is the shortest period between two voltage readings. Even with tendency of keeping parasitic capacitance of connecting cable as low as possible, the input capacitance of the digital voltmeter is factory fixed and therefore dictating the settling time of the circuitry. Significant reduction of the input capacitance is achieved in specially constructed electrometers (whose C_V is less than 10 pF) having an active guard terminal used for nullifying parasitic cable capacitance as well.

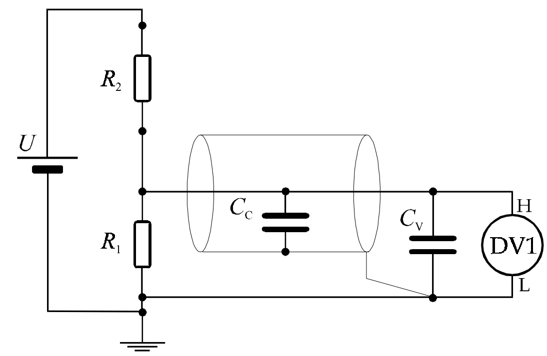

Fig.6. Input capacitance of the DV1, along with parasitic capacitance of the shielded cable, causes the exponential growth of measured voltage.

3. DETERMINATION OF DVM'S INPUT PARAMETERS

The analysis being presented above is showing that the relative ratio error of DVM-based high-ohm resistance comparison method is certainly affected with the input parameters of the measuring instrument. In order to find the capabilities and limitation of the described method using HP 3458A digital voltmeter as the DV1, a method of determination its input parameters has been investigated and realized. Schematics of measuring circuit is shown in Fig 7. DC-voltage calibrator FLUKE 5440B has been used as a very stable voltage source, connected to the DVM through the resistance R_P of 10 GΩ. The resistor R_P is of carbon-film type placed in thermally insulated metal enclosure that insures low thermal drift during measurement, less then 10 μΩ/Ω. The enclosure of R_P is connected to the shield of the coaxial cable attached to the "high" input terminal of the DVM. Voltage drop across the input resistance R_V is measured with the DVM itself, but it is also controlled with the electrometer transconductance amplifier TA having input resistance of 10^{15} Ω and extremely low input offset current ($I_{TA} \cong 7$ fA). Active guard terminal G of the TA equalizes the potential of the cable shield with the potential of the measuring point M, thus eliminating influence of the parasitic cable impedance and leakage resistance of the series resistor R_P.

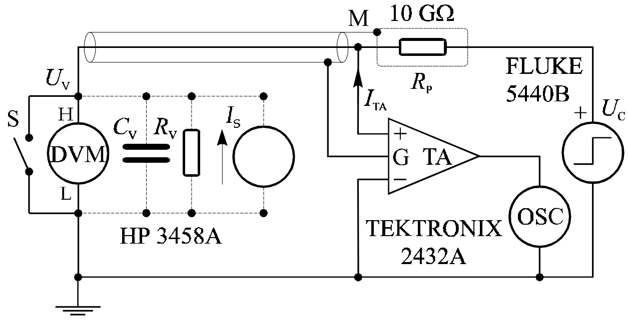

Fig. 7. Measuring circuit for determination of DVM's input parameters.

The calibrator and the digital voltmeter are connected to the PC using IEEE-488 interface bus and are both program-controlled. First measuring step of the method is offset-voltage U_0 measurement when DVM's input terminals are shorted out with switch S in position closed. Next step begins by opening switch S and calibrator output being set to 0 V. In that state the calibrator becomes shorted out and the only current flowing through the circuit is the sum of the input offset currents I_S and I_{TA}, causing noticeable voltage drop U_S across the parallel of R_P and R_V. Since R_V is shunted by smaller R_P, neglecting minor influences of R_V and I_{TA} the internal current I_S could be calculated as:

$$I_S = \frac{U_S - U_0}{R_P} . \tag{14}$$

It has been found experimentally that R_P of 10 GΩ is optimal for attaining significant reading as a compromise between DVM's sensitivity and the thermal (Johnson) noise of the resistor.

For the purpose of input resistance R_V determination, calibrator output must be set on voltage U_C (for example 10 V). After the stationary state has been achieved the DVM-reading of voltage U_V is done. Since R_P was chosen to be large enough to compare with teraohmic R_V, noticeable voltage drop across R_P makes possible the input resistance calculation by following relation:

$$R_V = R_P \cdot \frac{U_V - U_S + U_0}{U_C - U_V + U_S - U_0} . \tag{15}$$

The instability p_{Is} of the DVM's input offset current has been determined by means of experimental standard deviation for a series of 100 voltmeter's readings being taken within 10 minutes. For that purpose thermal stability and good insulation properties of R_P are of the most important. When the calibrator is shorted out, voltage drop across R_P due to input offset current I_S has been monitored on the oscilloscope connected at the measuring point M through the electrometer transconductance amplifier TA. It comes in sight that I_S is pulse-shaped [4] with the period of voltage sampling rate, as a consequence of DVM-integrator's switching when AZERO (auto zeroing) function is enabled. To avoid disturbances owing to pulsed parasitic capacitance charging, the measurement was performed with AZERO function disabled. It follows that temporary instability of the offset voltage U_0 increases, but since U_S in range of millivolts has been measured, this offset-voltage instability does not affect the instability of the internal current being determined. The results are given in Table I. for each of three DVMs of HP 3458A type that are used in PEL for the purpose of resistance standard calibration. It can be seen that internal currents of voltmeters HP 3458A are of picoamperes, as stated by manufacturer, but changes slowly within 10 minutes of measurement period, thus producing relative instability p_{Is} (10) of approximately ±0,1. It has to be mentioned that internal current of the DVM is not influenced by changing of sampling rate (command NPLC), even if AZERO function is enabled.

TABLE I. Results of DVM's input offset current measurement within 10 minutes period (date 2002/7/10).

DVM	I_S	p_{Is}
1.	−0,7 pA	±0,1
2.	3,3 pA	±0,1
3.	−0,18 pA	±0,2

The input resistance R_V and instability p_{RV} was found out at five measuring voltages raised in stepped fashion on 10 V range. The results are shown in Table II. and is noticeable that R_V of teraohmic value is not affected with the measuring voltage. The same measuring sequence was used to find the instability p_{RV} as had been used for p_{Is} determination. It is considered that the deviation of U_V is mostly caused by the instability of R_V, since both instabilities of voltage source U_C and resistance R_P are negligible in the circuit of formed voltage divider R_P-R_V. For input capacitance C_V determination (Table II) a stepped voltage of 10 V is applied and faster sampling rate is used to scan exponential growth of U_V.

TABLE II. Results of DVM's input resistance and input capacitance measurement (date 2002/7/15).

U_C	DVM 1 $R_V(1\pm p_{RV})$/TΩ	DVM 2 $R_V(1\pm p_{RV})$/TΩ	DVM 3 $R_V(1\pm p_{RV})$/TΩ
1 V	1,187·(1 ± 0,15)	1,112·(1 ± 0,11)	1,202·(1 ± 0,12)
3 V	1,184·(1 ± 0,11)	1,105·(1 ± 0,11)	1,219·(1 ± 0,07)
5V	1,191·(1 ± 0,09)	1,107·(1 ± 0,04)	1,233·(1 ± 0,11)
7 V	1,193·(1 ± 0,08)	1,107·(1 ± 0,06)	1,240·(1 ± 0,08)
9 V	1,190·(1 ± 0,08)	1,109·(1 ± 0,08)	1,246·(1 ± 0,05)
C_V	245 pF	263 pF	256 pF

Using appropriate exponential fitting function the time constant $R_P C_V$ has been found, from where input capacitance is calculated. Estimated relative uncertainty of C_V as a result of fitting session is less then ±0,5 %.

4. CONCLUSION

The analysis of influence of DVM's input parameters in DVM-based high-ohm resistance comparison method indicates a possible increase of relative error of resistance ratio particularly by reason of DVM's input resistance and input offset current instability. Interesting period for instability estimation is 10 minutes, as much as comparison of high-ohm standard resistor is usually performing. The results of parameters determination could be used for calculation of the relative error contributions X (8) and Y_S (12) as an illustration of the method of comparison restrictions. If HP 3458A digital voltmeter is used, and its worse-case parameters values are: R_V = 1,2 TΩ; p_{RV} = 0,2; I_S = 3 pA; p_{Is} = 0,2, the contributions X and Y_S are given in Table III. for three high-ohm resistance values (R_1) and two nominal ratios $r = R_1/R_2$, 1:1 and 10:1 respectively. The final conclusion is that comparison method based on HP 3458A digital voltmeter is not competent for measuring resistance standards greater than 100 MΩ because of considerable measurement uncertainty rise. Since the relative errors from Table III. are a function of both the parameter value and associated random drift, they cannot be treated as the systematic errors, so an adequate correction of resistance ratio error can not be done. One possible solution for reducing measurement uncertainty at high-ohm resistance comparison is interfacing DVM with electrometer transconductance amplifier that exhibits input resistance of PΩ and femtoamperic internal current, what is currently investigated in the laboratory PEL.

TABLE III. Contributions of DVM's input parameter instabilities in the relative error of comparison ratio over a range of high-ohm resistances.

r	R_1	X	Y_S
1	100 MΩ	4 μΩ/Ω	3 μΩ/Ω
	10 GΩ	380 μΩ/Ω	300 μΩ/Ω
	1 TΩ	$2{,}8\cdot10^{-2}$	$3\cdot10^{-2}$
10	100 MΩ	0,7 μΩ/Ω	30 μΩ/Ω
	10 GΩ	69 μΩ/Ω	3000 μΩ/Ω
	1 TΩ	$7\cdot10^{-4}$	$3{,}3\cdot10^{-3}$

REFERENCES

[1] J. Butorac, R. Malarić, I. Leniček, "Establishment of Traceability for Croatian Resistance Standards", CPEM 2000 Conference Digest, pp. 94-95, Sydney, Australia, 2000.

[2] M.E. Cage, D. Yu, B.M. Jeckelmann, R.L. Steiner, R.V. Duncan, "Investigating the Use of Multimeters to Measure Quantized Hall Resistance Standards", *IEEE Trans. Instrum. Meas.*, vol. 40, no. 2, pp. 262-266, April 1991.

[3] K.C. Lee, M.E. Cage, P.S. Rowe, "Sources of Uncertainty in a DVM-Based Measurement System for a Quantized Hall Resistance Standard", *Journal of Research of the NIST*, vol. 99, no. 3, pp. 227-240, May-June 1994.

[4] G. Rietveld, C.J. van Mullem, "Uncertainty Analysis of a DVM-based Quantum Hall Measurement Set-up", CPEM 2000 Conference Digest, pp. 90-91, Sydney, Australia, 2000.

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