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AUTO-CORRECTION AND DESIGN-FOR-TESTABILITY IN EMBEDDED MEASUREMENT SYSTEMS

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Abstract - For investigation and training of students in the field of high resolution measurement technology was built an embedded measurement system with 16 bit resolution and additional modules for self-diagnostics and auto-correction, including methods of design-for-testability in analogue circuits.

Keywords: Embedded measurement system; auto-correction; Design-for-testability; analogue Boundary-Scan; evaluation system

1. INTRODUCTION

The exact knowledge of the uncertainty and the actual calibration situation is for an embedded measurement system very crucially, particularly for higher resolution systems of 14 and more bits. The reliability of a measurement subsystem is important for the quality of any measurement results. High resolution does not guarantee automatically high precision for the user (or for a higher ordered controlling system). Therefore teaching includes a wide field of special tasks:

1. Explaining the problems of high resolution measurement systems and possibilities to solve them.
2. Analysing the methods of high stability of system parameters and for noise reduction with special algorithms, circuits, elements, technologies and necessary design steps.
3. Showing methods for the test/calibration of ADCs and analogue circuits in the measurement channel and for the whole measurement chain.
4. Examining algorithm and different realizations for calibration, (self-)diagnostics and auto-correction [1], [2].

An other field is the knowledge of the industrial manufacturing of print cards including the production test. One important way for the cost reduction and augmentation of the reliability is to realise methods of design for test as

- including special components for test driving and diagnostics or/and
- the implementation of a test structure.

It is necessary to show, that the test design is also an important task for the board designer in every design step. It is also important to show, that there are interesting methods to realize design-for-testability.

For these fields of tasks an embedded measurement system with 16 bit resolution and additional modules for self-diagnostics and auto-correction was built. The necessity of access to internal nodes and elements for testing forced a design with jumpers and test points. That gives the possibility, to vary the used structure of the measurement channel or parameters of relevant elements and to study the results. The problems and their solution have been derived from an industrial research project.

2. THE MEASUREMENT SYSTEM

The realized measurement system consists of a 16 bit microcomputer board from Phytec with the processor C167 from Infineon, which is coupled over the interface RS232 (or CAN) to a PC. The C167 is programmed to control the ADC and the self-correction. It also takes over the control of the sampling ADC, the noise reduction for selectable time-windows, simple diagnostic functions and the data preparation and communication. For that embedded virtual device a set of instructions was defined. Every command forces an answer to the PC. The transfer of the results starts after end of measuring. Only after successful transfer the microprocessor will receive the next command. So we have defined time conditions for the sampling process without special sampling hardware. The sampling rate is driven by an internal timer of the microprocessor. Therefore it was necessary, that the interfaces of ADC and microprocessor are adequate for a direct coupling (Fig. 1).

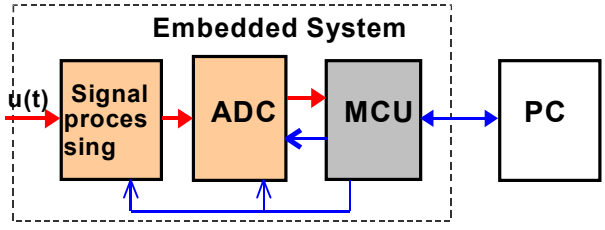

Fig. 1. The embedded system demonstrator

The analogue path includes a 16 bit-DAC with a high stable reference and switches for an active offset compensa-

tion in the input circuit, that can also be used for measuring the gain over the voltage range (Fig. 2). That gives the possibility to correct the measurement value by controlling MCU.

First step is to test the ADC for fixed values of reference voltage by the reference DAC. The MCU stores the results and calculates the offset error and the gain error. With these measured reference and correction values the MCU corrects the ADC values of the measured signal u(t). Proposed the characteristic of the realized analogue channel is very good linear, it is used a linear correction function. The stored offset error serves for an active offset compensation by hardware.

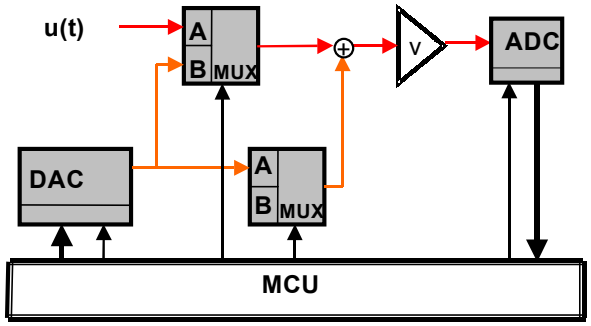

Fig. 2. Principle of self-calibrating circuit

For the examination the embedded measurement system there is an additional PC-controlled measurement system, based on IEEE488 devices (voltage reference source and voltmeter) and controlling program, based on LabView. The microprocessor is coupled about the RS232 interface. With the defined instructions the PC-user can control the work of the embedded system with a special LabView-Library. After the measurements the microprocessor sends the collected data to the PC. The LabView-program realizes the visualisation of the transfer curve.

Parts of the analogue signal processing unit are an offset-adjustable preamplifier (Fig. 2) and modules for special analogue signal handling, like

(a) selectable filters with different characteristics,

(b) calibrating multiplexer circuit for self-calibration systems,

(c) multiplexer with analogue boundary-scan-ability for systems with good on-board testability, corresponding to Fig. 2.

So, for students it is possible to study the problems of real analogue systems. Simultaneous they have to solve the problems of precision measurement technology in practice.

The module corresponding to (c) opens additionally the possibility of design-for-testability in analogue systems by the standard methods of analogue boundary-scan. Here we applied one of the first useable analog test access device with the "normal" function of an analogue multiplexer. In this case no additional circuit for the test access was necessary, because the test access structure is included in the multiplexer circuitry [3].

The IEEE11449.4 test access device from National Semiconductor allows to study the possibilities and the conditions for using this method of DFT in analogue systems for board tests. Additionally there is also the possibility to use this implemented test structure for self-calibration in the real application. Both application fields will be discussed.

The principle of such a circuit is shown in Fig. 3. Similar to digital pins (IEEE1149.1) there are implemented analogue Boundary-Scan Modules (ABM) for all analogue functional pins.

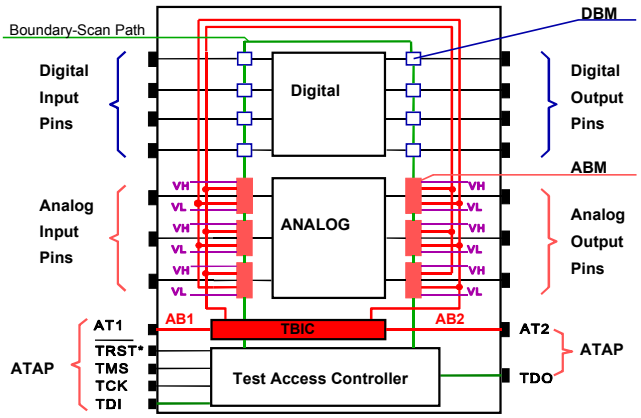

Fig. 3. Circuitry with IEEE1149.4

The principle of such an ABM-cell is shown in Fig. 4. With that standard test structure it is possible, to observe one functional net on the board and - also - to drive a signal into one net without any mechanical probes. Only the connections for the digital and analogue test bus lines are necessary for testing.

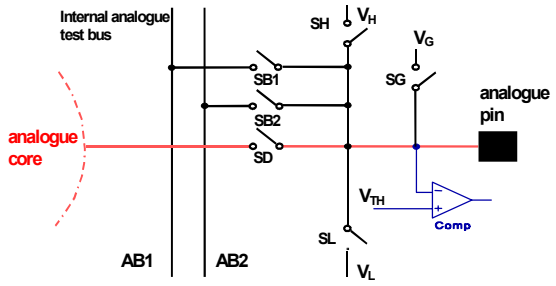

Fig. 4. Principle of an ABM cell in an IEEE1149.4 IC

Such ABMs are implemented in the used Analogue Test Access Device [3] from National Semiconductors. With these implemented "virtual needles" we can use internal test points to stimulate and to observe selected nets on the board or directly nodes in the circuit.

The internal analogue test bus lines **AB1** and **AB2** are connected through the pins **AT1** respectivly **AT2** with the test bus lines on the board (**AT1**, **AT2**). One can drive a defined current from the external test bus port into **AT1**-**AB1** to any selected ABM of the interesting source pin to stimulate the connected circuitry or elements. By selecting the interesting pin (testpoint) the voltage through **AB2**-**AT2** on the external test bus port **AT2** is observable.

For every test it is necessary to form testable circuits. That means, all input and output nodes of those circuit have

to be coupled to an ABM cell or - better – all pins of the elements have to include an ABM.

The simplest example for understanding is shown in Fig. 5. With driving the defined current I_{Meas} into the resistance R_x on ground you can measure the voltage U_{meas} on the line **AT2**. Then you can calculate the value of R_x.

This figure shows the signal pathes with real switches. Every switch causes an additional resistance Z_{SBi} into the signal path. This effect has to be noted for the measurement conditions. Especially, that means

$$R_U >> R_X \text{ and } R_U >> Z_{SBi}.$$

The element R_U is the input resistance of the voltmeter. That describes on the other hand of course the range of useable values for R_X.

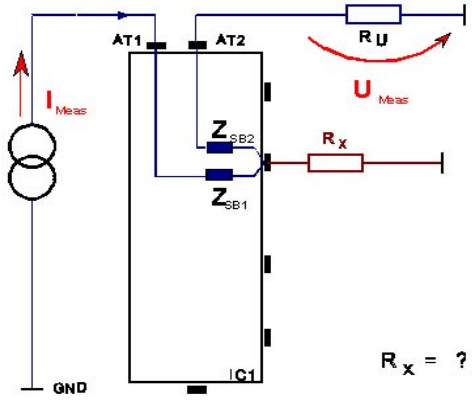

Fig. 5. Analogue Test Access Device

With these test structure we can realise static tests of simple external networks. In some cases we have to subdivide the test in different steps (see example in Fig. 6).

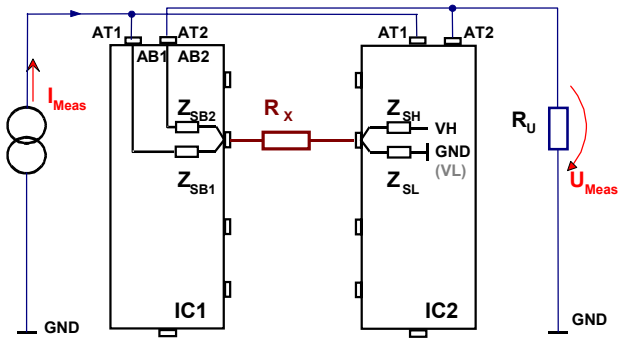

Fig. 6. Analogue Test Access Device

For example, if a resistor is placed between two scanable pins, so one has to realise two steps:

1. Measure U_{Meas1} about $(R_x + Z_{SL})$ from **AT2** of device IC1 with I_{Meas}.
2. Measure U_{Meas2} about $(R_x + Z_{SL})$ from **AT2** of device IC2 with I_{Meas}.
3. Calculate R_x:

$$R_x = (U_{Meas1} - U_{Meas2}) / I_{Meas}$$

This procedure gives the principle way for reducing the effects of the parasitic elements of the embedded test circuit.

Our demonstrator has to solve any problems. First, we want to show the variety of possibilities to test nodes, pathes and elements in a real measurement circuitry. Further, we want to demonstrate the technical limits of the proposed methods without any destroing effects. That should include the possibility of measuring of selected functional parameters. Third, at the moment we can only use one available type of scanable circuit. Therefore we had to find an acceptable compromise.

Now, Fig. 7 shows the internal structure of the analogue test access device with its functional elements and with its implemented test structure. Here we use the two multiplexers reducing the offset error of the amplifier and also for special calibrating cycle.

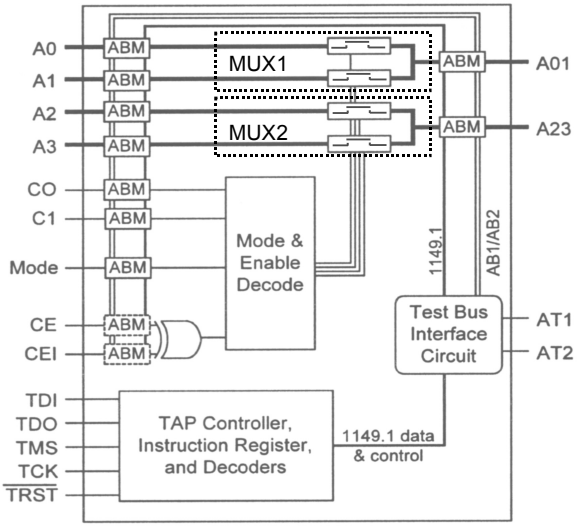

Fig. 7. Analogue Test Access Device [3]

By including the analogue test access device in the structure of Fig. 2 we can realise an analogue scan path, like shown in Fig. 8. These scan path can touch any important test points of the circuit. For scanning the functional pins of the operational amplifier we could include an additional special test circuit for analogue boundary scan.

So we are able to test the connections and embedded elements between all functional analogue pins. All nodes are included in the scan path. That means too, that all crucial nodes can be observed or their voltage levels can be measured.

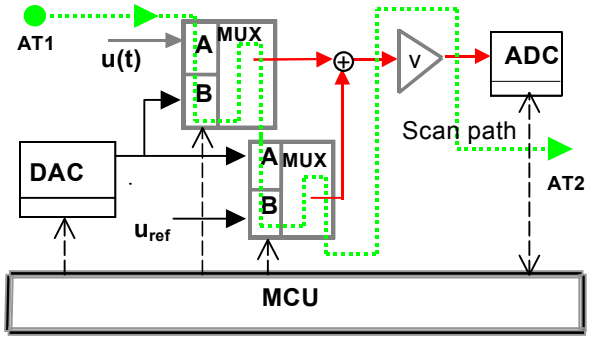

Fig. 8. Measurement system with analogue test path

However, for any industrial use we have to realise also a system for generating the test patterns and to analyse the test results. At the moment, there are only systems for the digital boundary scan method available. But of course, such a system can drive the test bus, which works according to the standard IEEE1149.1, and it collects also the resulting pattern. So we used the available boundary-scan system CASCON from Goepel Electronic. The generating of the test pattern and the analysing of the resulting pattern is a manual work.

3. CONCLUSION

It is shown, that it is possible to design a measurement system of high resolution on a relative simple technological level mainly using modern principles of noise reduction methods and embedded correction features. On the other hand it was shown, that the difference between the demonstrator for high education and its industrial solution is very small. One has to take in account the analogue design and layout rules by including an additional precision reference element and switches. By using the standard IEEE1149.4 there are new DFT possibilities for analogue systems. If the test structure is implemented in standard components, similar to the digital boundary-scan components, then the additional costs are not really important.

It is necessary to force the developing of analogue scanable circuits and corresponding test systems. Then it will be possible to increase the testability of mixed-signal boards and - at all - to reduce the test costs.

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