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ELIMINATION OF UNWANTED VOLTAGE DROPS ACROSS THE LINKS BETWEEN FOUR TERMINAL – PAIR COMPONENTS CONNECTED IN SERIES

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Abstract – Two possible methods of eliminating unwanted voltage drops in four terminal-pair bridge circuits are discussed, namely employment of combining networks and injection of compensation voltages. As an economical and practical way of producing these voltages, application of a slave digital synthesis (DSS) generator, directly synchronized with the source of the bridge supply voltage, is proposed. A possible design of such a generator, based on employment of a DSP evaluation board, is described.

Keywords: combining network, voltage compensation, phase-locked loop

1. INTRODUCTION

In designing precision bridges containing four terminal or four terminal-pair impedances, there is often a need to connect two such components in series and, at the same time, to deal with the fact that a spurious voltage drop is produced by the current passing through their link. For instance, in a simple capacitance bridge consisting of a multi-decade inductive voltage divider *IVD*, a detector *D* and two capacitances, C_1 and C_2, connected in series (Fig. 1), the effect of the voltage U_e between the low-potential leads of the capacitors has to be eliminated. This can be achieved, i.e. the detector reading can be made independent of the value of U_e, by proper adjustment of impedances Z_a and Z_b, which form a so-called *combining network*.

Conditions of correct adjustment of the combining network are identical with balance conditions of the four-arm bridge presented in Fig. 2, which has been derived from the bridge of Fig. 1 by setting the voltage source *U* to zero and by short-circuiting it. Clearly, the bridge of Fig. 2 can be balanced only in case that like impedances are used in the combining network. If, for example, two resistances $R_a = Z_a$ and $R_b = Z_b$ are used, the balance condition is

$$C_1/C_2 = R_b/R_a \qquad (1)$$

Being a special case of dividers consisting of like impedances, a multi-decade inductive voltage divider can also be applied as an excellent combining network.

As an alternative, small voltages having adjustable magnitudes and phases can be injected to compensate the voltage drops across the links between four terminal-pair components.

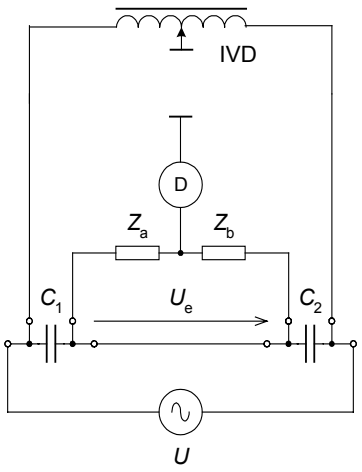

Fig. 1. Capacitance bridge

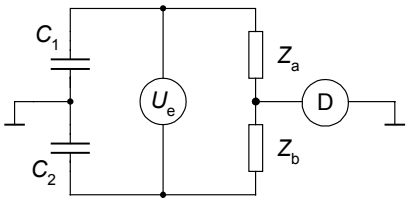

Fig. 2. Four-arm bridge

2. INJECTION OF COMPENSATION VOLTAGES

Compensation voltages can be derived from the bridge supply voltages by means of networks assembled from ratio transformers, inductive voltage dividers and phase shifters, and injected into the links via feedthrough transformers. Of course, this method becomes exceedingly expensive, if a number of such networks has to be used to compensate spurious voltages in complex bridge networks, such as e.g. the four terminal-pair quadrature bridges are [1-2].

A more economical and more practical way of producing the compensation voltages is shown in Fig. 3, where a master generator supplies the bridge and a directly synchronized slave generator delivers one of the required compensation voltages [3]. Of course, in case that a number

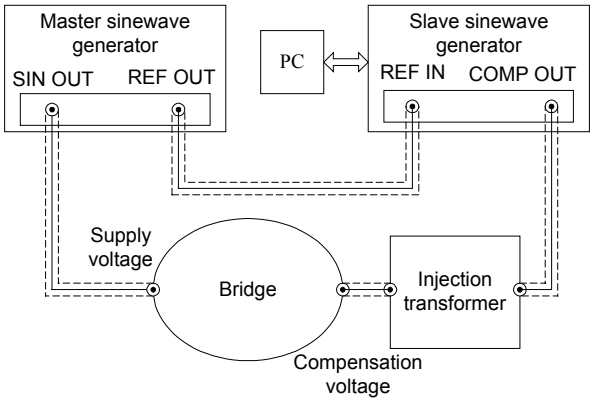

Fig. 3. Derivation of a compensation voltage

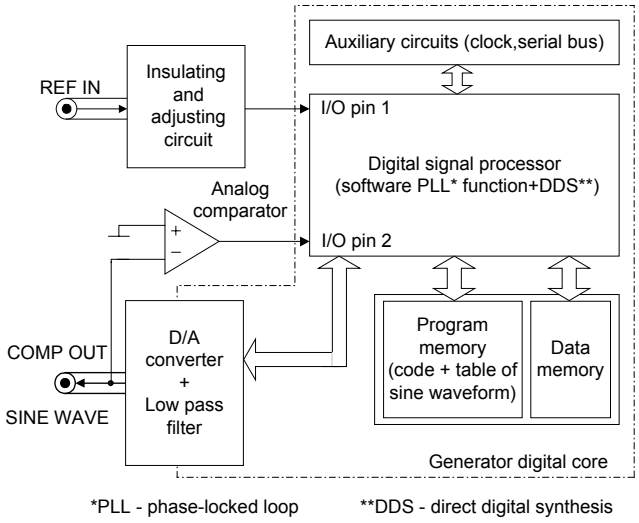

Fig. 4. Slave generator

of compensation voltages is required, a slave generator with a corresponding number of independent outputs has to be realized.

3. PRINCIPLE OF THE SLAVE GENERATOR

The circuit presented here (Fig. 4) makes use of a digital signal processor to provide a *phase-locked loop* (PLL) function, as well as for generating a sinusoidal output voltage by the technique of the direct digital synthesis (DDS). The PLL function is solved only by a software implementation with a minimum hardware support and the corresponding control algorithm flowchart is presented in Fig. 5.

A reference signal (REF OUT, TTL compatible) from the master generator is fed, via insulating and adjusting circuits, directly to the input digital pin of the processor to attain the maximum possible sample rate. The achievement of relatively high accuracy in the measurement of the reference frequency is very important for proper work of the slave generator, namely for the PLL function. The design of control algorithm strictly assumes excellent stability of the input reference signal.

The insulating and adjusting circuits ensure suppression of ground loops and voltage reduction from the TTL level to a level of +3V. This is achieved by application of a resistive divider and an opto-coupler.

The output signal (a sine wave generated by the DDS technique) from the DAC channel is first converted to a square (digital) form by means of an analog comparator and then fed to another input digital pin of the processor to be sampled.

A RS 232 serial port ensures communication with a master PC system and makes it possible to set manually the required magnitude and phase of the generated voltage.

The generator design has been based on employment of an EZ-KIT 2189 M evaluation board. In addition to a digital signal processor, this board includes a 16-bit codec (two A/D and two D/A converters along with low pass filters) with a maximum sample rate of 64 kHz . Only the insulating and adjusting circuits had to be added. A serial bus establishes communication between the processor and the codec.

4. CONTROL ALGORITHM

The control algorithm provides phase locking and sine wave generation for injection of compensation voltages. The corresponding flowchart is in Fig. 5.

The control algorithm consists of a main loop and an interrupt procedure that is used for computing the next sample of sine wave output by the DDS technique.

At the beginning of the main loop, the processor evaluates frequency f_{REF} of the reference signal. Uncertainty of this evaluation being inversely proportional to the sample rate f_{S} (in our case 18.75 MHz) and to the measurement time, it is less than 5 parts in 10^6 for frequencies up to 5 kHz. The reference frequency is calculated from

$$\frac{f_S}{f_{REF}} = N_{REF} \cdot N_A \tag{1}$$

where N_{REF} is the number of the reference signal samples and N_{A} is the number of the averaged results of the measurements of the period of the reference signal. To attain approximately the same PLL settling time in the whole frequency range from 500 Hz to 5 kHz, N_{A} is chosen 250 for $f_{\mathrm{REF}} < 1$ kHz and $N_{\mathrm{A}} = 2500$ for $f_{\mathrm{REF}} > 1$ kHz.

After that, the control algorithm calculates $\Delta\varphi$ according to equation (2) to ensure the sine wave output generation. The frequency f_{DDS} of the output DDS must be the same as the reference frequency f_{REF}. In (2), f_{SC} is the clock rate for DDS (in our case it is given by a codec property, $f_{\mathrm{SC}} = 64$kHz), N is the number of accumulator bits and $\Delta\varphi$ is the increment of accumulator for the required frequency f_{REF}.

$$f_{DDS} = \frac{f_{SC}}{2^N} \cdot \Delta\varphi \tag{2}$$

The DDS algorithm utilizes a 32-bit accumulator and works with 4096 sine samples, stored in the processor program memory. The 32-bit accumulator wide guarantees

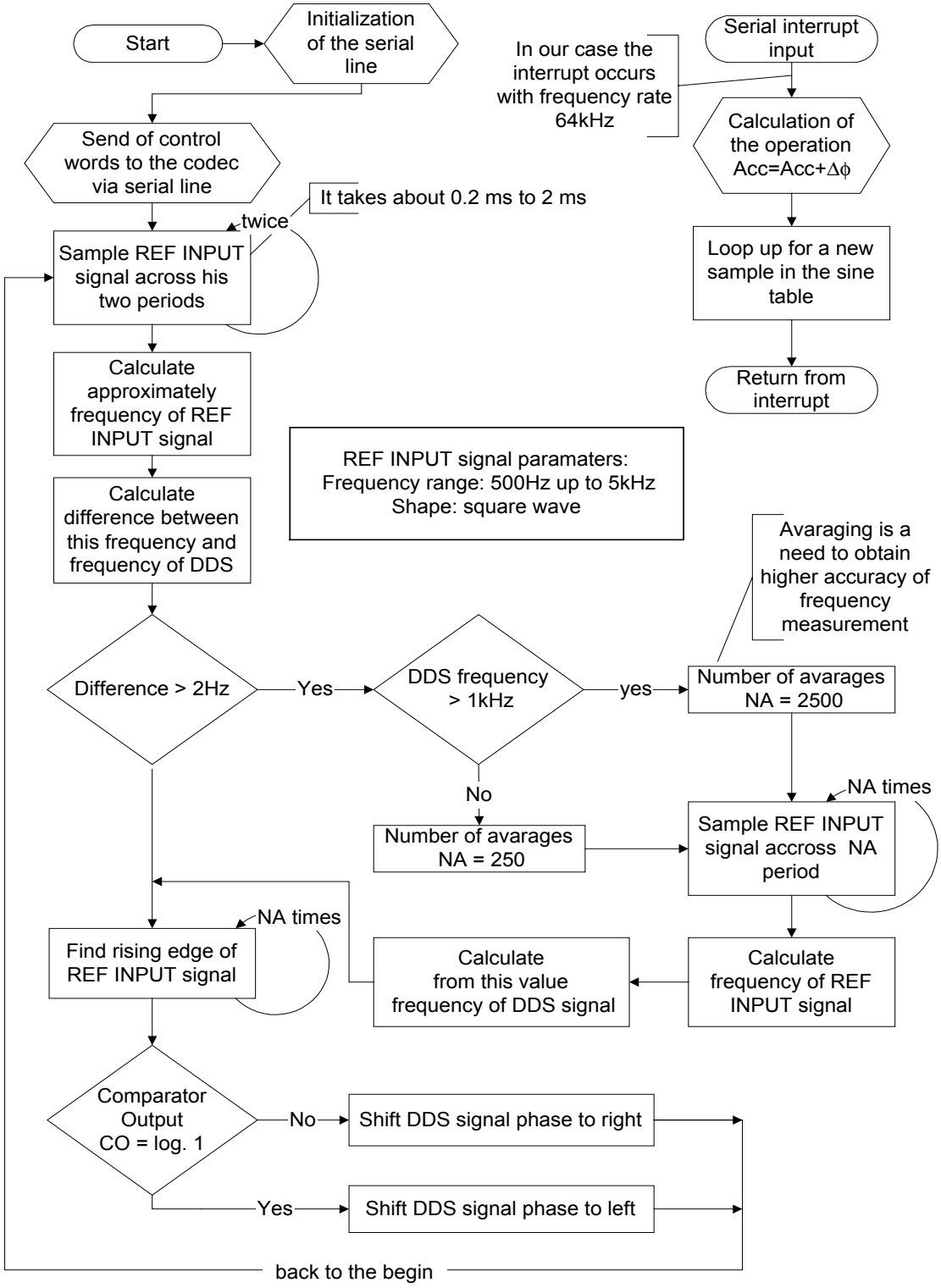

Fig. 5. Control diagram

frequency resolution of approximately 15 μHz for f_{SC} = 64kHz. Once the value of the frequency of the reference signal is known, output voltage COMP OUT of comparator is sampled, the phase of the generated voltage is evaluated, and the control algorithm ensures a phase shift necessary for obtaining the required phase value. If a jump in frequency occurs, the settling time is approximately 2 seconds. In case that the change of the reference frequency does not exceed 2 Hz, the DDS signal frequency remains unchanged. The control algorithm measures only the phase shift after each signal period and adjusts the phase between the reference and the generated signal by means of addition /subtraction of a constant to/from the value stored in the DDS accumulator. The adjusting of phase appears in the output sine wave signal as a phase jitter of ± 1° and causes also a decrease of total harmonic distortion (THD) of output signal. In spite of these facts, the THD of sine wave output signal is better than -60dB.

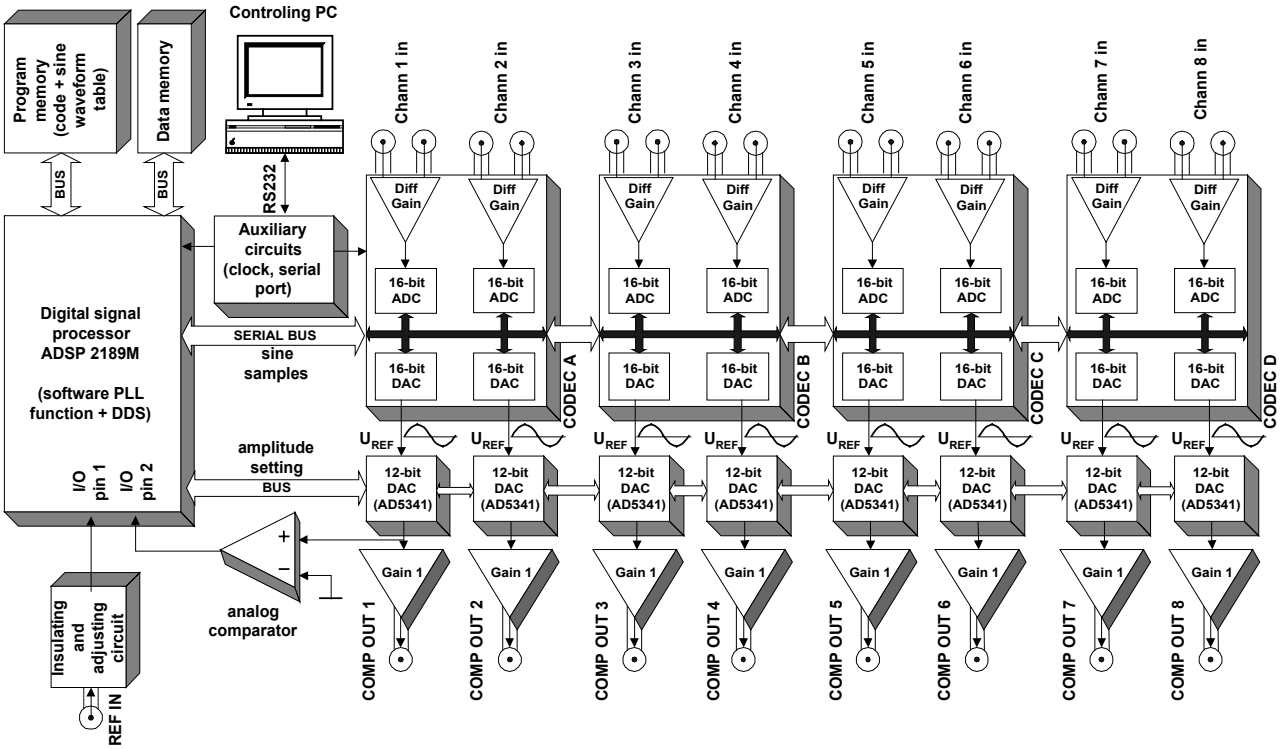

Fig. 6. Block diagram of an 8-channel slave generator

5. PRELIMINARY RESULTS

As an example, results of measurement of spurious voltage drops across a link between two 10 kΩ four terminal-pair resistors are given in Table I. A substantial reduction of the original drops accomplished by the injection of compensation voltages is evident. An inductive voltage divider has been used for setting the required magnitudes of the compensation voltage in course of this test. Thanks to a sufficient computational performance of the digital signal processor, equipment of the present generator by more independent outputs is possible.

At present, we are developing an 8-channel slave generator, a block diagram of which is shown in Fig.6. This solution already includes pre-amplifiers and AD converters to enable automatic compensation of spurious voltage drops. The new design of the slave generator will also implement an algorithm based on synchronous filtering [4]. Advantage of such a design consists in integration of detectors, synchronous demodulators realized by software, and output amplifiers into one circuit.

TABLE I. Spurious voltage drops

Frequency [kHz]	Voltage drop before compensation	Voltage drop after compensation	Reduction
0,5	51 µV	120 nV	425 times
1	67 µV	47 nV	1425 times
2	95 µV	53 nV	1792 times
3	115 µV	66 nV	1742 times
4	132 µV	72 nV	1714 times
5	145 µV	85 nV	1705 times

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