24th IMEKO TC4 International Symposium
22nd International Workshop on ADC and DAC Modelling and Testing
IMEKO TC-4 2020
Palermo, Italy, September 14-16, 2020

A novel measurement method for DAC frequency response characterization

Luca De Vito, Francesco Picariello, Ioan Tudosa

Department of Engineering, Unversity of Sannio, Benevento, Italy
e-mail: {devito, fpicariello, ioan.tudosa}@unisannio.it

***Abstract* – The paper proposes a novel measurement method for frequency response characterization of Digital-to-Analog Converters (DACs). The method uses a Compressive Sampling (CS) technique which exploits the sparsity of the DAC impulse response in the time domain. The mathematical formulation of the method and its preliminary simulation analyses are presented. The obtained results demonstrate that the proposed measurement method based on CS could benefit from a significant sampling rate reduction respect to the Nyquist one.**

I. INTRODUCTION

A Digital-to-Analog Converter (DAC) is a device (or system component) responsible for the domain transformation of a signal from its numerical representation to an analog waveform. The correct functionality of DAC devices differs according to their field of applications. Examples are ranging from medical equipment, telecommunications, wireless sensors and actuator networks, industrial plants, up to test instrumentation, to name few. This variety of application fields impose to choose DACs according to the [1]: (i) vertical resolution in terms of bits, (ii) samples update rate in terms of clock frequency, (iii) Spurious Free Dynamic Range (SFDR), and (iv) to the analog output bandwidth. In practice, the DAC's analog output path is affected by the: (i) manufacturing process which adds parasitics to the Integrated Circuit (IC) package, (ii) extra subsystems components and circuitry interconnects, (iii) temperature variations, and (iv) various mismatches (e.g. impedance, transistor threshold voltage, etc.). All of these will lead to a degradation of the generated waveform [1] and due to this reason, the measurement of the frequency response of a DAC is a desideratum in many fields of applications.

In Fig. 1, the frequency response of a DAC working at a sampling frequency f_s is depicted. The frequency response is an indication of the analog bandwidth of the DAC. It is worth remembering that, due to the zero-order hold mechanism of the DAC's circuitry, the frequency response presents a *sinc*–shaped transfer function [2]. As it can be visualised from Fig. 1, the 3 dB–bandwidth of a DAC frequency response is evaluated to be at the frequency where the DAC transfer function gets underway

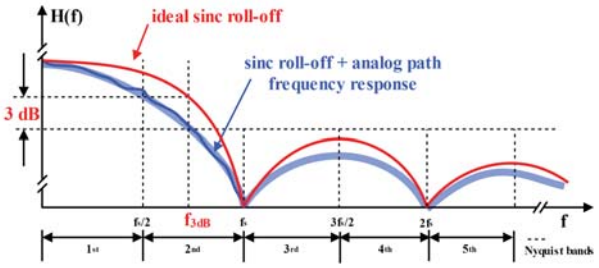

Fig. 1. Generic frequency response of a DAC (adapted from [1]).

from an ideal *sinc* by 3 dB, [3]. In order to compensate this effect of the *sinc* roll-off, a magnitude characterization is necessary.

Measuring accurately the DAC's frequency response is a challenging task. Recently, the research community in the field of metrological characterization of data converters has raised particular attention regarding the development of novel powerful measurement techniques. In [3], a method based on least square estimation, which can be utilized to characterize the DAC from dc to any target frequency, is proposed. Furthermore, the Authors demonstrated that their method can be also utilized to [3]: (i) derive the impulse response of the DAC, (ii) predict DAC operating bandwidth, and (iii) provide an insight into DAC sources of distortion. Besides all the above advantages of [3], the main issue remains its practical implementation, since it requires an Analog-to-Digital Converter (ADC) operating at the Nyquist frequency of the DAC under test. Other proposals have been published in [4]–[9]. The utilized approaches are based on generating full-scale sinewave tones at the output of the DAC and measuring them by means of laboratory bench signal analyzers. By sweeping the generated sinewave frequency, the magnitude response of the DAC under test will be obtained. However, if the output frequency increases, the *sinc* roll-off will determine a decrease in output signal amplitude, and this measurement will specify the DAC ac performance. Although, due to the field operating environment conditions and aging, changes in the frequency response of DACs are happening, thus making the existing frequency response characterization inappropriate. To this reason, developing novel measurement techniques that could be integrated into DAC chips

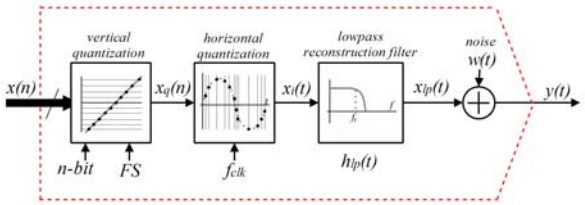

Fig. 2. Simplified DAC model.

will allow Built-in-Self Test (BIST) systems [10]–[17] to monitor those changes (e.g. when it is required) and it will relax the field maintenance of sensitive equipment [1].

In this paper, a novel measurement method which exploits a Compressive Sampling (CS)–based technique for DAC frequency response characterization is proposed. The aim of this research is to uniquely develop a circuit architecture for BIST implementing a such innovative measurement method [18].

The rest of the paper is organized as follows. In Section II, a short overview of the DAC frequency response modelling is presented. The proposed measurement method and its mathematical formulation are described in Section III. A preliminary simulation analysis and its discussion is reported in Section IV. Last Section presents the conclusions and future work.

II. DAC FREQUENCY RESPONSE MODELLING

A model describing the DAC output waveform according to several non-idealities was proposed in [19]. In particular, the causes of non-idealities affecting the DAC output waveform are classified in [19]: (i) vertical quantization, (ii) horizontal quantization, and (iii) clock modulation. The vertical quantization refers to the discrete-amplitude nature of the generated DAC waveform. In particular, the amplitude level of the samples are approximated with the nearest voltage level, which are identified according to the DAC Full Scale (FS) and its resolution. Furthermore, due to the Integral Non-Linearity (INL), the DAC output values do not match the expected ones (i.e. nearest voltage levels) according to the input codes [19]. The horizontal quantization refers to the discrete-time nature of the DAC waveform. It is the main degradation factor when the generation frequency is not sufficiently greater than the Nyquist frequency of the expected waveform. In addition to horizontal quantization, further spurious components appear in the spectrum of the output waveform when the clock source f_{clk} is affected by periodic variations in the generation period T_{clk}. Thus, each generated instant can either be delayed or anticipated respect to its expected position.

By considering the above mentioned non-idealities and the DAC architecture described in [2], the model used in this paper has been carried out according to the general architecture depicted in Fig. 2. This architecture consists of four functional blocks: (i) vertical quantization, (ii) horizontal quantization, (iii) lowpass reconstruction filter, and (iii) additive noise. The vertical quantization (i.e. known and as the uniform amplitude quantization) is a deterministic effect upon sample points (e.g., $x(n)$, which describes a discrete waveform) bonded by a finite voltage resolution of a DAC ($n-bit$) while is approximating with the nearest voltage level those samples. In [19], the Authors states that the vertical quantization effects are weakly coupled with the horizontal quantization and time base stability (f_{clk}). Therefore, in this paper, the vertical quantization effects are not taken into account. The horizontal quantization is performed on the $x(n)$ samples by means of zero-order hold [2], which consists of holding the voltage constant at the DAC output for the update period $T_{clk} = 1/f_{clk}$. This operation can be modeled as:

$$x_i(t) = \sum_{n=-\infty}^{n=+\infty} x(n) \cdot g\left(\frac{t - n \cdot T_{clk}}{T_{clk}}\right) \tag{1}$$

where, $g(\theta)$ is the unitary pulse function with unitary duration in the normalized time variable, θ:

$$g(\theta) = \begin{cases} 1, & \text{if } 0 \leq \theta < 1 \\ 0, & \text{elsewhere} \end{cases}. \tag{2}$$

Eq. (1) is equivalent to the time-domain convolution of an ideal train of Dirac's pulses, having $x(n)$ as amplitude, and a square pulse with T_{clk} duration [20], [21]. Thus, the frequency response of the DAC by considering the zero-order hold operation is given by [2], [20]:

$$H_{zoh}(f) = sinc\left(\frac{\pi f}{f_{clk}}\right) \tag{3}$$

The reconstruction filter performs the following functions [21]: (i) remove all the unwanted images from the output signal, and (ii) equalize the response in the target output band to remove the linear distortion due to the DAC frequency response. Cut-off frequencies for reconstruction filters depend on the DAC sampling rate and the target Nyquist band (see Fig. 1).

In the proposed analyses the reconstruction filter is a lowpass filter which has a frequency response equal to $H_{lp}(f)$. The noise component affecting the DAC output has been modeled as Additive White Gaussian Noise (AWGN), $w(t)$, with null mean, operating on the lowpass reconstruction filter output, $x_{lp}(t)$, as follows:

$$y(t) = x_{lp}(t) + w(t) \tag{4}$$

The overall frequency response of the DAC is given by:

$$H_{DAC}(f) = H_{zoh}(f) \cdot H_{lp}(f) \tag{5}$$

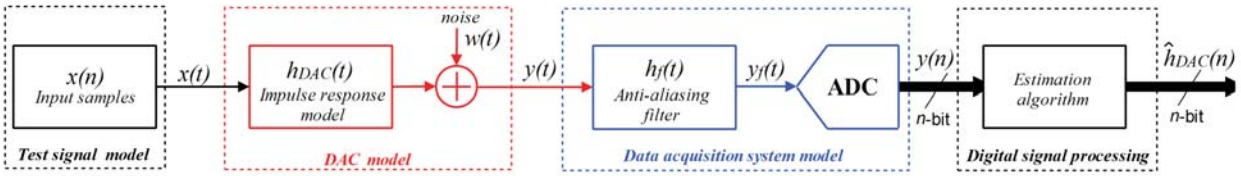

Fig. 3. Simplified model of the proposed method for DAC frequency response measurement.

III. THE PROPOSED METHOD

The proposed method is derived from [22] where it was used for estimating the frequency response of a wireline channel by means of CS.

By considering the impulse response, $h_{DAC}(t)$, and a finite number of input codes $x(n), n = 0, \ldots, N + L - 1$, the DAC output (see Fig. 3) can be modeled as:

$$y(t) = x(t) * h_{DAC}(t) + w(t), \tag{6}$$

where:

$$x(t) = \sum_{m=-L}^{N-1} x(n) \cdot \delta(t - n \cdot T_{clk}), \tag{7}$$

T_{clk} is the generation clock period, $w(t)$ is the AWGN affecting the DAC output, $\delta(t)$ is the Dirac's pulse, and $*$ denotes the convolution operation. According to the proposed architecture (see Fig. 3), the DAC output $y(t)$ is firstly filtered with the anti–aliasing filter $h_f(t)$ and then it is acquired by the ADC at the sampling frequency f_{ADC}. The anti–aliasing filter has a cut–off frequency equal to $1/2T_{clk}$ in order to limit the bandwidth of $y(t)$ into the range [0, $1/2T_{clk}$]. The output of the anti–aliasing filter $y_f(t)$ is given by:

$$y_f(t) = x(t) * [h_{DAC}(t) * h_f(t)] + w_f(t), \tag{8}$$

where:

$$w_f(t) = w(t) * h_f(t) = \int_{-\infty}^{\infty} h_f(t - \tau) w(\tau) d\tau. \tag{9}$$

In (7), the considered number of input DAC codes is $N+L$, where NT_{clk} is the duration of the acquisition window and LT_{clk} represents the maximum duration of the DAC impulse response. The sampled version of the DAC impulse response is considered K-sparse in the time domain, i.e. it contains at most K samples, with $K < L$.

Taking into consideration $h_c(t) = h_{DAC}(t) * h_f(t)$, the resulting impulse response of the cascade of the DAC and of the anti–aliasing filter can be rewritten as:

$$\begin{aligned} y_f(t) &= x(t) * h_c(t) + w_f(t) = \\ &= \int_{-\infty}^{\infty} x(t - \tau) h_c(\tau) d\tau + w_f(t). \end{aligned} \tag{10}$$

With respect to (7) and that $h_c(\tau)$ is time invariant during the generation, (10) can be written as follows:

$$y_f(t) = \sum_{n=-L}^{N-1} x(n) \cdot h_c(t - nT_{clk}) + w_f(t). \tag{11}$$

Since $y_f(t)$ and $h_c(t)$ were filtered by the anti–aliasing filter, having cut–off frequency equal to $1/2T_{clk}$, their bandwidths are also $1/2T_{clk}$. By taking into consideration that the ADC works at the sampling frequency $1/T_{clk}$, the acquired samples can be expressed as:

$$y_f(mT_{clk}) = \sum_{n=-L}^{N-1} x(n) \cdot h_c(mT_{clk} - nT_{clk}) + w_f(mT_{clk}) \tag{12}$$

In agreement with the fact that the maximum duration of the impulse response of the DAC is LT_{clk}, (12) can be written as:

$$y_f(mT_{clk}) = \sum_{n=0}^{L-1} x(m - n) \cdot h_c(nT_{clk}) + w_f(mT_{clk}) \tag{13}$$

In matrix form, it leads to the following expression:

$$\mathbf{z} = \mathbf{X}\mathbf{h}_c + \mathbf{w}_f, \tag{14}$$

where:

$$\mathbf{X} = \begin{bmatrix} x(0) & x(-1) & \ldots & x(-L+1) \\ x(1) & x(0) & \ldots & x(-L) \\ \vdots & \vdots & \ddots & \vdots \\ x(N-1) & x(N-2) & \ldots & x(N-L-2) \end{bmatrix}. \tag{15}$$

and:

$$\begin{aligned} \mathbf{z} &= [y_f(0),\ y_f(T_{clk}),\ \ldots,\ y_f((N-1)T_{clk})]^T, \\ \mathbf{w}_f &= [w_f(0),\ w_f(T_{clk}),\ \ldots,\ w_f((N-1)T_{clk})]^T, \\ \mathbf{h}_c &= [h_c(0),\ h_c(T_{clk}),\ \ldots,\ h_c((L-1)T_{clk})]^T. \end{aligned}$$

In order to take advantage of the DAC impulse response sparsity in the time domain, the ADC can work at a sampling frequency f_{ADC} lower than the Nyquist one, f_{clk}. In this way, during the time window NT_{clk}, the ADC acquires a vector of M samples, $\mathbf{y} = [y(1),\ y(2),\ \ldots,\ y(M-1)]^T$, with a downsampling factor $CR = f_{clk}/f_{ADC}$. This operation can be modeled as follows:

$$\mathbf{y} = \mathbf{R}\mathbf{X}\mathbf{h}_c + \mathbf{w}_f, \tag{16}$$

where, $\mathbf{R}$ is a $M \times N$ matrix, modeling the process of downsampling by CR. If $M < L$, in the time domain, $\mathbf{h}_c$ can be estimated by solving:

$$\begin{aligned} &\widehat{\mathbf{h}}_c = \arg\min_{\mathbf{h}_c} \|\mathbf{h}_c\|_1, \\ &\text{subject to:} \quad \mathbf{y} = \mathbf{R}\mathbf{X}\mathbf{h}_c \end{aligned} \tag{17}$$

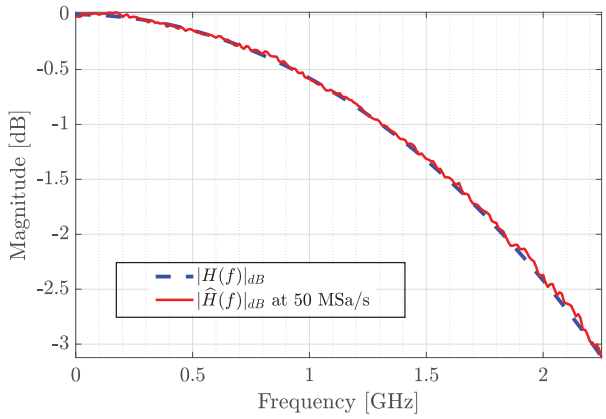

Fig. 4. Comparison of the magnitudes of the estimated frequency response (red line) with the ADC working at $50\,\mathrm{MSa/s}$ *and the ideal one (blue line).*

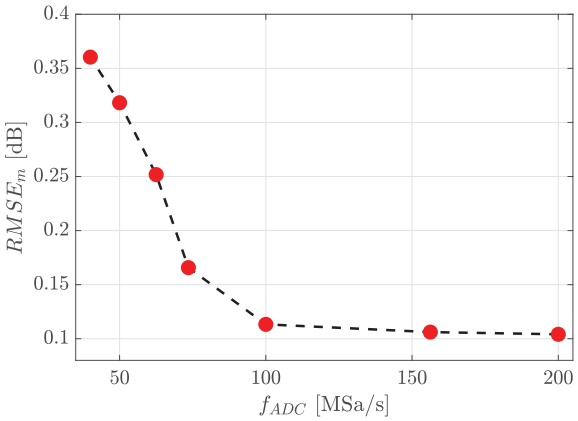

Fig. 5. Average of the $RMSE$*s against the ADC sampling frequency ranging from* $40\,\mathrm{MSa/s}$ *up to* $200\,\mathrm{MSa/s}$.

where, $\|\cdot\|_1$ represents the ℓ_1 norm operator.

The problem in (17) is solved with the Orthogonal Matching Pursuit (OMP) [23] algorithm, which exhibits a low computational load compared with the others (i.e. basis pursuit and greedy algorithms) and a good reconstruction quality.

From $\widehat{\mathbf{h}}_c$, it is possible to derive the frequency response of the DAC in the frequency range $[0, 1/2T_{clk}]$, by:

$$\widehat{H}_{DAC}(k/T_{clk}) = \frac{\widehat{H}_c(k/T_{clk})}{H_f(k/T_{clk})}, \tag{18}$$

where, $\widehat{H}_c(k/T_{clk})$, and $H_f(k/T_{clk})$ are the Discrete Fourier Transforms (DFTs) of $\widehat{h}_c(mT_{clk})$, and $h_f(mT_{clk})$, respectively.

IV. SIMULATION ANALYSIS

A. Simulation setup

The aim of the simulation tests is to select the specifications of the ADC to be used for acquiring the signal provided by the DAC, and then estimating the DAC frequency response. The considered ADC specifications are: (i) the ADC sampling frequency, f_{ADC}, (ii) the ADC resolution, and (iii) the number of samples acquired by the ADC, M. The figure of merit used to assess the performance of the proposed method against the above mentioned specifications refers to the Root Mean Square Error $RMSE$ of the magnitude of the estimated frequency response, $\widehat{H}_{DAC}(k/T_{clk})$, respect to the ideal one, $H_{DAC}(k/T_{clk})$:

$$RMSE = \sqrt{\frac{1}{L}\sum_{k=0}^{L-1}\left[|\widehat{H}_{DAC}(k)|_{dB} - |H_{DAC}(k)|_{dB}\right]^2} \tag{19}$$

Monte Carlo analyses have been performed on 100 trials and the average of the obtained $RMSE$s has been provided for each performed simulation test, $RMSE_m$.

The simulated DAC has the following characteristics: (i) the clock frequency f_{clk} is fixed to $5\,\mathrm{GHz}$, (ii) the bit resolution $n-bit$ is 12, (iii) the full scale FS is $2\,\mathrm{V}$, (iv) the lowpass reconstruction filter is a Finite Impulse Response (FIR) filter having cut–off frequency of $6\,\mathrm{GHz}$, and (v) the Signal to Noise Ratio (SNR) of the the DAC output signal is $70\,\mathrm{dB}$. On the other hand, the data acquisition system, which contains the ADC, has an anti–aliasing filter that has been simulated as FIR filter having cut–off frequency of $2.25\,\mathrm{GHz}$. Furthermore, the ADC full scale has been fixed to $4\,\mathrm{V}$.

B. Simulation results

In Fig. 4, the magnitudes of the estimated frequency response $\widehat{H}_{DAC}(f)$ and the ideal one $H_{DAC}(f)$ are depicted. In this simulation, the sampling frequency of the ADC, f_{ADC}, is $50\,\mathrm{MSa/s}$, the ADC resolution is 16–bit, and the number of acquired samples, M, by the ADC is 125. The obtained results show that the estimated frequency response well approximates the ideal one for the frequency range up to $2.25\,\mathrm{GHz}$, which is the cut–off frequency on the anti–aliasing filter. By considering an ADC bit resolution of 16–bit, Monte Carlo analyses have been performed for assessing the mean of the $RMSE$s against the ADC sampling frequency ranging from $40\,\mathrm{MSa/s}$ up to $200\,\mathrm{MSa/s}$. For the simulations N is 5000, thus for the sampling frequency of $40\,\mathrm{MSa/s}$, the number of acquired samples M is 40. The obtained results are reported in Fig. 5. It can be noted that by increasing the sampling frequency the $RMSE$ decreases, however, all the obtained values are lower than $1\,\mathrm{dB}$. For the further analyses, the sampling frequency has been fixed at $50\,\mathrm{MSa/s}$.

Another analysis has been performed for assessing the

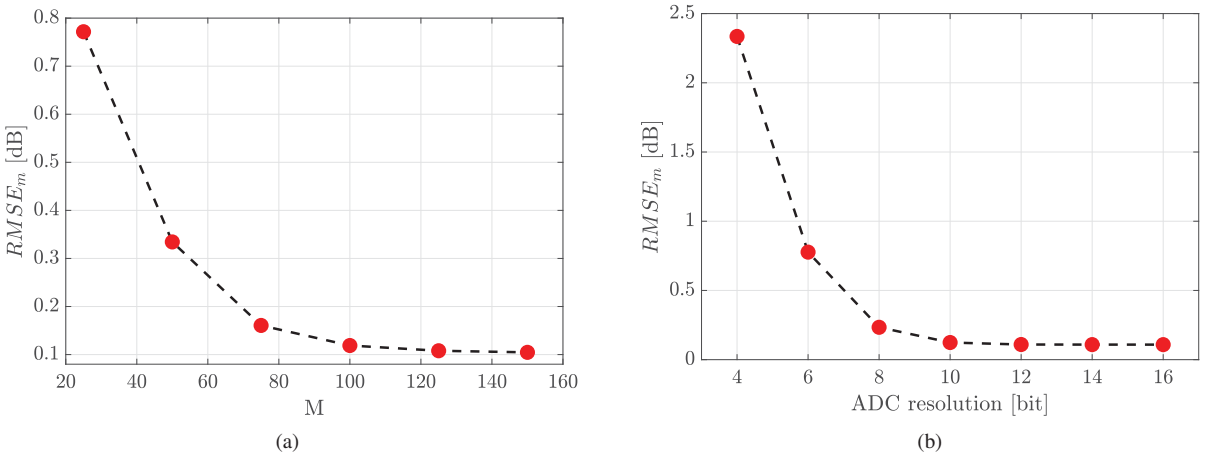

Fig. 6. Average of the $RMSE$s against the: (a) number of acquired samples by the ADC, M, ranging from 25 up to 150, and (b) ADC resolution ranging from 4–bit up to 16–bit with a step of 2–bit.

$RMSE$ against the number of acquired samples by the ADC, M, ranging from 25 up to 150. The sampling frequency of the ADC is $50\,\mathrm{MSa/s}$ and the ADC resolution is 16–bit. As depicted in Fig. 6a, the performance of the proposed method depends on the number of acquired samples. In particular, by increasing the M, the $RMSE$ values decrease. As in the previous case, the obtained $RMSE$s are lower than $1\,\mathrm{dB}$. For the further analysis, the number of acquired samples by the ADC is equal to 125. For this value, the mean of the $RMSE$s is around $0.1\,\mathrm{dB}$.

The last analysis has been performed for assessing the $RMSE$ against the bit resolution of the ADC ranging from 4 bit up to 16 bit with a step of 2 bit. For this analysis, the sampling frequency of the ADC is $50\,\mathrm{MSa/s}$ and the number of acquired samples M is 125. As it was expected, the obtained $RMSE$ decreases with the ADC resolution increasing (see Fig. 6b). In particular, by considering the ADC resolutions higher than 10 bit, the obtained $RMSE$ values are around $0.1\,\mathrm{dB}$.

All the reported results demonstrate as the proposed method for estimating the frequency response of a DAC, up to half the DAC clock frequency, exhibits an accuracy in terms of $RMSE$ in the order of $0.1\,\mathrm{dB}$, if a 10–bit ADC working at $50\,\mathrm{MSa/s}$ with $M = 125$ is adopted.

V. CONCLUSIONS AND FUTURE WORK

In this paper, a novel measurement method for DAC frequency response estimation was presented. The method exploits the Compressive Sampling theory regarding the time domain sparsity of the DAC's impulse response. The proposed method can be utilized for DAC frequency response compensation as it is shown in Fig. 7.

Future work will be directed to: (i) develop a hardware prototype implementing the proposed measurement method, (ii) the experimental assessment of the implemented prototype, (iii) the comparison of the experimental results with the theoretical ones obtained in simulations, and (iv) to verify that the proposed measurement method can be used for DAC frequency response compensation as depicted in Fig. 7.

VI. ACKNOWLEDGEMENT

The authors would like to thank Prof. Pasquale Daponte for his helpful suggestions during all the phases of the research.

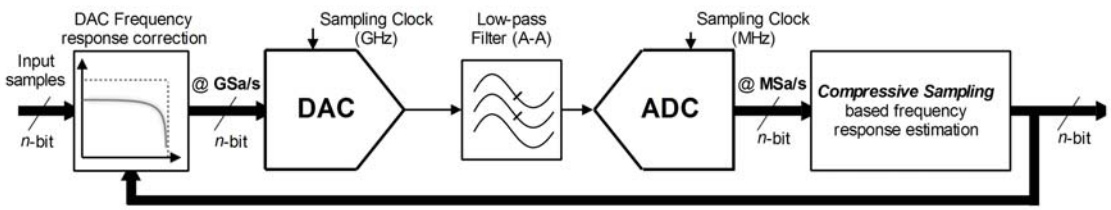

Fig. 7. Scheme for DAC frequency response estimation/correction with the proposed method.

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