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Influence of the capacitor's dielectric absorption on the dual slope ADC

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***Abstract* – Paper deals with the influence of parasitic parameters representing the dielectric absorption of a real capacitor. Dielectric absorption causes nonlinearity of the transfer characteristic of dual slope analog to digital converters. Theoretical analysis and simulation results determine more precisely the requirements on the utilised components.**

***Keywords* – Dielectric absorption, Dual slope ADCs**

I. INTRODUCTION

Dielectric absorption (DA) of capacitors is a source of possible errors in the analog preprocessing blocks and integrating analog to digital converters. The physical reason – relaxation of the dielectric dipoles in the capacitor's dielectric – is manifested by the "memory" effects in capacitors utilized in the analog preprocessing blocks. Dielectric absorption is an integral parameter determining influence of the residual charge from absorption capacitors. Dielectric absorption causes the nonlinearity in the analog preprocessing blocks such as sample and hold circuits (S&H), Voltage Controlled Oscillators (VCOs), exponential signal generators and Integrating Analog to Digital converters (IADCs).

Application manuals of the IADCs recommend to use an integrating capacitor components with low dielectric absorption [1], [2]. Manuals simply recommend polypropylen capacitor where the dielectric absorption is low (DA ≤ 0.5%).

Final effect of the dielectric absorption is modelled by parasitic RC dipoles. Their time constants and residual capacities influence error of preprocessing circuits in any data acquisition block. It seems, that nonlinearity errors of Dual Slope Integrating ADCs (DS-IADC) are influenced not only by the value of the DA, but by the parameters of parasitic dipoles as well.

Theoretical analysis of the DS-IADC converting process allows to reconsider restrictions given on the capacitors. Software tool designed on the base of this analysis allows to assess impact of the available capacitors on the market on the nonlinearity of the converter. Paper [3] presents ASIC design of DS-IADC made as electrometers for the current measurement from the monocrystalline diamond for clinical dosimetry sensors. Proposed ASIC structure allows to integrate currents smaller than pA close to the sensing part. The integration capacitor is made with "metal – metal capacitor" technology, where the capacitor structure is made by dedicated oxide layer for the capacitor between METAL5 and METAL6 layer, suitable for chosen ASIC technology. In order to identify the nonlinearity limits of the implemented converter the dielectric properties of the oxide layer have to be estimated in advance.

This paper is organized as follows: section 2 introduces model of the dielectric relaxation effects. In section 3 the influence of the dielectric absorption components on the accuracy of an idealized DS-IADC is theoretically analysed. Section 4 presents the simulation results of the absorption effects on the nonlinearity of the transfer characteristic after offset and gain correction. The main novelty of this paper is the analysis of essential absorption effects determining IADC nonlinearity even independently on value of DA coefficient.

II. DIELECTRIC RELAXATION IN REAL CAPACITORS

Dielectric relaxation process of a capacitor can be modelled as shown in Fig. 1. Here the capacity C represents the ideal behaviour of the capacitor. Parallel RC branches represent the relaxation processes in the dielectric. In the real capacitor with significant dielectric absorption the charge on the capacity C is being recovered from the parasitic capacitors (C_1, C_2, ..., C_i) for any change of its voltage.

The DA represents percentage of the voltage, which is recovered on the capacitor C when previously charged capacitor is shorted for a short time. The testing procedure is standardized and described in [7] Fig. 2.

Let us consider shorting time smaller than the time constants of the dipoles. After breaking of the short-circuit the charges from the parasitic capacitors C_1, C_2, ..., C_i (Fig. 1) will partially recover the charge in the ideal

capacity C.

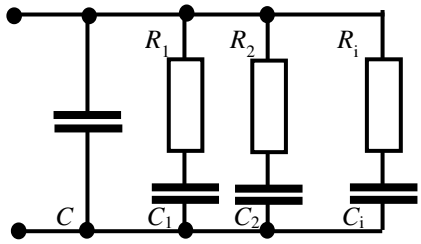

Fig. 1. Electrical model of the dielectric absorption in the capacitor.

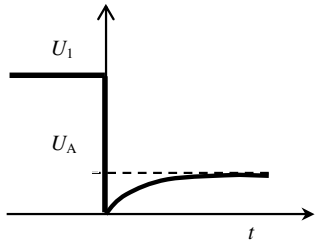

Fig. 2 Measurement of DA coefficient

The DA coefficient is expressed by the ratio

$$DA = \frac{U_A}{U} = \frac{C_1 + C_2 + \cdots C_i}{C} 100\% \cdot \qquad (1)$$

DA coefficient gives no information about time constants of the parallel RC branches in the capacitor's model. Articles [4], [5] are focused on the measurement of all parameters in the model Fig. 1. In the following, the influence of time constants of RC branches on the linearity of DS-IADC will be analysed.

III. INFLUENCE OF DIELECTRIC ABSORPTION ON DS-IADC LINEARITY

Let us consider simplified structure of DS-IADC in Fig. 3. Time interval of the first phase is constant and equal to T_0. The second phase T_X is determined by the instant when output voltage from the integrator crosses back the zero level. This instant is registered by the voltage comparator and measured by the counter in the cascade.

In order to determine influence of absorption components on the linearity, all components in the structure are considered ideal except for the integrating capacitor. Here two parallel absorption RC components are considered. One RC branch represents absorption effect with the shortest time constant and the second RC circuit the dielectric absorption component with the maximal time constant.

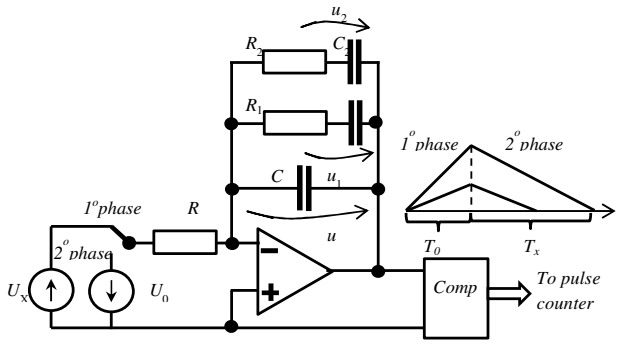

Fig. 3 Block diagram of DS IADC

The output voltage from the integrator is described by the system of linear differential equations:

$$\begin{bmatrix} u' \\ u_1' \\ u_2' \end{bmatrix} = \begin{bmatrix} -\frac{G}{C} & \frac{1}{R_1 C} & \frac{1}{R_2 C} \\ \frac{1}{R_1 C_1} & -\frac{1}{R_1 C_1} & 0 \\ \frac{1}{R_2 C_2} & 0 & -\frac{1}{R_2 C_2} \end{bmatrix} \begin{bmatrix} u \\ u_1 \\ u_2 \end{bmatrix} + \begin{bmatrix} b \\ 0 \\ 0 \end{bmatrix} \cdot \qquad (2)$$

Here conductivity $G = \left(R_1 R_2 + R_2 R + R_1 R\right) \Big/ R_1 R_2 R$ and $b_1 = U_x \Big/ CR$ in the first phase and $b_2 = -U_{REF} \Big/ CR$ in the second phase.

The output voltage at the integrator in the 1st and 2nd phase is described by the equation

$$\begin{aligned} u(t) &= A_1 t + A_2 e^{-B_2 t} + A_3 e^{-B_3 t} && \text{1.phase} \\ u(t) &= u(T_0) - (A_1 t + A_2 e^{-B_2 t} + A_3 e^{-B_3 t}) && \text{2.phase.} \end{aligned} \qquad (3)$$

The system of differential equations (2) can be solved analytically because of its linearity. Voltage $u(t)$ was calculated from the system (2) using symbolic programming environment "Octave". This programming tool allows us to avoid possible errors caused by the numerical integration in the known software simulators like "Cadence/PSpice" or "Multisim".

The nonlinearity $INL(k)$ of the ADC transfer characteristic was obtained as the difference between calculated time interval T_X and idealized time ${}^{i}T_X$. Ideal time interval was calculated as linear interpolation between time T_{Xmin} for smallest input voltage U_{Xmin} and T_{Xmax} for the voltage U_{Xmax} at the end of Full Scale Range (FSR). The code value k is calculated for DS-IADC as $k = \text{round}\left[2^N U_X \Big/ FSR\right]$ under assumption of resolution of N bits.

$$INL(k)=\frac{T_X-{}^iT_X}{{}^iT_X}100\%,\ \text{where}$$
$$ {}^iT_X=\frac{T_{X\max}-T_{X\min}}{U_{X\max}-U_{X\min}}\left(U_X-U_{X\min}\right)+T_{X\min}. \quad (4)$$

Here the $INL(k)$ represents nonlinearity after offset and gain error compensation. The offset error is realized by the auto-zeroing circuit [1], [2]. The gain compensation can be done by the adjustment of the input resistor R or by the digital post-processing.

IV. EXPERIMENTAL RESULTS

The mathematical model described by (2) was used for the evaluation of the absorption effects in real integrating capacitor. Absorption parameters of the capacitor Arcotronic MKP 470nF were determined from the decomposition of exponential components as described in [6]. Two dominant RC branches were represented by resistance R_1=470kΩ and C_1=23nF. Second absorption branch was represented by resistance R_2=22.7MΩ and C_2=4.7nF. Ideal capacity determined using identification of the main exponential component was C=478nF. The DA coefficient is DA=5.7% (Fig. 4). The upper trace shows the relation between input voltage U_x and time interval T_x of the second phase. The nonlinearity using Time-Voltage chart is difficult to observe. The conversion nonlinearity is more visible using the terminal definition of the $INL(U_x)$ (4). The nolinearity of the modelled DS-IADC with the capacitor Arcotronic MKP 470nF is shown on the lower trace in Fig. 4. Maximal nonlinearity in this case $INL_{max}\cong 1.5\%$ corresponds to the deviation of $\Delta k \cong 61$ for DS-IADC with 12 bit resolution. The nonlinearity error is out of acceptable limits.

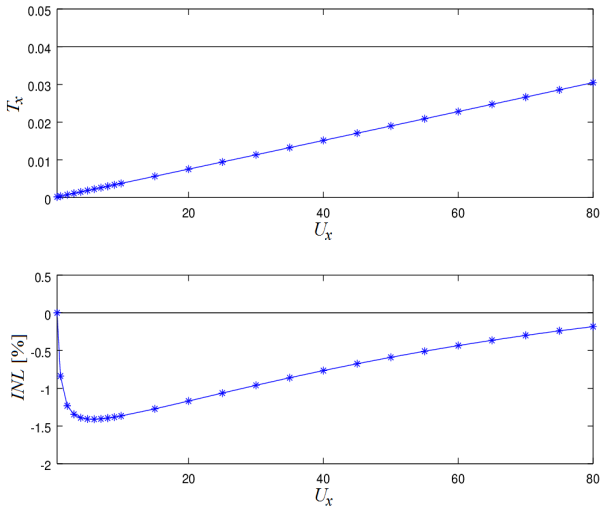

Fig. 4 Nonlinearity error of DS IADC with integrating capacitor Arcotronic MKP 470nF

The influence of the absorption effects on DS-IADC nonlinearity were analysed for another capacitor of the same technology, Vishay MKP 470nF. Its nominal capacity was the same C=470nF but the dielectric components were different: R_1=7.2MΩ and C_1=3nF. Second absorption branch was represented by resistance R_2=16MΩ and C_2=8.8nF. The dielectric absorption is DA=2.5 %

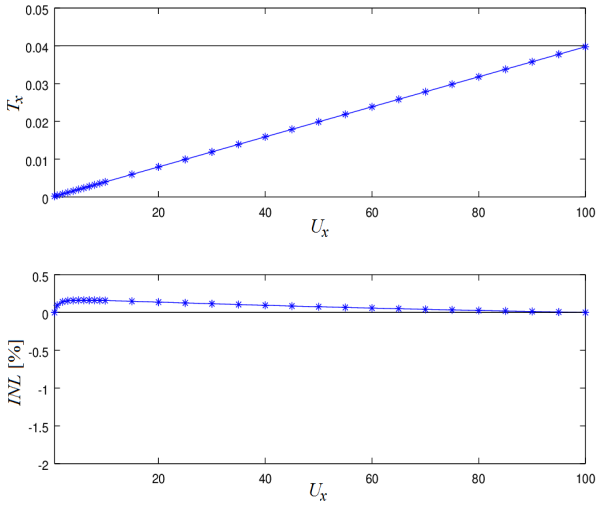

Fig. 5 Nonlinearity error of DS IADC with integrating capacitor Vishay MKP 470nF

Fig. 5 shows, that the shape of the nonlinearity of the DS-IADC is influenced not only by the technology and DA, but also by the ratio between the dipoles' time constants.

The influence of two absorption RC circuits on the final DS-IADC nonlinearity was studied by the mathematical model (2) under assumption of DA coefficient equal to 1%. The parasitic capacitors C_1, C_2 were modelled as equal. The capacity C for the study of influence of dipols' time constants on DS-IADC nonlinearity was supposed to be equal to C=1μF. The resulting capacities of absorption dipoles have been C_1=C_2=5nF under above mentioned assumptions. Time constants τ_1, τ_2 from the interval (1ms - 100ms) were determined by the serial resistances R_1 and R_2. Time interval of the first phase of the conversion procedure by DS-IADC was assumed T_0=40ms. The input resistance of the integrator was considered R=50 kΩ.

Three combinations of absorption elements were modelled. The first combination is represented by the resistance in the first RC branch R_1=20MΩ (τ_1=100ms) and R_2=10MΩ (τ_2=50ms). The analytical calculation of the final nonlinearity for the DS-IADC model (2) is shown in Fig. 6.a.

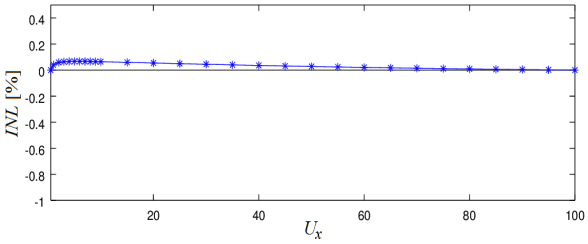

Fig. 6.a Nonlinearity error of DS IADC with DA=1% a time constants τ_1=100ms, τ_2=50ms

Second combination of absorption RC braches is represented by first RC branch R_1=200kΩ (τ_1=1ms) and R_2=10MΩ (τ_1=50ms) Fig. 6.b.

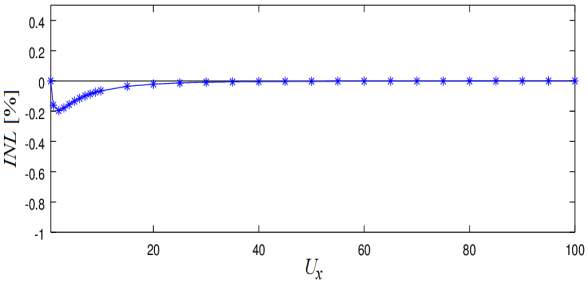

Fig. 6.b Nonlinearity error of DS IADC with DA=1% a time constants τ_1=1ms, τ_2=50ms

Third combination of modelled absorption RC braches for s is represented by first RC branch R_1=200kΩ (τ_1=1ms) and R_2=800kΩ (τ_1=2ms) Fig. 6.c.

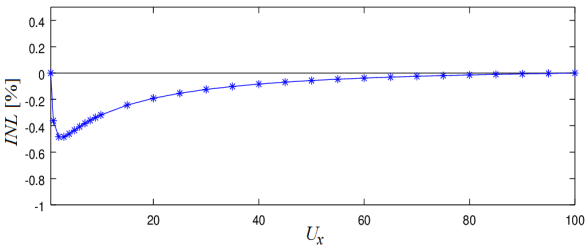

Fig. 6.c Nonlinearity error of DS IADC with DA=1% a time constants τ_1=1ms, τ_2=2ms

Previous simulations showed that there is an optimum in the dielectric absorption for the modelled circuit. In the case of modelled DS-IADC the optimal situation is represented by the resistance R_1=10MΩ and R_2=6MΩ. (Fig. 7)

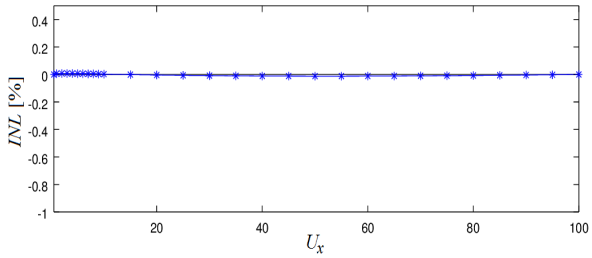

Fig. 7 Nonlinearity error of DS IADC with DA=1% a time constants τ_1=5ms, τ_2=3ms

V. CONCLUSIONS

Dielectric absorption of the integrating capacitor in the DS-IADC has considerable impact on the nonlinearity error. The maximal nonlinearity (4) of the simulated DS-IADC (Fig. 6.c) is INL_{max}= -0.5%. It corresponds to the maximal value of effective number of bits *ENOB*=8. This value is much smaller than maximal resolution of those converters defined by ADC producers. The guaranteed resolution for ICL7109 is equal to 12 bits. Careful selection of integrating capacitor as the only external component has to be taken in the consideration.

Simulation of the modelled integration capacitor with different time constants of the absorption RC branches showed that besides low value of dielectric absorption coefficient the time constants of those branches have significant influence on the final nonlinearity. Shorter time constants than the integration intervals T_0 and T_x in both phases have higher impact on the final nonlinearity error even for quite large dielectric absorption coefficient DA. Longer time constants have lower influence on the final nonlinearity error especially for the smaller values of input voltage.

The performed study showed that the information about the absorption coefficient is not sufficient enough for the selection of the integrating capacitor. Beside knowledge of DA coefficient, the circuit designer has to know even the parasitic components representing dielectric absorption of integrating capacitor utilized in DS-IADC. If the time constants of parasitic RC branches are significant, the integration intervals T_0 and T_x could be adapted to their values.

VI. ACKNOWLEDGMENT

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