

New hardware interface to synchronize stand-alone measurement instruments

Francesco Lamonaca, Domenico Luca Carnì, Domenico Grimaldi

*Dept. of Computer Science, Modeling, Electronics and System Science,
University of Calabria, Rende (CS) Italy
(dlcarni@dimes.unical.it)*

Abstract – The Measurement Instruments (MIs) connected by Hardware Interface (HI) to the node of the Distributed Measurement System (DMS) can coordinate their operations by synchronized trigger signals sent from the HIs to MIs. In the research it is taken into consideration the case that the HIs cannot be connected to DMS and, then, the MIs are standalone.

With this aim a new architecture of HI is proposed for the synchronous triggering of the MI. The proposed architecture avoids the random effects of concurrency of the software processes running on PC, and reduces the random causes of delay to detect the trigger condition. From the analysis of the HI the model of the synchronization time delay is pointed out, including the opening time of the hardware components. This model permits to evaluate the effects of each cause affecting the execution of the trigger command.

I. INTRODUCTION

Synchronized measurement is a new service achievable by Distributed Measurement Systems (DMSs) [1-3]. Usually, the Measurement Instrument (MI) is interfaced to the node of the DMS by Hardware Interface (HI) and the synchronization procedure operates on the clock, internal or external, of this last. The MIs can coordinate their operations by synchronized trigger signals sent from the HIs to MIs.

The synchronization procedure needs that all the nodes communicate to share common synchronization signal or message packets to adjust their clock.

The synchronization service is not available if the network's topology doesn't provides continuous, reliable and stable link, wired or wireless, to whole network [1-3]. In this cases the MIs are standalone and the synchronization among them is an open problem.

The solution based on GPS signal [3] is not always suitable for indoor scenarios.

In this paper, a new architecture of HI is proposed to synchronize standalone MIs. In particular, all the HIs are synchronized among them without connection to the DMS and, successively, each HI is brought to the MI for

the synchronous triggering. To this aim the HI is equipped with tuneable clock that is synchronized before the connection HI-MI and the measurement procedure. The hardware architecture of HI is designed to (i) avoid the random effects of concurrency of the software processes running on PC, and (ii) reduce the random causes of delay to detect the trigger condition [4, 9].

The model of the synchronization time delay between the operations executed by two MIs, each one equipped by the HI, is pointed out. The model permits to evaluate the influence of each component of the HI on the synchronization accuracy.

The paper is organized as follows. The hardware architecture and the logical operations performed by the new proposed HI are presented. Successively, the model of the synchronization time delay of the proposed HI is pointed out. Finally, the conclusions are drawn.

II. HARDWARE INTERFACE ARCHITECTURE

Fig.1 shows the hardware architecture of the proposed HI connecting the MI.

It is constituted by: (i) PIC16F84a, (ii) 8-bit Counter block, (iii) Clock block equipped by 10MHz temperature compensated crystal oscillator, and (iv) board Rabbit RCM4400W.

A Triggering operation

The board Rabbit RCM4400W receives from the Master PC on the WiFi interface the information about the *trigger condition* to execute the triggering of the MI, and transmits it on the serial interface, pin D, to the PIC. The software running on the PIC checks the *trigger condition* by means of the interrupts arising from the Counter block, and sends the *trigger signal* to the MI by rising the signal on the pin RB1. The Clock block is used as reference clock to temporize with high accuracy the Counter block and, as a consequence, the command execution into the PIC.

The Counter block is used as frequency divider. Indeed, because the Clock block has frequency equal to 10MHz and the number of bit of the Counter block is 8bit, the PIC receives the interrupt each 25.6 μ s, while the elementary operations to check the trigger condition are performed by the PIC in 12.5 μ s. In this way the end of

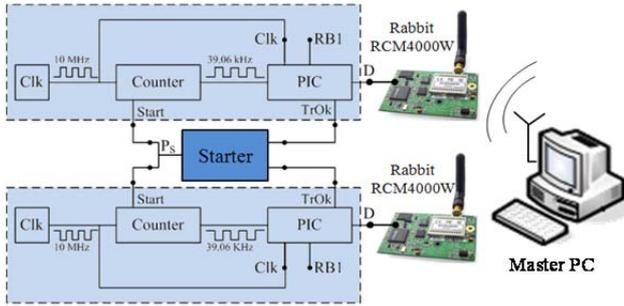


Fig. 1. Block scheme of the proposed HI.

performed operations is guaranteed before the successive interrupt occurs.

B. Synchronization of the Counter block

The two pins TrOk and Start are used to perform the synchronization of the Counter blocks of two different HIs by means of the external Starter block, as shown in Fig.1.

The Starter block is constituted by two latches and one port AND. While each input of the Starter block does not receive the high signal level from the pin TrOk of the two HIs, the signal at the pin Ps is low. Once received all the agreements, the output signal at the pin Ps is high. This signal is also used to reset the Starter latches.

On each HI, latch is connected to the pin Start of the Counter block to ensure the correct functioning, once the Starter block is disconnected.

III. SINCRONIZATION OF STANDALONE MEASUREMENT INSTRUMENTS BY THE PROPOSED HI

The synchronization involves, Fig.1, the Master PC to

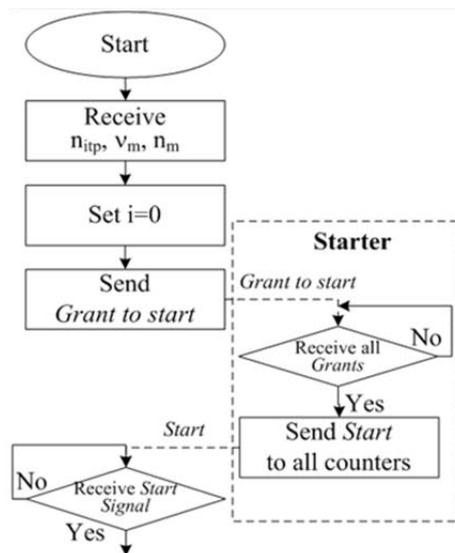


Fig. 2. Block diagram of the performed operation by HI for the synchronization.

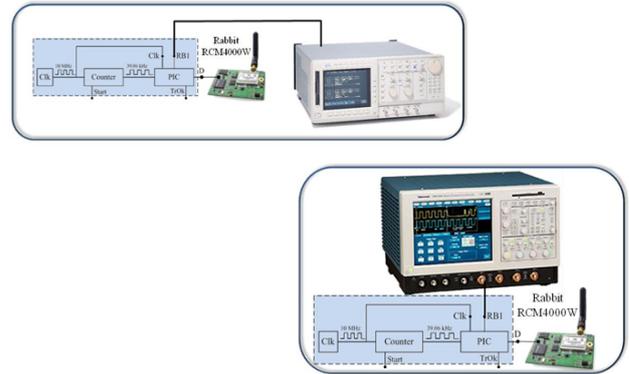


Fig. 3. Block scheme of the connection of the HIs to standalone MIs.

send the trigger condition at each HI, and the external Starter block to synchronize the start of the counting between two HIs.

Fig.2 shows the block diagram of the performed operations for the synchronization between two HIs.

The trigger condition corresponds to the number $n_c = n_{\text{ipp}} 2^N$, with n_{ipp} number of interrupts that the PIC must to count before the execution of the command for the MI, and N bit number of the Counter block. The Master PC evaluates n_{ipp} according to the frequency of the Clock block and the bit number of the Counter block. The Master PC sends, also, the information concerning with the number of repetitive measures n_m with period v_m . In the case only one measure is requested $n_m = 1$. Once set into the PIC the internal variable n_{ipp} , n_m , v_m , the HI is ready. Therefore, it sends to the Starter block the grant to start signal by rising the voltage level on the pin TrOk (Fig.1).

Once received all the grants, the Starter block sends to the two Counter blocks the signal *Start to count*, by rising the voltage on the pin Ps. Each HI receives this signal in parallel modality. The time delay between the gate opening of the two Counter blocks depends on the hardware characteristics of the components. The interrupt sent by each Counter block forces the corresponding PIC to operate in synchronized modality.

Once the Counter block starts, each HI can be:

- disconnected from the external Starter block,
- moved to the measurement place,
- connected to the MI.

Fig.3 shows the block scheme of the connection of the HIs to stand alone MIs. The standalone MIs receive synchronized trigger signals by the HIs.

During this operation mode, each PIC receives the interrupt from the Counter block in synchronized modality with other PICs.

The operations performed by the PIC at each interrupt are (Fig.4):

- (i) the internal variable i is incremented,
- (ii) when i equal to n_{ipp} , HI sends the trigger

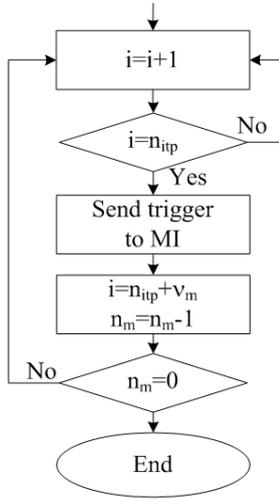


Fig. 4. Block diagram of the performed operation by HI into the Operative Phase.

signal to the MI by the pin RB1, and the new values are upgraded $n_{itp}=n_{itp}+v_m$, $n_m=n_m-1$.

- (iii) if $n_m=0$, the measurement procedure is considered done and the PIC is waiting for the new trigger condition.

IV. MODEL OF THE RANDOM VARIATION OF THE SYNCHRONIZATION DELAY IN HI

The synchronization time delay ΔT between the operations performed by two MIs, each one equipped by the HI shown in Fig.1, is:

$$\Delta T = \left(n_{c1} \frac{1}{f_{c1}} - n_{c2} \frac{1}{f_{c2}} \right) + \left(n_{p1} \frac{1}{f_{p1}} - n_{p2} \frac{1}{f_{p2}} \right) + O_C + O_P + E_P; \quad (1)$$

where f_{c1} oscillator frequency of HI#1 equipping the MI#1, f_{c2} oscillator frequency of HI#2 equipping the MI#2; f_{p1} and f_{p2} oscillator frequency of PIC#1 and PIC#2, respectively; n_{c1} and n_{c2} counting number of HI#1 and HI#2, respectively; n_{p1} and n_{p2} number of elementary operations to execute the procedures on PIC#1 and PIC#2, respectively; O_C start offset time between the Counter on HI#1 and that on HI#2, O_P start offset time between two PICs, E_P delay time introduced by the hardware of the two PICs to rise the voltage level of the trigger signal for the MI.

O_P can be neglected because the following condition

occurs: the storage of the internal variable n_c , n_m , v_m into each PIC ends before the incoming of the first interrupt signal generated by the associated Counter. Indeed, the external Starter block sends the start to count signal to the two Counters once received the grant to start signals by both the PICs.

Under the condition that the PIC performs the operations to check the trigger condition before of the successive incoming interrupt, it is possible to assess that the delay to perform the operation is not influenced by the previous interrupt delay. Therefore, the operations taken into account in n_{p1} and n_{p2} are the following:

- (i) the internal counter is incremented,
- (ii) the occurrence of the trigger condition is checked,
- (iii) the trigger procedure is executed.

The variation of the synchronization time delay (1), evaluated according to the considerations given in [10], is:

$$u_{\Delta T} = \sqrt{\left(\left(-n_{c1} f_{c1}^{-2} \right) \Big|_{x} u_{f_{c1}} \right)^2 + \left(\left(n_{c2} f_{c2}^{-2} \right) \Big|_{x} u_{f_{c2}} \right)^2 + u_{O_C}^2 + \left(\left(n_{p2} f_{p2}^{-2} \right) \Big|_{x} u_{f_{p2}} \right)^2 + \left(\left(-n_{p1} f_{p1}^{-2} \right) \Big|_{x} u_{f_{p1}} \right)^2 + u_{E_P}^2} \quad (2)$$

where $u_{f_{c1}}$, $u_{f_{c2}}$, uncertainty of f_{c1} , f_{c2} , respectively, $u_{f_{p1}}$, $u_{f_{p2}}$, uncertainty of f_{p1} , f_{p2} , respectively, and u_{O_C} variation of O_C . u_{E_P} variation of E_P and represents the uncertainty of the synchronization time delay introduced by the hardware of the two PICs to rise the voltage level of the pin RB1 to control the MI.

The (2) is valid in both absence of conditional jump and correlation between parameters. Indeed, the conditional jump modifies the number of operations, n_{p1} and n_{p2} , to be executed on the basis of the particular event.

In the case under examination, it is assumed:

$$\begin{cases} f_{c1} = f_{p1} \\ f_{c2} = f_{p2} \end{cases} \quad (3)$$

according to the block scheme of Fig.1. Moreover, for synchronization purpose can be imposed $f_{c1}=f_{c2}=f_c$, and $n_{c1}=n_{c2}=n_c$. Because the PIC#1 and PIC#2 execute the same procedure, it is $n_{p1}=n_{p2}=n_p$.

In order to evaluate u_{O_C} , the parameters defining the offset O_C must be defined. O_C depends on the difference between the two time intervals, shown in Fig.5. In particular, for each HI the time interval is starting from the incoming of the positive slope of the signal feed by the pin Ps of the Starter Block and is ending at the effective start to count.

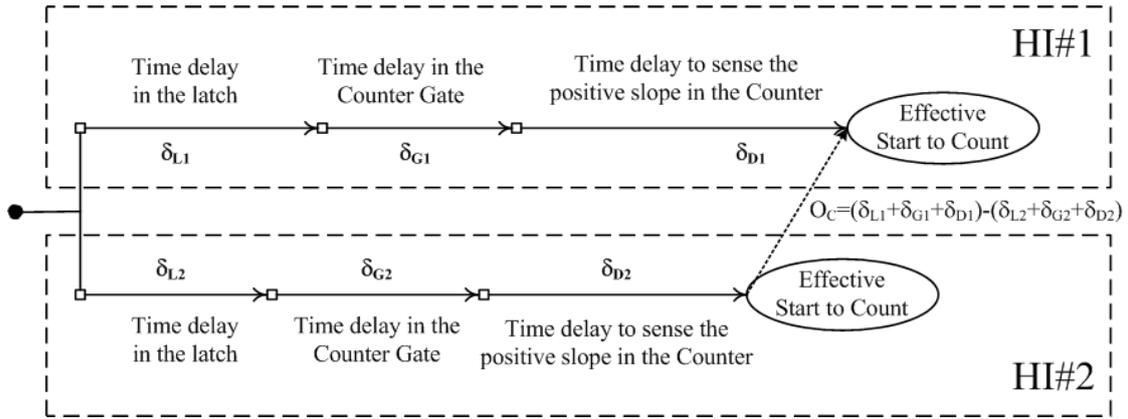


Fig. 5. Time interval starting from the incoming of the positive slope of the signal feed by the pin Ps of the Starter Block and ending at the effective start to count for each HI.

Each time interval is the sum of:

- 1- time delay δ_L between the incoming of the positive slope of the signal feed by the pin Ps of the Starter Block to the Latch and the one fed by the Latch to the Counter's Gate,
- 2- time delay δ_G between the incoming of the signal fed by the Latch and the effective Counter's Gate opening,
- 3- time delay δ_D between the effective Counter's Gate opening and the incoming of the positive slope of the signal fed by the Clock (Effective start of count).

Therefore, it is:

$$O_C = (\delta_{L1} + \delta_{G1} + \delta_{D1}) - (\delta_{L2} + \delta_{G2} + \delta_{D2}) \quad (4)$$

In Fig.5 the different length between δ_{L1} and δ_{L2} , δ_{G1} and δ_{G2} , respectively, highlights the random effect of the hardware components. The different length between δ_{D1}

and δ_{D2} depends on the different phase of the Clock signals.

In particular, the data sheet of the hardware component furnishes the information about the variation range of δ_L and δ_G . In general, δ_L and δ_G can be assumed uniformly distributed in the variation range. Therefore, the corresponding standard deviation (u) can be evaluated according to [10] by $u = \Delta/(2\sqrt{3})$ where Δ is the width of the variation range.

In order to evaluate the variation range of δ_D , Fig.6 shows two typical cases. In the case a), the Counter block receives the positive slope of the signal generated by the Clock after dt_1 from the opening of the Counter's Gate. Therefore, the Counter will count with delay equal to $\delta_D = dt_1$ respect to the opening of the Gate. In the case b), the Counter receives the positive slope of the signal generated by the clock after $\delta_D = f_c^{-1} - dt_2$, $dt_2 < f_c^{-1}$ is the time interval between the positive slope of the signal and the Counter's Gate opening. Therefore the Counter will

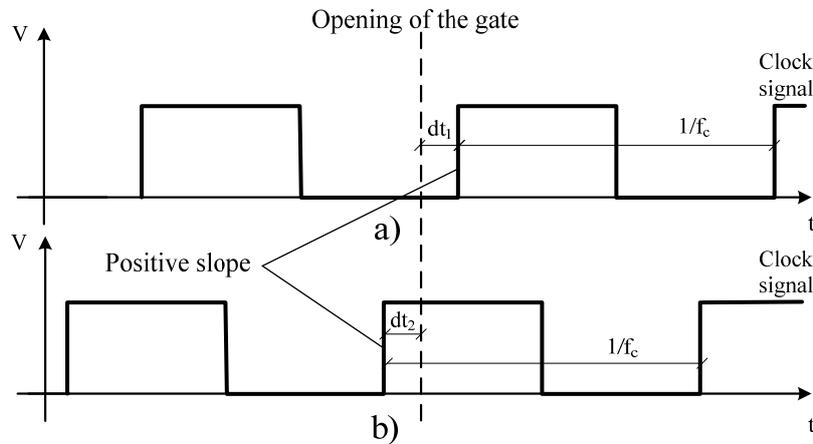


Fig. 6. Delay between the opening of the Counter's Gate and the effective start to count.

a) best case, the gate opens dt_1 before the positive slope of the signal ($\delta_D = dt_1$),

b) worst case, the gate opens dt_2 after the positive slope of the signal ($\delta_D = f_c^{-1} - dt_2$).

count with a delay equal to δ_{D2} respect to the synchronized Gate opening.

The evaluation of u_{oc} can be obtained from (4) by taking into consideration the variation of the single parameters.

V. CONCLUSIONS

A solution based on embedded HI is proposed for the synchronous triggering of standalone MIs.

The HIs are synchronized before the connection HI-MI.

The HI is designed to (i) avoid the random effects of concurrency of the software processes, and (ii) reduce the random causes of delay to detect the trigger condition [4, 9].

The hardware architecture and the logical operations performed by the proposed HI are discussed.

The model of the synchronization time delay between the operations executed by two MIs, each one equipped by the HI is given. The model permits to evaluate the influence of the HI components on the synchronization accuracy among the operations performed by the MIs.

ACKNOWLEDGMENT

This work was partially supported by the Italian grant RIDITT, project DI.TR.IM.MIS "Diffusion and transfer of technologies to companies working in the field of measurements", funded by the Italian Ministry of Economic Development.

REFERENCES

- [1] J. H. Cho, H. Kim, S. Wang, J. Lee, H. Lee, S. Hwang, *et al.*, "A Novel Method for Providing Precise Time Synchronization in a Distributed Control System Using Boundary Clock", *IEEE Transactions on Instrumentation and Measurement*, vol. 58, pp. 2824-2829, 2009.
- [2] M. Aiello, A. Cataliotti, V. Cosentino, and S. Nuccio, "Synchronization Techniques for Power Quality Instruments", *IEEE Transactions on Instrumentation and Measurement*, vol. 56, pp. 1511-1519, 2007.
- [3] A. Carta, N. Locci, and C. Muscas, "GPS-Based System for the Measurement of Synchronized Harmonic Phasors", *IEEE Transactions on Instrumentation and Measurement*, vol. 58, pp. 586-593, 2009.
- [4] F. Lamonaca, D. Grimaldi, and R. Morello, "Dynamic Scheduling of Trigger Command for sub- μ s Alignment Accuracy in Distributed Measurement System", *IEEE Transaction on Instrumentation and Measurement*, vol. 63, pp. 1795 - 1803, 2014.
- [5] F. Lamonaca and D. Grimaldi, "Trigger Realignment by Networking Synchronized Embedded Hardware", *IEEE Transaction on Instrumentation and Measurement*, vol. 62, pp. 38-49, 2013.
- [6] F. De Rango, A. Perrotta, "Performance evaluation of two slot assignment strategies under distributed TDMA MAC protocol over mobile ad hoc networks," Proc. of IEEE 73rd Vehicular Technology Conference, VTC2011-Spring, Budapest, Hungary, 15-18 May 2011.
- [7] F. Lamonaca, A. Gasparri, E. Garone, D. Grimaldi, "Clock Synchronization in Wireless Sensor Network with Selective Convergence Rate for Event Driven Measurement Applications", *IEEE Transaction on Instrumentation and Measurement*, 2014. DOI:10.1109/TIM.2014.2304867. ISSN:0018-9456.
- [8] E. Garone, A. Gasparri, F. Lamonaca, "Clock Synchronization for Wireless Sensor Network with Communication Delay", Proc. of American Control Conference, June 17 - 19 2013, Washington, DC, pp. 771-776. ISSN: 07431619 ISBN: 978-147990177-7.
- [9] F. De Rango, A. Panzarella, S. Marano, "Controlled interference mitigation MAC for UWB networks with quality of service support," Proc. of IEEE International Conference on Mobile Adhoc and Sensor Systems, MASS, Pisa, Italy, 8-11 Oct. 2007.
- [10] International Organization for Standardization, Guide to the Expression of Uncertainty in Measurement (GUM), 1998.