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Voltage Source Inverters: an Easy Approach for Fast Fault Detection

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Abstract- This paper presents a novel fault detection algorithm for fault-tolerant converters. In the algorithm analysis, based on a simple geometrical approach, both the case of faults in single device and the loss of an entire inverter leg have been considered. The proposed fault detection algorithm is characterized by simplicity, low computational and implementation effort and easy control integration. The proposed algorithm is verified by means of experimental results and reveals a valid and suitable alternative to the actual state of the art in the field of inverter fault detection.

I. Introduction

Recent studies in power electronics reliability have shown that, in the field of variable frequency electrical drives, up than the 80% of faults are to be ascribed to single or multiple silicon device failures [1]. Diagnostic systems on converters and electrical motors [2-3] are nowadays of particularly importance renewable energy sources integration [4-6]. Typically these failures are caused by counterblow destruction as in the case of short circuit of silicon packed devices, by losing driver pulse occurring if driver circuit or power supply are invalid so that no trigger pulse can be sent to the gate of the power device, and, finally, by open circuit failure that heavily affects the output voltages and currents waveforms [7-10]. Open-circuit faults generally do not cause shutdown of the system, but degrades its performance. Therefore, diagnostic methods can be used to device fault- tolerant systems, which continue working even with faults but at reduced capacity. The short-circuit faults, instead, are difficult to deal with, because the time between the fault initiation and failure is very small. In many short-circuit failure conditions, the time between the fault initiation and the device failure is very short. The devices can withstand abnormal currents up to around 10 μs. Therefore, most of the existing devices short-circuit detection and protection methods are hardware circuit based and very few are algorithm based [11]. The rapid intervention of ultra-rapid protection fuses, in general, causes the short-circuit fault to evolve rapidly into a corresponding open-circuit fault. For this reason, more attention has been given to the open-circuit fault diagnosis.

Fault-tolerance of power converters has gained a growing attention in the last years and several fault-tolerant topologies for power converters and drives were proposed with the support of both simulation and experimental results. Their advantage in limiting voltages and currents floating-off have been subject of long discussions, but none of the proposed solution can actually be dictated as the universal one. Furthermore each of them is strongly connected to the case in which it is applied. However, a really capital part of the fault- tolerant operation of a power converter is the algorithm of fault detection. A fault detection algorithm should be fast enough to avoid the total destruction of the power device (evidently with the aid of additional protections); it should require a small implementation effort and the smallest number of additional sensors in order to be as cheaper as possible [12] and a full integration with the reconfiguration algorithm for fault-tolerant operation (if present).

II. The existing approaches

Many fault detection methods have been proposed in the technical literature. Among the most cited fault detection method there are: the Park's vector method suggested for the first time in [13]; the normalized Park's vector method; the direct current method.

The Park's vector method analyses the average values of the current space vector in the complex plane and collects information for the precise fault localization by using the absolute value and the phase of the current vector. This method is really effective, but presents the drawback to be load- dependent. For this reason, [14] suggests a modified version in which only the normalized Park's vector is used.

The direct current method proposed in [15] exploits the symmetrical current components and in particular the direct component for diagnosis purpose.

Many other fault diagnosis methods have been investigated. Some of them have been explicitly concerned to the disruption phenomena inside the IGBTs device packaging. All of the proposed methods are referred to a specific

application such as electrical AC drives, electric vehicles and distributed generation. Finally, [16] proposes a really fast algorithm for a precise fault detection in a particular converter topology used as an active filter. The algorithm results to be effective in less than 20 μs.
In this paper the authors present a novel fault detection algorithm integrated in the control of a fault-tolerant voltage source inverter. The presented algorithm approaches the problem of fault detection in a manner similar to that of the current Park's vector but with a lesser computational effort and an easier integration in the control of the fault-tolerant inverter. Furthermore it is not linked to any particular application.

III. The proposed approach

To describe the proposed fault detection algorithm, it is useful to analyse two cases:

- following the fault of a single device, an entire leg of the inverter is disconnected. This may happen if the fault rapidly propagates to the second device of the leg, as in the case of a packaged module or for the intervention of fast fuses or other protections. For the loss of an entire leg, the current on the faulted phase vanishes;
- only a single device fault and the current in the faulted phase can circulate only for an half wave closing its pattern through the freewheeling diode and/or in the second device of the leg. The fault condition can persist long enough causing a degradation in performance.

In the first case, before the fault, the load current space vector follows a circular trajectory with a superimposed ripple. After the fault the current of the faulted phase is completely loosen and for insulated neutral loads the current of the residual phases are in opposition; for instance, by supposing that current of phase A vanishes:

$$\begin{cases} i_A = 0 \\ i_B = I_x \sin(\omega t) + r(t) \\ i_C = -I_x \sin(\omega t) - r(t) \end{cases} \tag{1}$$

in which I_x is the current peak value and *r(t)* is a function describing the current ripple. By transforming the current in a fixed reference frame with the matrix transformation:

$$T = \sqrt{\frac{2}{3}} \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{pmatrix} \tag{2}$$

The transformed current vector in the case considered in (1) becomes:

$$\boldsymbol{i}_{Fault-A} = \begin{pmatrix} 0 \\ \sqrt{2} I_x \sin(\omega t) + \sqrt{2} r(t) \\ 0 \end{pmatrix} \tag{3}$$

and for fault on B and C phase respectively:

$$\boldsymbol{i}_{Fault-B} = \begin{pmatrix} -\frac{\sqrt{3} I_x \sin(\omega t) + \sqrt{3} r(t)}{\sqrt{2}} \\ -\frac{I_x \sin(\omega t) + r(t)}{\sqrt{2}} \\ 0 \end{pmatrix} \tag{4}$$

and:

$$\boldsymbol{i}_{Fault-C} = \begin{pmatrix} \frac{\sqrt{3} I_x \sin(\omega t) + \sqrt{3} r(t)}{\sqrt{2}} \\ -\frac{I_x \sin(\omega t) + r(t)}{\sqrt{2}} \\ 0 \end{pmatrix} \tag{5}$$

The conditions to diagnose the faults may be so synthesized as follows:

$$\begin{cases} i_\alpha = 0 & \text{faulted phase is A} \\ i_\alpha = \sqrt{3} i_\beta & \text{faulted phase is B} \\ i_\alpha = -\sqrt{3} i_\beta & \text{faulted phase is C} \end{cases} \tag{6}$$

i.e. in the case of complete phase fault the currents Park's trajectory becomes a line whose slope allows to determine which of the three phases is the really faulted. It is worthwhile to remark that (6) does not depend on the ripple amplitude *r(t)* neither on the peak current value so that fault diagnosis is not affected by the nature or the magnitude of the load. To make the fault detection more reliable and robust, the relations (6) have to be rewritten as follows:

$$\begin{cases} |i_\alpha| \leq \epsilon & \text{faulted phase is A} \\ |\sqrt{3} i_\beta - i_\alpha| \leq \epsilon & \text{faulted phase is B} \\ |\sqrt{3} i_\beta + i_\alpha| \leq \epsilon & \text{faulted phase is C} \end{cases} \qquad (7)$$

where the parameter ε introduce a security bandwidth taking into account the current measurement uncertainties. This bandwidth can be chosen narrow enough after the measurement uncertainty evaluation [17-18].

In the second case, the current in the faulted phase can circulate during a half wave as said before. Supposing that a fault happens in the upper device the currents circulates in the freewheeling diode and in the other unfaulted power device. In this case the current expression (only for the half period in which it can circulate) can be summarized as follows:

$$\begin{cases} i_A = I_x \sin(\omega t) + r'(t) \\ i_B = I_x \sin(\omega t - \frac{2}{3}\pi) + r'(t) \\ i_C = I_x \sin(\omega t + \frac{2}{3}\pi) + r'(t) \end{cases} \qquad (8)$$

where $r'(t)$ is a different current ripple function. In the other half period the expression is given by (1). The current Park vector has the following expressions:

$$\boldsymbol{i}_{Park} = \begin{pmatrix} \frac{\sqrt{3} I_x \sin(\omega t)}{\sqrt{2}} \\ -\frac{\sqrt{3} Ix \cos(\omega t)}{\sqrt{2}} \\ \sqrt{3} r'(t) \end{pmatrix} \qquad (9)$$

for the first half, where r'(t) appears only to be a zero sequence component and one among (3), (4) or (5) for the second half, whichever is the faulty phase. The conclusion is that the Park's current vector trajectory in this case is composite, being a circle during an half wave and a line whose slope depends on the faulted phase in the residual half wave period so that the (7) are to be applied.

In order to include both cases the fault detection algorithm considers the sampled currents, and in particular if N is the number of current samples per period, the fault is really present if the relations (7) are satisfied for a $N/2-2$ samples at most. The number $N/2-2$ is chosen for security reason by excluding the samples near the zero crossing of the currents, but a smaller number of pulses may be chosen in order to reduce time consuming. The choice of counting samples however allows avoiding a false positive test that can occur for a transient losing of driver pulses that not necessarily conduct to a disruptive fault. Figure 1 shows the flow chart of the proposed fault detection algorithm.

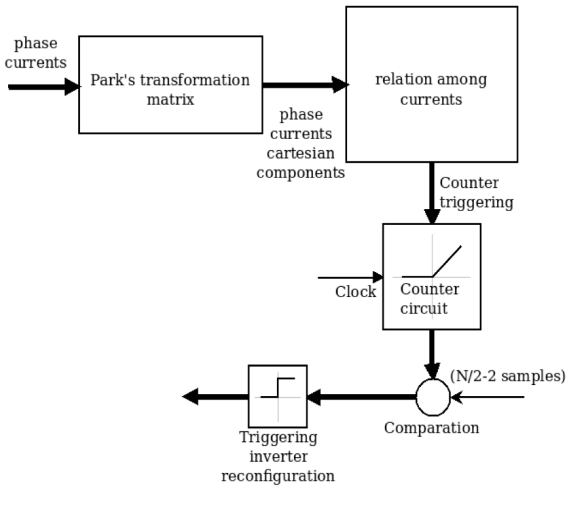

Figure 1. Flow chart of the proposed fault detection algorithm

IV. Experimental results

For the experimental verification of the proposed fault detection algorithm, a test bench based on an INFRANOR power converter, an induction motor and a dSPACE 1103 control board has been built and set up.

The system constitutes an induction motor electrical drive fed by a fault-tolerant inverter with non-redundant topology as shown in Figure 2. The converter used in the test bench is a commercial frequency converter whose control board has been replaced by a customary one designed to be driven by the dSPACE control board and a hardware interface for converting the TTL gating pulses to the “line drive” type of the INFRANOR converter.

The fed induction motor is a two poles three phase squirrel cage with 5.5 kW rated power, 2870 rpm rated speed, 50 - 60 Hz rated frequency, 18.3 Nm rated torque, 400 V rated voltage, 13 A rated current.

The motor speed is controlled with a simple constant V/f strategy.

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A digital Yokogawa oscilloscope with two differential probes (DC up to a 25 MHz bandwidth) and 3% accuracy have been used to register voltage and currents waveforms. Given the nearness of the inverter, an analysis of the electromagnetic immunity of the measurement system has been carried out [19-20].
Measurements data were stored in the host computer of the dSPACE board and plotted with the help of "Waveforms Viewer" software package.
Fault emulations have been realized with the help of solid state relays and connectors being driven from the dSPACE board and its software interface. In this way it was possible to test the behaviour of the fault-tolerant converter in all possible condition without a real disruption of the power devices (see Figure 3 for the solid state relay circuit).
Several tests have been made at different voltage and frequency values and at different PWM frequency in order to verify the effectiveness of the fault detection algorithm in various operating conditions.

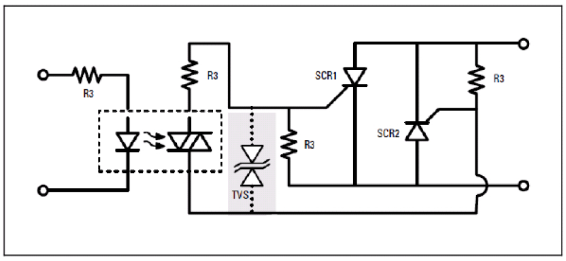

Figure 3. Solid state relay for the fault emulation

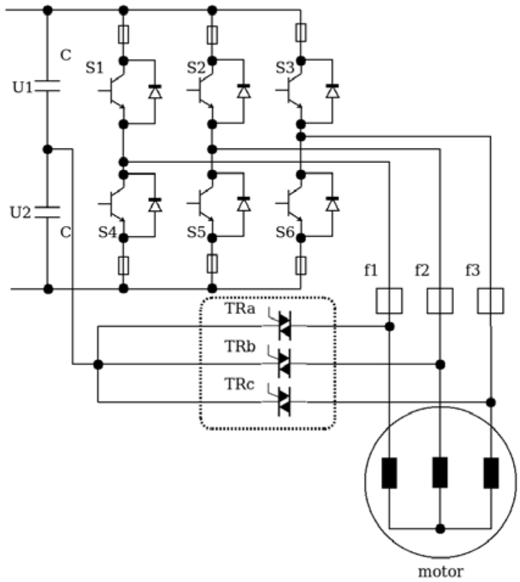

Figure 2. The non-redundant topology of fault-tolerant inverter

Figures 4 and 5 show different patterns for phase voltage before and after fault both for faulty and unfaulty phase. These patterns confirm the correct fault-tolerant operation of the control system in the inverter.

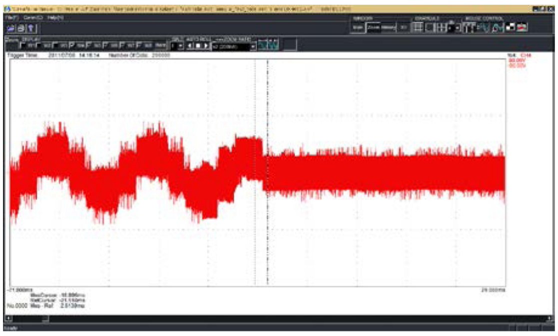
Figure 4. Fault emulation at 50 Hz, reference voltage 60 V, f_{PWM} = 10 kHz; voltage before and after fault on faulted phase

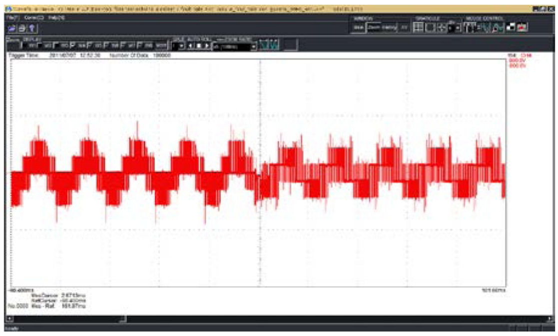
Figure 5. Fault emulation at 50 Hz, reference voltage 60 V, f_{PWM} = 10 kHz; voltage before and after fault on unfaulted phase

Figure 6 shows the pattern of phase current before and after the fault. In the zoomed section at the bottom it is evident the time in which the current interruption after fault occur and the restoring after the he fault detection and the start of inverter reconfiguration.
Figures 7 and 8 shows voltage at faulty phase and currents before and after the fault emulation with a reference voltage V = 100 V, f = 50 Hz and f_{PWM} = 20 kHz.
All the reported figures show that at different operating conditions the behaviour of the inverter and of the detection algorithm does not change substantially when the reference voltage change and the PWM frequency

assumes different values. A small difference in the current ripple may be noted before and after fault, that is natural considering how the number of switching after fault has changed. In general, as experimentally demonstrated in many different technical papers after faults and reconfigurations a growth in the current ripple this change in the ripple is less evident if the switching frequency is high that is due to the filtering effect of the load in a wider frequency range.

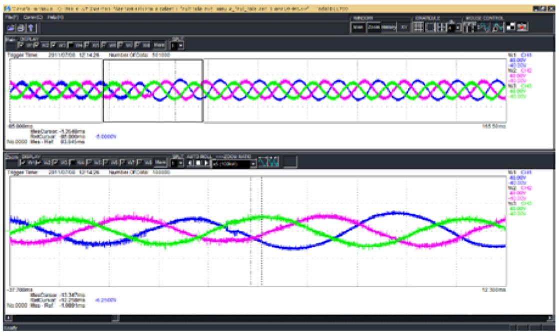

Figure 6. Currents before and after faults - long registration and zoom near the fault instant

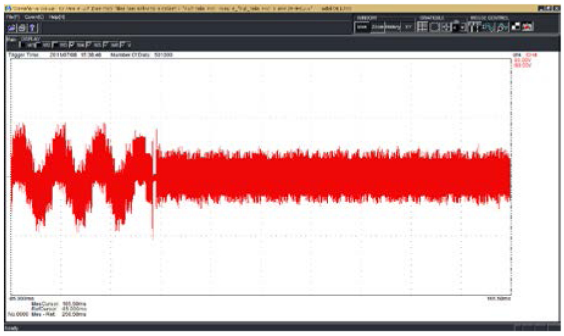

Figure 7. Voltage at faulty phase before and after the fault emulation with reference voltage 100 V, f = 50Hz and f_{PWM} = 20 kHz

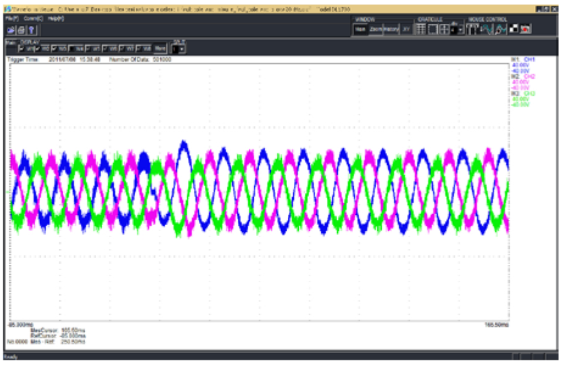

Figure 8. Load currents before and after the fault emulation with reference voltage 100 V, f = 50 Hz and f_{PWM} = 20 kHz

V. Conclusions

In this paper a novel fault detection algorithm have been presented, discussed, and verified via experimental results. The proposed fault detection algorithm is characterized by simplicity, low computational and implementation effort with a consequent enough fast execution, easy control integration with the possibility to use it both in hardware in the loop systems and microprocessor of common industrial usage. The algorithm is based on a geometrical approach on the trajectory of the Park's current vector following a consolidated technical literature, with some different issues in order to reduce the computational burden and to increase reliability in the fault detection. In the algorithm analysis both the case of fault in single device and the loss of an entire inverter leg have been considered, furthermore false positive detections due to losing pulse drive are avoided by considering a pre-fixed number of current samples before reconfiguration.

As a matter of fact, a prudential number of pulses has been considered for this goal but a more comprehensive statistical investigation on the faults in different conditions should reduce the number of pulse for which eq. (7) are to be verified before the system reconfiguration so reducing the time of fault detection that in each case does not overcome 10 ms. This values may be considered as a good time for systems to whom no particular performance is required and however it may be considered sufficient to avoid a back propagation of the fault effects and is smaller than the time of fault detection of the main algorithms presented in previous papers. The presented algorithm is a valid and suitable alternative to the actual state of the art in the field of inverter fault detection with the further advantage of an easy integration in the control system of a fault-tolerant inverters.

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