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Using an IEEE1149.1 Test Bus for Fault Diagnosis of Analog Parts of Electronic Embedded Systems

Zbigniew Czaja[1], Bogdan Bartosinski[2]

[1] Gdansk University of Technology, Faculty of Electronics, Telecommunications and Informatics, Department of Metrology and Optoelectronics, ul. G. Narutowicza 11/12, 80-233 Gdansk, Poland, phone 48 58 347-14-87, fax 48 58 347-13-57, e-mail zbczaja@pg.gda.pl
[2] Gdansk University of Technology, Faculty of Electronics, Telecommunications and Informatics, Department of Metrology and Optoelectronics, ul. G. Narutowicza 11/12, 80-233 Gdansk, Poland, phone 48 58 347-15-37, fax 48 58 347-13-57, e-mail bbart@eti.pg.gda.pl

Abstract-The new solution of a BIST called the JTAG BIST for self-testing of analog parts of electronic embedded systems is presented in the paper. The JTAG BIST consists of the BCT8244A and SCANSTA476 integrated circuits of Texas Instruments controlled via the IEEE 1149.1 bus. The BCT8244A is a scan test device with octal buffers, and the SCANSTA476 is a 12-bit ADC with 8 analog input channels. Self-testing approach is based on the fault diagnosis method in which we stimulate the tested analog part by the single square pulse using the BCT8244A and we sample the time response of the analog part two times by the SCANSTA476. The measurement results are used for fault detection and also a single soft fault localization of the analog part.

I. Introduction

For many years the IEEE 1149.1 (JTAG) standard [1] has been used on electronic boards and systems for digital and structural test access. Now, a lot of integrated digital circuits are equipped in the JTAG bus. This standard is also connected with emerging of the test bus, such as FPGA configuration, its emulation, and Flash memory programming, especially microcontroller program memory programming and debugging. Thus, the JTAG bus is pervasive and versatile, but it is a strictly digital tool.
Hence, in this paper we propose to extend an existing JTAG infrastructure to enable measurements of parameters of mixed-signal or analog circuits. To this aim, we elaborated a new solution of a BIST (Built-In Self Tester) called the JTAG BIST. It is used to stimulate the analog part of an electronic embedded system included the JTAG bus, and to measure its time response parameters. Thanks to this, we can obtain fault detection and also single soft fault localization in this analog part.
In the common BIST technique, the BISTs are implemented in the form of additional structures to facilitate testing. In this technique, there are no standards, thus a variety of testers dedicated to a specific class of systems are developed. From the literature there are known numerous specialized BISTs, *inter alia*: oscillation-based BISTs (OBIST) [1,2], histogram-based BISTs (HBIST) for diagnosis of ADCs [3,4], BISTs for fully differential circuits [5,6], Transient Analysis Method BISTs - TRAM BISTs (TBIST) [7-9], ΣΔ-type BISTs [10,11].
In contrast to our proposition, these solutions of the BISTs need aditional digital interfaces, not included in their structures, to communicate with the system controller, that is expandable systems about aditional circuits used only for communication. While we use to configure the BIST, what should be pointed out, only components already equiped with the interface – the JTAG bus.

II. The JTAG BIST architecture

The JTAG BIST consists of the BCT8244A and the SCANSTA476 integrated circuits of Texas Instruments controlled via the IEEE 1149.1 bus (Fig. 1).
The BCT8244A is a scan test device with octal buffers [13]. It supports the boundary scan to facilitate testing of complex circuit-board assemblies. The SCANSTA476 is a low power, 12-bit ADC (Analog Voltage Monitor) used for sampling or monitoring up to 8 analog input channels [14]. The vendor proposes to use it during product development, environmental tests, production and field service for verifying and monitoring power supply and reference voltages, and also for card or system-level health monitoring and prognostic applications.

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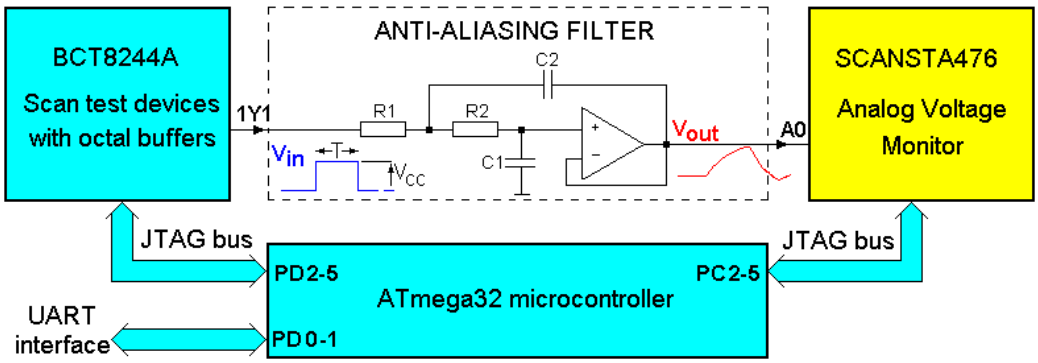

Figure 1. Block scheme of a JTAG BIST for self-testing of analog parts of mixed-signal electronic systems

For testing our solution of the JTAG BIST we built the electronic embedded system (Fig. 1) controlled by the ATmega32 microcontroller [15]. The microcontroller communicates with the BCT8244A and the SCANSTA476 via the JTAG buses emulated on its GPIOs. It selects the analog input of the SCANSTA476, initiates a measurement, and accesses the results. We control the microcontroller, which is based on the UART interface connected via the FT232 chip to the USB port of the PC. As the tested analog part we chose a second-order anti-aliasing filter in the Sallen-Key topology.
The microcontroller controls the JTAG BIST according to the modified measurement procedure proposed in [16].

III. The measurement procedure

A self-testing approach of analog parts of electronic embedded systems is based on the fault diagnosis method which belongs to SBT (Simulation Before Test) and dictionary methods [16]. Thus, this approach consists of

- a pre-testing stage, when the fault dictionary dedicated for the given analog part is created,
- a testing stage in which we use the JTAG BIST, that is the measurement procedure,
- a classification stage of fault detection and single soft fault localization.

Hence, the JTAG BIST works according to the measurement procedure. The single square pulse stimulating the analog part is generated at the 1Y1 output of the BCT8244A (Fig. 1). Its amplitude is set *a priori* to the value of the high level of a digital signal, and its duration time is established by the timer of the microcontroller. The time response of the analog part is sampled twice by the SCANSTA476. The sample moments t_1 and t_2 are determined also by the timer of the microcontroller. The values of measured voltages v_1 and v_2 are read via the JTAG bus from the SCANSTA476 by the microcontroller.
An algorithm (shown in Fig. 2) presenting details of the measurement procedure, whose timing is shown in Fig. 3, was implemented in the measurement function. The code of the function is divided into two parts. The first part is realized in the main program, the second one in the interrupt service of the Timer 1 Compare Match Interrupt.
At the beginning, in the first step of the main function, we initialize two JTAG buses, and next via these buses the BCT8244A and SCANSTA476 circuits. During the initialization, we also set the initial values of variables: *counter* – it points to the next time value written to the OCR1A register of Timer 1, *counter_result* – the counter of voltage samples, *wait* – it is used to program the synchronization between the main function and the interrupt service.
In the next step, we start the measurements. That is, we set the high level voltage at the output 1Y1 of the BCT8244A – it is the beginning of the square stimulating pulse (we use the function which introduces the command EXTEST (data value – 00 00000000 00000001b) to the BCT8244A), we write in the OCR1A register the value $t(1)$ corresponding to the value t_1 (1.855 ms) – the first moment of sampling of the time response of the tested analog circuit, and start Timer 1 in the Clear Timer in the Compare (CTC) Mode.
Next, we test the variable *wait* waiting for finishing of the measurement procedure whose maintenance has been taken over by the interrupt service.
During the first interrupt service (*counter* = 1) of the Timer 1 Compare Match Interrupt, that is when the Timer 1 counted the t_1 time, the SCANSTA476 samples for the first time the response of the tested circuit (to this aim, we send the command MUXSEL 0 to the SCANSTA476. The measurement result is recorded in the variable $v(1)$ and the new value $t(2)$ is written to the OCR1A register.

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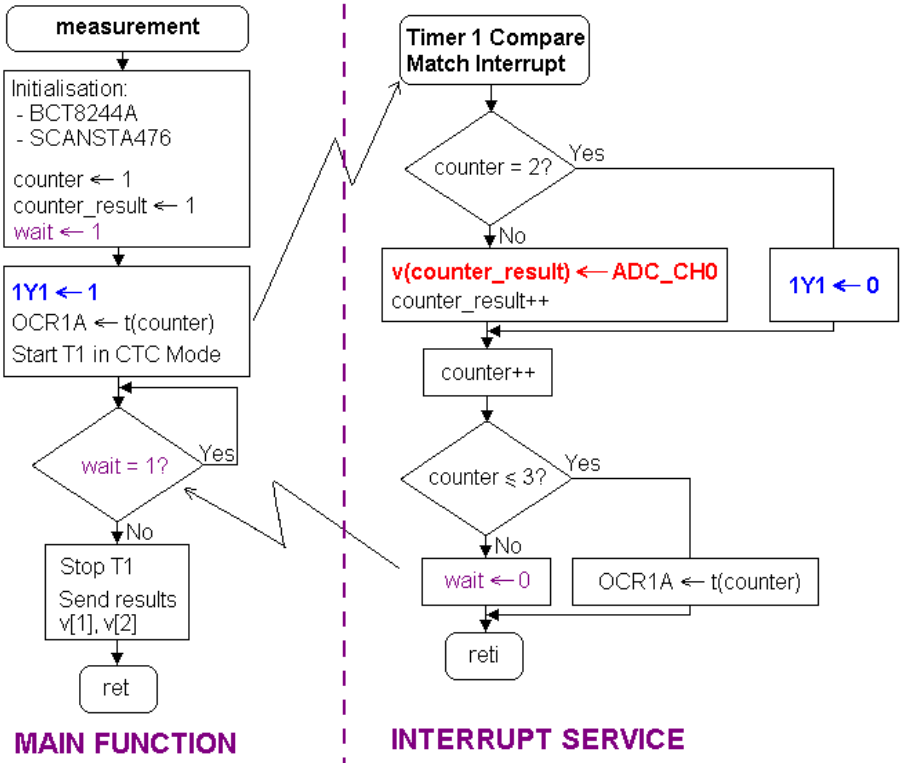

Figure 2. The flowchart of the measurement algorithm for the JTAG BIST

When the second interrupt appears, at the moment $T = t(1) + t(2) + t_d = 3.288$ ms (t_d – the software time delay), the stimulating pulse is finished – by setting the low level at the 1Y1 output (by sending the command EXTEST (data value – 00 00000000 00000000b) to the BCT8244A) and the $t(3)$ value is written to the OCR1A register. When the Timer 1 counts up to the $t_2 = t(1) + t(2) + t(3) = 4.303$ ms, the last interrupt is triggered. In its service the SCANSTA476 measures the second voltage sample, which is stored in the $v(2)$ variable, and the variable *wait* is cleared, which means that the measurement procedure is finished.
Thus, the main function again takes over the control on the measurement procedure. It stops Timer 1 and sends measurement results $v(1)$, $v(2)$ via the UART (exactly via the USB, as mentioned earlier) to the PC.

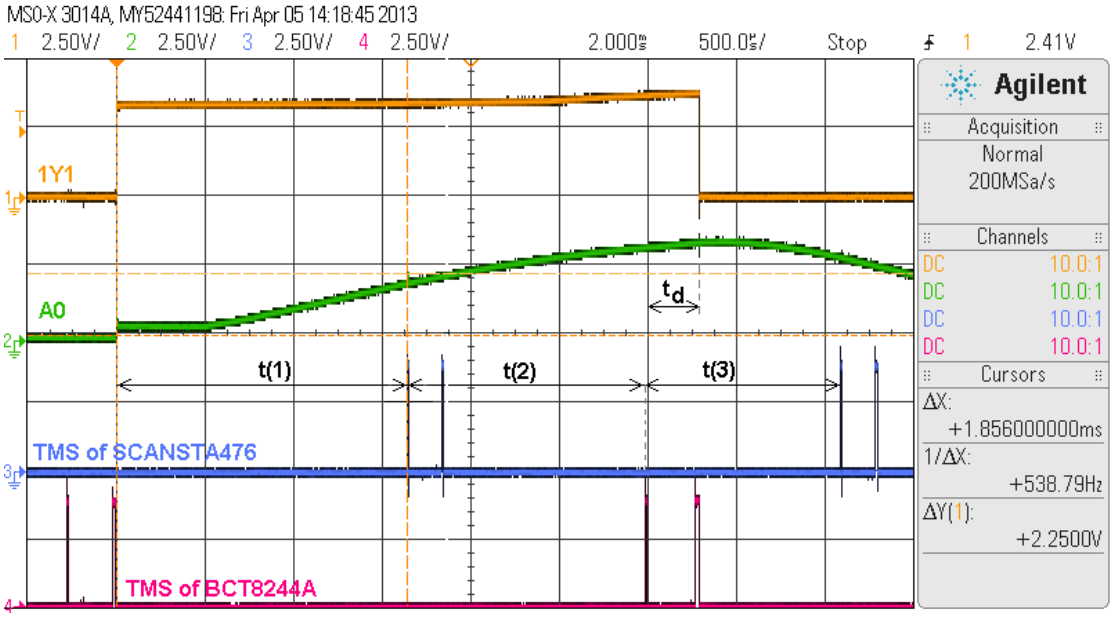

Figure 3. Timings of the measurement procedure for the JTAG BIST

Work of this algorithm is illustrated by timings measured by the Agilent MSO-X 3014A oscilloscope (Fig. 3). There are the following meanings of lines shown on the oscilloscope screen:

– The orange line (channel 1) – the test square pulse generated at the 1Y1 output of the BCT8244A.
– The green line (channel 2) – the time response of the tested analog circuit measured by the oscilloscope on the A0 line (the input Channel 0 of the SCANSTA476).
– The blue line (channel 3) – the TMS line of the JTAG bus controlling the SCANSTA476. It shows moments of sampling of the tested circuit response by the SCANSTA476.
– The red line (channel 4) – the TMS line of the JTAG bus controlling the BCT8244A. It presents moments at which the signal on the 1Y1 line of the BCT8244A is toggled.

Additionally, we marked on Fig. 3 times $t(1)$, $t(2)$, $t(3)$ counted up by Timer 1.

As mentioned, after completion of the measurement procedure, the measurement results can be sent to the PC (which is shown in Fig. 2), and next they can be used by the classification procedure to detect and to localize the faults. For example, we can use two classification methods. In the first method [16], it is checked on which identification curve or in the nearness of which curve the measurement point is placed. Hence, if the measurement point is situated nearest the given curve, it shows that the component assigned to this curve is faulty. In the case of the second method [17], which is dedicated for circuits with tolerances of non-faulty components, we check if the measurement point is placed inside the given localization belt.

IV. The experimental verification

The new solution of the JTAG BIST was experimentally verified on the example of the low-pass Sallen-Key topology filter shown in Fig. 1. Its component values are: R_1 = 9844 Ω, R_2 = 9880 Ω, C_1 = 70.41 nF, C_2 = 146.55 nF. We use the LA6358 operational amplifier operating from a single power supply (5 V).
The ATmega32 microcontroller controlling via the JTAG buses the BCT8244A and the SCANSTA476 works with a 16 MHz quartz crystal oscillator. Timer 1 is clocked directly by the system clock. It is used to determine the times $t(1)$, $t(2)$, $t(3)$. From these times we obtain the sampling moments t_1 = 1.855 ms, t_2 = 4.303 ms, and the duration time T = 3.288 ms of the tested square pulse. The amplitude of the pulse at the BCT8244A 1Y1 output is within the range from 3.50 V to 3.90 V. This imperfection of the pulse, visible in Fig 3 – channel 1, results from electrical parameters (especially the output pin current efficiency [13]) of this output pin. The reference voltage of the 12-bit ADC SCANSTA476 is set to 4.97 V.

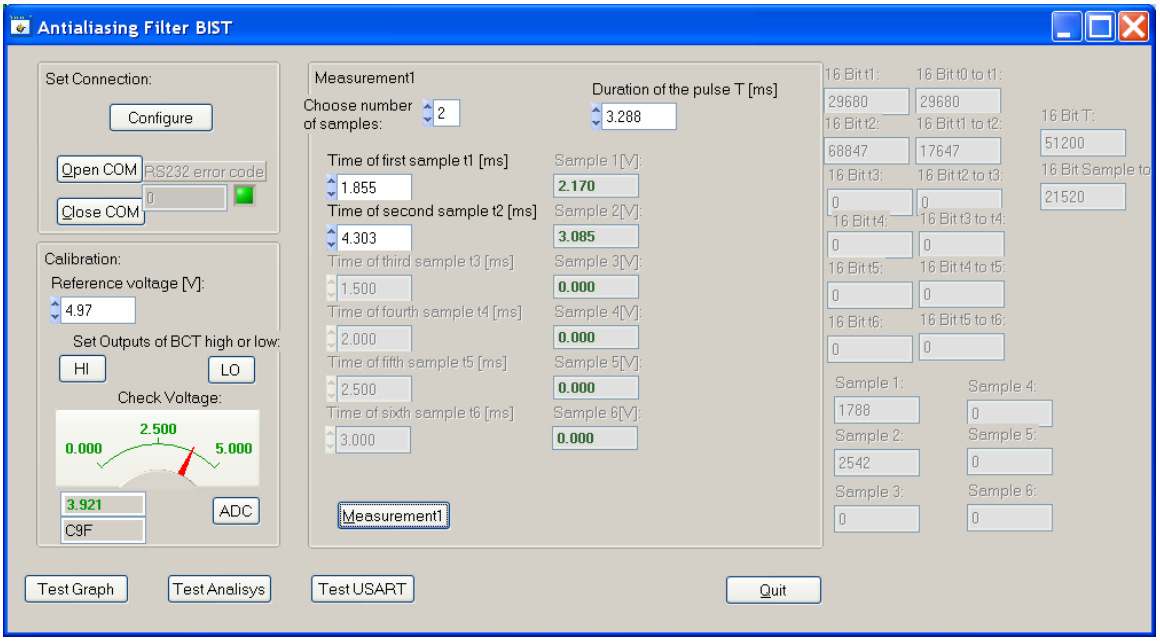

Figure 4. The main panel of the application used to control the development system of the JTAG BIST

To perform measurements, we use an application created in the LabWindows/CVI development environment. Its main virtual panel is shown in Fig. 4. The application controls the development system of the JTAG BIST, that is, it allows us to fully control the BCT8244A and the SCANSTA476 circuits, to set values of all times, to

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measure voltage samples and to analyze the measurement results.
Measurements were carried out for chosen 12 values of each component, as presented in Table 1 containing the experimental results. Different soft faults of each component were physically entered to the tested circuit and each time the measurement procedure was run. For resistors, a decade resistor was used and for the capacitors a decade capacitor whose values were controlled by the 4263B LRC METER of Agilent (Func. Cp-D, Freq. 1 kHz, Level 1 V, Bias 0 V).

Table 1. Measurements results for chosen sets of values of particular tested circuit components made by the JTAG BIST

R_1 [kΩ]	0.984	1.968	4.922	6.891	8.860	9.844	10.829	14.766	19.689	49.223	68.912	98.446
v_1 [V]	3.771	3.77	3.151	2.827	2.583	2.456	2.344	1.984	1.675	0.891	0.711	0.562
v_2 [V]	1.151	1.369	2.101	2.397	2.577	2.622	2.665	2.742	2.698	1.924	1.578	1.248
R_2 [kΩ]	0.988	1.976	4.94	6.916	8.892	9.88	10.868	14.821	19.761	49.404	69.165	98.808
v_1 [V]	3.376	3.383	3.117	2.83	2.574	2.455	2.352	1.98	1.664	0.905	0.727	0.544
v_2 [V]	0.925	1.081	1.859	2.271	2.532	2.62	2.606	2.784	2.715	1.898	1.561	1.222
C_1 [nF]	14.65	29.31	73.27	102.58	131.89	146.55	161.2	219.82	293.1	732.75	1025.85	1465.5
v_1 [V]	2.698	2.715	2.704	2.619	2.527	2.446	2.399	2.152	1.914	1.214	1.051	0.899
v_2 [V]	1.602	1.674	1.966	2.23	2.5	2.618	2.736	3.067	3.277	3.023	2.653	2.225
C_2 [nF]	7.04	14.08	35.21	49.29	63.37	70.41	77.46	105.62	140.83	352.08	492.92	704.17
v_1 [V]	3.788	3.781	3.772	3.1	2.643	2.458	2.297	1.827	1.461	0.737	0.584	0.468
v_2 [V]	0.075	0.341	2.044	2.45	2.611	2.629	2.626	2.534	2.314	1.373	1.086	0.841

The measurement results included in Table 1 treated as the measurement points were plotted in the form of triangles for R_1, squares for R_2, diamonds for C_1 and circles for C_2 in the measurement space with the simulation curves (solid lines), as shown in Fig. 5.
Each curve represents changes of properties of the tested circuit following from changes of the values of the given component for which it was drawn [16].

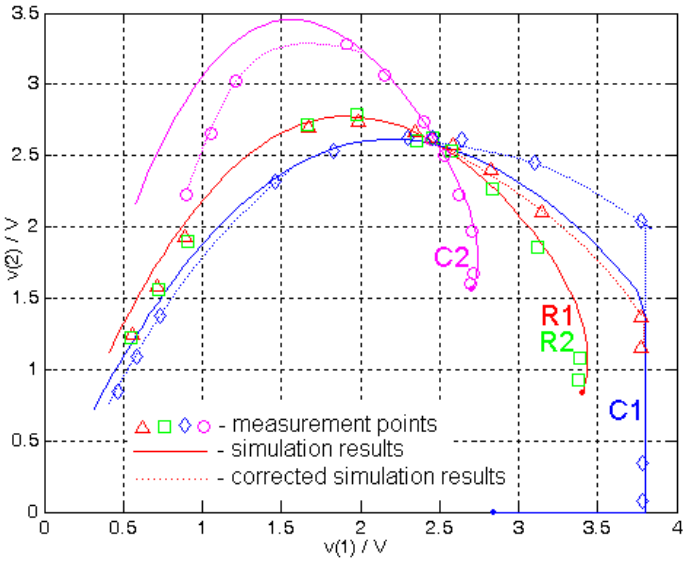

Figure 5. Family of localization curves of the tested analog circuit (Fig. 1) with measurement points

Comparing the placement of the measurement points with theoretical curves in Fig. 5 it is seen that the majority of points are situated on their curves, what experimental confirms that the method works correctly. Only for small values of R_1, R_2 and C_1 and big values of C_2 there are divergences. These differences follow from the electrical parameters of the output pin of the BCT8244A (what we can observe in Fig. 3 – the shape of the 1Y1 signal) especially, as mentioned earlier, from the output pin current efficiency [13], that is, from our point of view, following from the relatively high output impedance. Thus, taking into account this fact, we supplemented the model of the tested circuit used in the MATLAB simulation. The modified parts of curves are presented as dotted lines in Fig. 5.

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However, we ultimately plan to add the inverter built from an IRF7105PBF [18] at the 1Y1 output. In this way we will eliminate the output pin variable impedance of the 1Y1 output pin and in this way we will correct the shape of the stimulating square pulse.

V. Conclusions

Thanks to our proposition of extending an existing JTAG infrastructure with the JTAG BIST, system designers who utilize JTAG techniques to debug prototype boards will now benefit from having access to analog nodes, that is they have the possibility to test not only digital circuits but also analog circuits. This benefit also extends to those performing production tests in the factory and to hardware in the field. For high-availability systems that require continuous monitoring, designers can now use the existing JTAG bus for embedded analog measurement.
Use of the JTAG BIST consisting of the BCT8244A and the SCANSTA476 integrated circuits can also extend the lifecycle of the electronic system by reducing field service and maintenance costs, while improving system availability with innovative health monitoring features.

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