DESIGN OF A DIFFERENTIAL OPERATIONAL AMPLIFIER IN A CLOCK-LESS A/D CONVERTER

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Abstract: This paper presents a differential operational amplifier used in a continuous-time 8-bit folding analog-to-digital converter. The clock-less architecture is composed of 8 identical stages with 1 bit/stage. The circuit is designed in a 350nm CMOS process with a supply voltage of 3.3V. Simulation results show that, with this operational amplifier, the 8-bit clock-less ADC can achieve a Signal-to-Noise and Distortion Ratio of 53dB. The ADC has a power consumption of 5.51mW.

Key words: differential, operational, amplifier, clock-less, analog-to-digital converter.

1. INTRODUCTION

The low-voltage, high-performance IC's employed in modern communication products frequently must employ fully differential signal paths in order to achieve sufficient signal amplitude with a minimum of power.

Many electronic devices use differential amplifiers internally. The output of an ideal differential amplifier is given by:

$$V_{out} = A_d(V_{in}^+ - V_{in}^-) \qquad (1)$$

where Vin+ and Vin- are the input voltages and Ad is the differential gain.

In practice, however, the gain is not quite equal for the two inputs. This means, for instance, that if Vin+ and Vin- are equal, the output will not be zero, as it would be in the ideal case. A more realistic expression for the output of a differential amplifier thus includes a second term.

$$V_{out} = A_d(V_{in}^+ - V_{in}^-) + A_c\left(\frac{V_{in}^+ + V_{in}^-}{2}\right) \qquad (2)$$

Ac is called the common-mode gain of the amplifier.

As differential amplifiers are often used when it is desired to null out noise or bias-voltages that appear at both inputs, a low common-mode gain is usually considered good.

The common-mode rejection ratio, usually defined as the ratio between differential-mode gain and common-mode gain, indicates the ability of the amplifier to accurately cancel voltages that are common to both inputs.

Common-mode rejection ratio (CMRR):

$$CMRR = \frac{A_d}{A_c} \qquad (3)$$

Clocked processors have dominated the computer industry since the 1960s because chip designers saw them as more reliable, capable of higher performance, and easier to design and test than their clock-less counterparts. The clock establishes a rhythm that drives all chip, and this time constraints make design easier by reducing the number of control decisions [1].

In synchronous designs, the data moves on every clock edge, causing voltage spikes. In clock-less chips, data are not all produced at the same time, which spreads out current flow, thereby minimizing the strength and frequency of spikes and emitting less electromagnetic interference (EMI). Less EMI reduces both noise-related errors within circuits and interference with nearby devices [1].

Asynchronous chips have no clock and each circuit powers up only when used, so asynchronous processors use less energy than synchronous counterparts [1].

Moreover, regular sampling time uncertainty introduces additional errors when analog signals are sampled at equal time intervals and reconstructed at time intervals that show a timing uncertainty or vice versa. Sampling clocks show short term and long term time jitter. Especially the short term time jitter has influence on the performance of a converter [2].

In continuous-time system the amplitude can be quantized into discrete amplitude levels, resulting in an amplitude discrete signal. This operation can be performed to maintain well-defined amplitude levels when signals pass through several processing stages.

Reference [3] has confirmed that continuous-time signal processing is possible, and that it presents several advantages in comparison to the classical discrete-time case: no signal aliasing, no quantization error aliasing, this avoids sub-harmonic components, and reduces the in-band quantization error power.

Analog-to-digital converters (ADCs) are usually specified to have a fixed conversion time, but clock-less ADCs is gaining relevance in many fields, ranging from astronomy to medicine [4]. Some applications in equipments of the medical area, such as X-rays and spectrometry equipments need ADCs that are activated by the beginning

of the event and closed down in the end, to control the energy sent during the event. Thus, the conversion time has a large range of variations [5]. In this paper we propose the design of a differential operational amplifier for use in an architecture for a clock-less 8-bit 1-bit/stage folding ADC.

The use of differential operational amplifiers brings several advantages as high rejection of supply noise and higher output swings. And these features are very important in clock-less A/D converters.

2. BASIC CONCEPT OF THE CONVERSION TECHNIQUE

The general architecture of the proposed clock-less ADC is shown in Fig. 1. This structure is a folding architecture. It is one of a number of possible serial or bit-per-stage architectures. It consists of a cascade of identical stages, with one 1-bit sub-ADC and a gain stage multiplying by either 2 or -2.
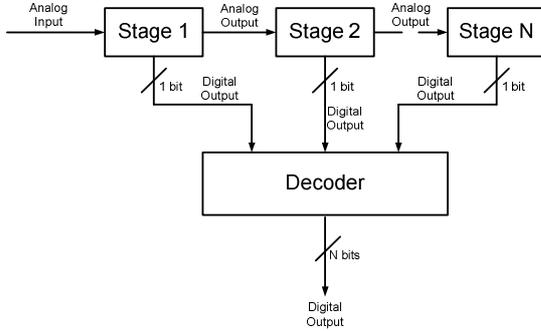

Fig. 1. Block diagram of the clock-less folding ADC with 1-bit/stage.

The idea behind this A/D converter is based on the general rectification algorithm [6]:

$$V_{out} = 2\left|V_{in}\right| - V_{Ref} \qquad (4)$$

A block diagram of one stage of this ADC along with its input and output signal waveforms are shown in Fig.2. Single-ended current-mode implementations have been proposed in [6,7,8].
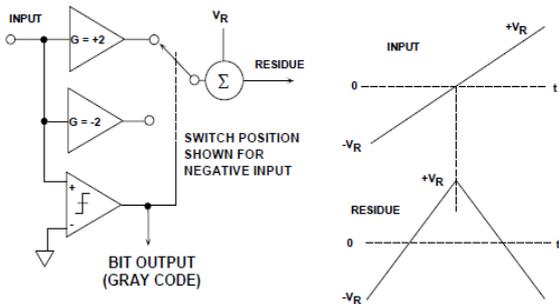

Fig. 2. Conversion algorithm of a folding ADC stage [9].

In this work, we propose to build the conversion algorithm illustrated in Fig.2, using the differential voltage-mode circuit shown in Fig.3. The output voltage of each stage of the proposed clock-less ADC is as follows:

$$V_{outp} = V_{DP}\left(2V_{inn} + V_{refp}\right) + V_{DN}\left(2V_{inp} + V_{refp}\right) \qquad (5)$$

$$V_{outn} = V_{DP}\left(2V_{inp} + V_{refn}\right) + V_{DN}\left(2V_{inn} + V_{refn}\right) \qquad (6)$$
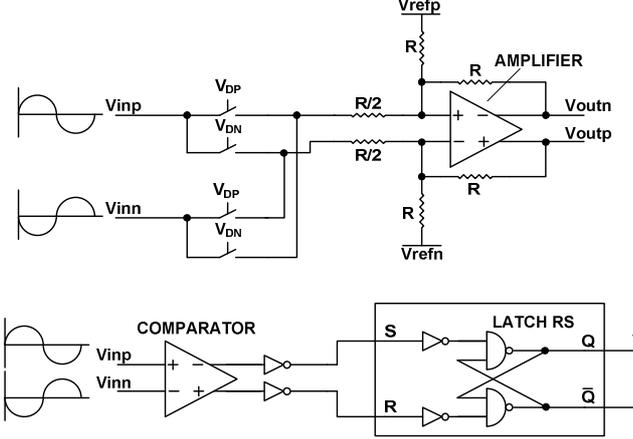

Fig. 3. Differential realization of one stage a clock-less folding ADC.

In the proposed clock-less ADC, when the analog input signal crosses the reference levels, only the sign of the signal is inverted, thus relaxing the requirements on the operational amplifier. This scheme has often been referred to as serial-Gray (since the output coding is in Gray code), or folding converter because the shape of the transfer function. Performing the conversion using a transfer function that produces an initial Gray code output has the advantage of minimizing discontinuities in the residue output waveforms and offers the potential of operating at higher speeds than the more conventional binary approach [10].

3. CIRCUIT DESIGN

The first step in designing the proposed clock-less folding ADC is to determine the operational amplifier specifications.

A complete model of an 8-bit clock-less folding ADC, using the 1-bit architecture illustrated in Fig.3, was build using macro-models for the differential operational amplifiers. This model was used to determine the minimum specifications of the operational amplifier specifications in order to achieve a Signal-to-Noise and Distortion Ratio (SNDR) higher than 50dB.

In order to calculate the SNDR, first the digital output is passed through an ideal DAC, second the continuous-time analog output is sampled using a high sampling rate compared to the input signal frequency range and finally an FFT is performed on the sampled signal. An SNDR higher than 50dB was achieved with a DC-Gain of 70dB and a Gain-Bandwidth-Product of 45MHz.

Note that a conventional 8-bit discrete-time ADC cannot theoretically achieve a SNR higher than 49.76dB (6N+1.76dB). These results support claims made in [3] that continuous-time ADCs have lower quantization noise than their discrete-time counterparts.

The operational amplifier used in the design of the 1-bit/stage ADC is show in Fig. 4, 5(CMFB circuit) and 6(Bias circuits). This is a two-stage amplifier using Miller technique for frequency compensation.

This differential amplifier was designed in 350nm CMOS technology for the specifications determined in the previous section. The transistor sizes of the operational amplifier are shown in table I.

Table 1. Dimensions of the operational amplifier's transistors.

Transistors	W/L (µm/µm)
MNA01, MNA02	5.53/1.0
MPA03, MPA04	15.90/1.0
MNA05	11.37/1.0
MPA06, MPA08	127.73/1.0
MNA07, MNA09	49.46/1.0
MNA10	39.77/10.00
MPA11	1.51/10.00
MPA12, MPA13	12.58/10.00
MNA14	4.46/10.00
MNA15, MNA16	2.23/10.00
MNA17	8.81/10.00
MPA18	99.57/10.00
MNA19	0.61/10.00
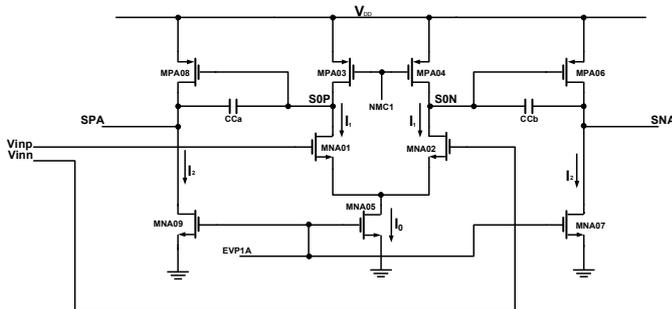
Fig. 4. Two-stage differential amplifier.(I0 = 20 µA; I1 = 10 µA; I2 = 100 µA)(Vinp, Vinn, NMC1 and EVP1A (in); SPA and SNA (out))

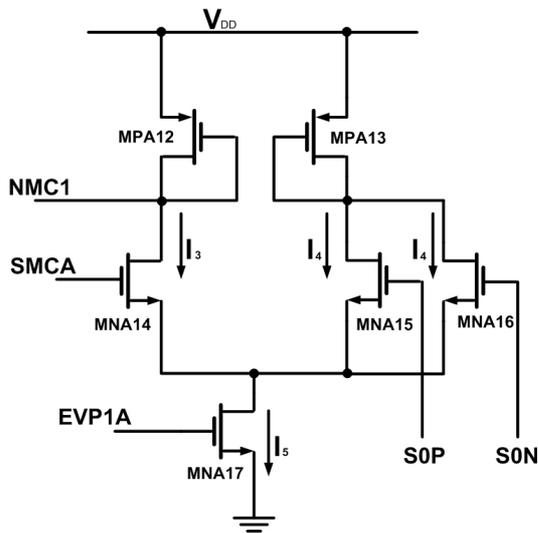**Fig. 5. Common-Mode Feedback Circuit (CMFB).(EVP1A = 0.736 V (in); NMC1 = 2.44 V(out); SMCA = 2.44 V (in); I3 = 1 µA; I4 = 0.5 µA; I5 = 2 µA; S0P and S0N (in))**
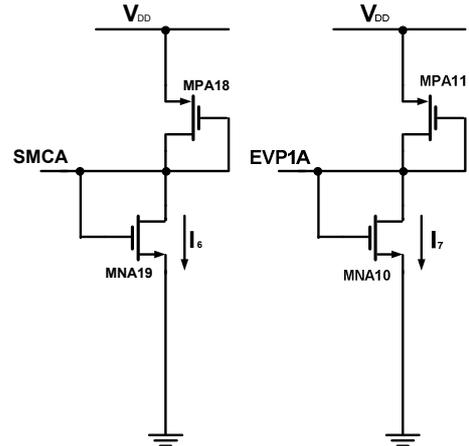

Fig. 6. Bias circuits. CMFB – left (SMCA out) and First stage – right (EVP1A out).

4. SIMULATION RESULTS

The amplifiers specifications are show in table II. This amplifier is used to design an 8-bit clock-less folding ADC based on the architecture illustrated in Fig.3.

Table 2. Specifications of the operational amplifier.

A_o	71.65 dB
F_T	45.4 MHz
SR	23.5 V/µs
Consumption	140 µW

The ADC is simulated by applying a sinusoidal signal with maximum signal amplitude and a frequency of 8 kHz. Fig.7 shows the FFT of the output of the clock-less folding ADC. It can be seen that the 3rd harmonic is around -60dB and that the folding ADC achieves a maximum SNDR of 53 dB in a 50 kHz bandwidth.

The performance and the circuit characteristics of the ADC are listed in table III. From this table, we can see that a clock-less folding ADC achieves high performance.
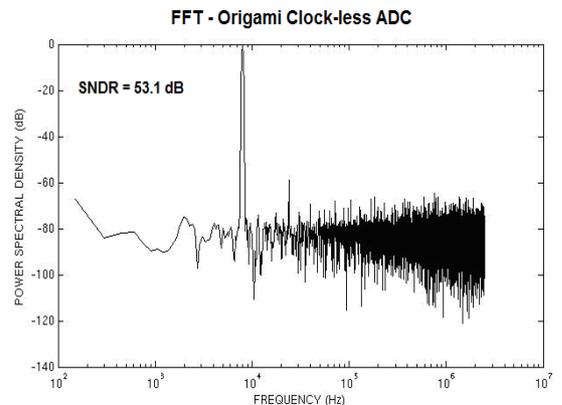

Fig. 7. The Power Spectral Density of the output of a clockless Folding ADC using the two-stage differential amplifier of Fig.4 and the dimensions of Table 1.

Table 3. Specifications ADC Folding.

	Folding
Input Frequency (fin)	8 KHz
DC Gain (amp.)	71.65 dB
GBW (amp.)	45.4 MHz
Resolution	8 bits
Power consumption (Analog Parts)	5.51 mW
ENOB	8.53 bits
SNDR	53.1 dB

5. CONCLUSIONS

In this paper, we propose the design of a differential operational amplifier to use in an architecture for a clock-less folding ADC. The proposed 1-bit stage is based on a differential voltage-mode circuit.

The required operational amplifier specifications were determined by simulation in order to obtain the desired clock-less Folding ADC performance. The op-amp was designed and integrated in the complete model of a clock-less 8-bit Folding ADC.

AKNOWLEDMENTS

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