

Fault tolerant techniques to diagnose and mitigate Single Event Upset (SEU) effects on electronic programmable devices

Lorenzo Ciani¹, Marcantonio Catelani¹, Lorenzo Veltroni²

¹ University of Florence, Department of Electronics and Telecommunications,
via S. Marta 3, 50139, Florence (Italy)

marcantonio.catelani@unifi.it, lorenzo.ciani@unifi.it

² Sirio Panel S.p.A. – Loc. Levarella Becorpi – 52025 Montevarchi (AR)

Abstract - This research faces the problem of disturbance induced by high energy particles on electronic devices. Based on detailed analysis of this phenomenon, the work is divided into two parts: in the first part testing of the Single Event Upset (SEU) has been carried out with the aim of determining diagnostic techniques and the mitigation of this disturbance, taking into account the fact that testing is one of the fundamental points in electronic programmable devices; in the second part a fault tolerant technique has been devised so as to achieve the requirements demanded on a real avionic system.

I. Effects of high energy particles

The environment where a system is due to work can influence the behaviour of electronic components contained inside it, due to high energy ionizing and non-ionizing incident particles (electrons, ions, protons, neutrons etc).

Single Event Effects (SEE) are due to the action of a single particle which crosses the substrate of integrated circuit while the others are due to the total action of the flow of particles to which the integrated circuit is subject during its entire operative life [1].

Main interest is directed to the SEE as the increase in the microelectronics integration scale has led to an increase in this kind of disturbance.

SEE are of a different type and differentiate in both transient and permanent effects. In some cases, permanent effects can be so catastrophic that they cause the complete device breakdown.

SEE are classified in:

- Transient Effect: Single Event Upset (SEU) and Single Event Transient (SET);
- Permanent Effect: Single Event Latch up (SEL), Single Event Burnout (SEB) and Single Event Gate Rupture (SEGR).

When a SEU occurs, radiation deposits a quantity of energy on a bistable element so as to cause the logic state commutation (upset). This effect predominates among those produced from the radiation of high energy particles. Upsets are easily seen in unprotected memory cells, particularly in the SRAM (Static Random Access Memory), see Figure 1 for an example.

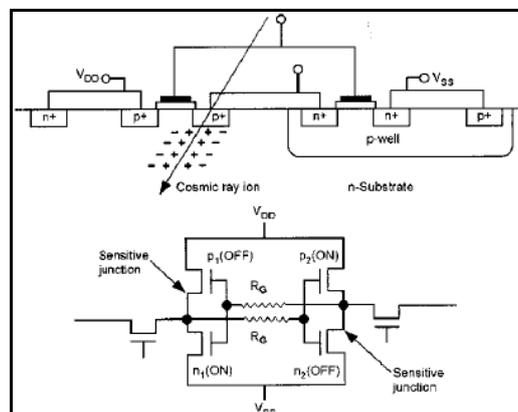


Figure 1. SRAM cell upset example.

When a charge particle, with a mechanism similar to SEU, it induces a transient on a logic port and we talk about SET. This effect is hard both to characterize and to foresee, because an effect of memorization does not take place as in the case of SEU. It can therefore generally be verified when the component is coupled with a memory device such as a latch or flip-flop which can memorize the transient as wrong information: in this case it is said that a SET has originated a SEU. Depending on the instant of the reproduction of the logic transient compared to the clock, one can or cannot have a SEU. If the transient occurs during the period of set-up or hold time of a register, the SET will lead to the reproduction of a SEU.

Multiple Bit Upset (MBU) consists of a number of cells higher than or equal to two commutation. Study of MBU is very similar to that of SEU. The cause of MBU is also to be identified in the flow of high energy particles to which the electronic devices are submitted.

II. Causes of Single Event Upset

SEUs are caused by the presence of high energy particles in cosmic radiation and, only in the smallest part, in the radioactive discharge of the component package. Cosmic radiation is formed from subatomic particles and high energy photons with the prevalence of protons produced by thermonuclear reaction which occurs in the stars.

From this radiation known as "primary", it is possible to distinguish a secondary radiation which originated as the result of a collision between primary rays and atoms from the atmosphere, composed of neutrons, protons and muons. Neutrons do not have charging capacity therefore are less likely to be adsorbed and also have a high capacity of penetration. This is why at the flight altitude (30000-50000 ft), the particles which are prevalent and responsible for the upset are neutrons [2], see Figure 2.

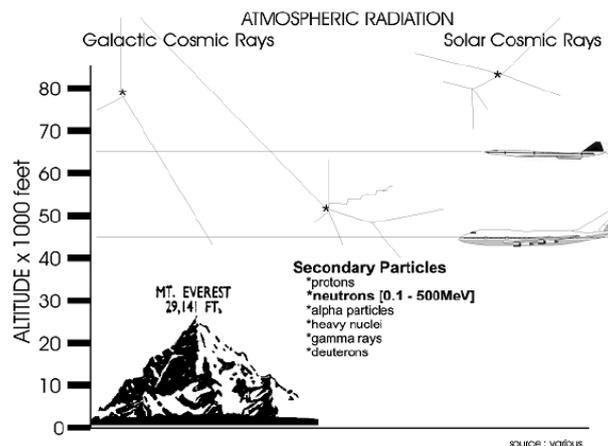


Figure 2. Atmospheric Radiation Environment.

To estimate the extent of the disturbance a statistical approach is adopted through which, initially, the upset rate named Single Event Rate (SER) is calculated by means of several statistical models. They describe the flow of radiation and calculate the upset rate, have been realized by IBM [3], NASA [4], NRL (Naval Research Laboratory) [5], USNA (United States Naval Academy) [2] e Boeing [1]. The last one is the one usually used in aeronautics.

III. Diagnostic techniques and disturbance mitigation

Diagnostic and mitigation techniques separate into fault avoidance and fault tolerant techniques. The first one consist in hardware techniques trough which it is possible to reduce the sensitivity of the device to radiation, that is, reduce the probability that upset will occur.

Fault tolerant techniques allows the system to function even in the case of fault. These techniques use redundancy to disguise, correct or reveal eventual upset and are the same ones used to protect digital system from any other type of error.

Redundancy consists of the addition of k bit of control to the m bit of information, so obtaining coding

from $m+k$ bit. This coding lets us have 2^{m+k} combinations, 2^m will single out valid words, the others will make up words which are not valid so that the Hamming distance of the coding is greater than zero. We refer to the fact that the distance of Hamming is defined as the number of bit for which two valid words differ [6]. It is also known that if the minimum Hamming distance of the coding is equal to $t+1$, t errors can be revealed, whereas it must be at least equal to $2t+1$ to correct t errors.

Fault tolerant techniques which are more suitable for this kind of disturbance, have been studied:

- Parity bit technique needs the addition of only one control bit to make the number of “1” of the word equal. This technique allows an odd number of errors to be revealed but doesn’t allow them to be corrected.
- Single Error Correction – Double Error Detection (SEC-DED) allows the correction of single errors and reveal multiple upset on two bit. As the SEU is an effect which interests the upset of a bit and MBU strikes mainly two bit, the SEC-DED technique is particularly adapt for this type of disturbance.
- Cyclic Redundancy Check (CRC) only lets errors be revealed. Its performances depend on the algorithm which determines number and form of the control bit.
- Triple Modular Redundancy (TMR) consist of the triplication of each single module of the system and allows the whole disfunctioning of one of the three modules to be disguised.

Disturbance produced by high energy particles on an electronic device can, in some applications, result unacceptable. This is the case for avionics and space applications where project requirements demand high reliability levels and what’s more, the extent of the disturbance is such that it can not be ignored.

IV. Solution developed for an avionic system

The aeronautics operating system under examination is a surveillance display present in a military aircraft cockpit. The task of system is to define the altitude of the airport for landing by means of an encoder, to visualize the selected value in meters, on a display and to transmit the information to the other system present in the aircraft cockpit.

The functions of the system are carried out through a logic device realized on a FPGA (Field Programmable Gate Array) which receives signals from the encoder and translates them into information to send to the display by means of I2C bus (Inter-Integrated Circuit) and to the other systems of the cockpit by CAN bus (Controller Area Network bus). The component of the system which is subject to upset is FPGA.

Once the critical component of the surveillance display is located in the FPGA, it is necessary to do a detailed examination of the disturbances brought on by the high energy particles on this particular component. In literature [7] errors in FPGA are separate into:

- Permanent Errors – if the configuration memory is involved and in this case the errors are removed only with a new configuration. Generally these are the worst type of errors.
- Transient Errors – which are the errors in the logic, in the registers and in the user memory that can be removed by means of correction technique.

In Figure 3 the upset rate value for the configuration memory, user memory and the registers used in this project are quoted. The values derive from tests carried out at the Los Alamos Laboratory (New Mexico, USA) [8], and relate to airborne environment by means of the Boeing model [1].

EP2C5T: Altera CyclonII (SRAM 90 nm)		
Configuration Memory upset rate	Registers upset rate	User Memory upset rate
$\lambda_{C-RAM} = 1.08 \times 10^{-4}$ $n^{\circ}upset/(chip \cdot h)$	$\lambda_{reg} = 1.6 \times 10^{-6}$ $n^{\circ}upset/(chip \cdot h)$	$\lambda_{mem} = 2.39 \times 10^{-5}$ $n^{\circ}upset/(chip \cdot h)$

Figure 3. FPGA upset rates.

In this figure, one can observe how the configuration memory presents the biggest rate, because the cells are realized in SRAM technology which offers a high level of sensitivity towards this disturbance. Protection of the configuration memory is obtained by means of the CRC technique. The FPGA used in the project permits the CRC techniques to fill automatically up to 32 bit, activating this function in the programming of the chip [9].

Alternatively, it is however to use FPGA with Flash or Antifused configuration memory which is immune to these disturbances. These FPGA have been developed with the clear intention of getting rid

of the more common SRAM based FPGA from the problem and of introducing a higher sensitivity level to the upset. Whenever possible however, use of SRAM based FPGA which normally offer better performance and which can be protected with fault tolerant techniques, is preferred.

Therefore, SEC-DED fault tolerant technique is introduced differentiating between harmful and unarmful errors and that is only data which lead to a variation of the permanent function have been protected, so reducing the complexity of the additional code: sign of the condition of state machine and data contained in the ROM (Read-only memory) implemented in the system.

A development of the SEC-DED has been realized for the state machine, the SEC-DED system together with the parity bit method has been used so allowing protection of the registers with SEC-DED code from eventual upset and the signal inside the logic, from eventual transition by means of parity bit. That is obtained by adding parity bit to the coding and by inserting the SEC-DED code onto that word. It is naturally necessary to implement a SEC-DED decoder inside the FPGA (see Figure 4).

The user memory is protected by directly storing data with the SEC-DED code and by checking the correctness which comes out with a SEC-DED decoder (see Figure 5).

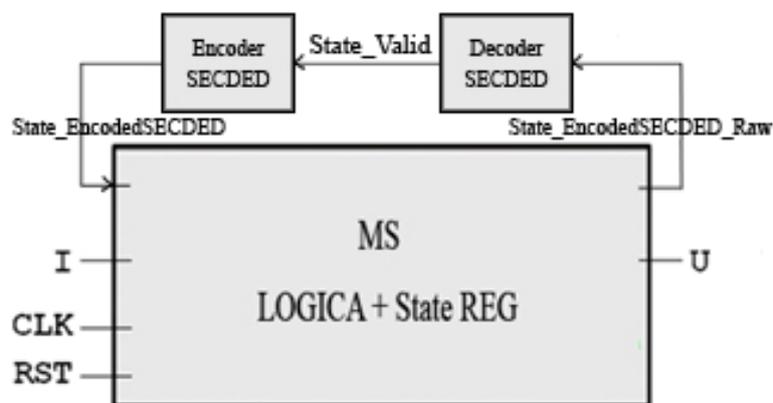


Figure 4. Registers fault tolerant technique block diagram.

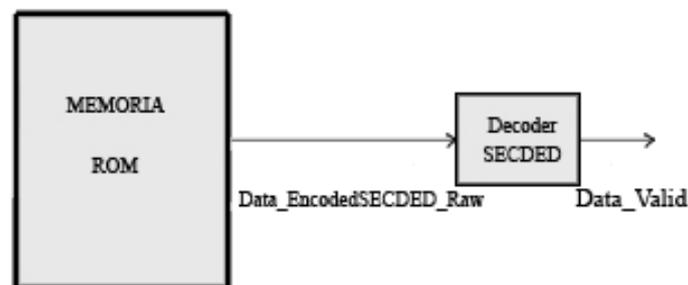


Figure 5. User memory fault tolerant technique block diagram.

V. Conclusions

This research work has allowed us to understand breakdown mechanism brought about by high energy particles and to individuate in the neutrons, the predominant component of radiation in avionics. Models to estimate the entity of the disturbance have been locked for and an increase in multiple upset due to increase in the integration scale of device has been found.

Acquired knowledge has allowed us to individuate diagnostic techniques and the mitigation of this disturbance has been developed to estimate both the need to introduce fault tolerant techniques and which of these allow us to comply with the project requirements.

Therefore a fault tolerant technique for a system present on a military aircraft has been analyzed and

devised. The technique which has been developed is general purpose and can be introduced into any generic electronic device on an aircraft.

References

- [1] Eugene Normand, "Single-Event Effect in Avionics", IEEE transaction on nuclear science, Vol. 43, No. 2, Aprile 1996.
- [2] Justin A. Sarlese "Development of a semi-empirical model for SEUs in modern DRAMs", U. S. Naval Academy Annapolis 2000.
- [3] J. F. Ziegler, "Terrestrial cosmic rays" IBM, 1996.
- [4] E. Normand, T. J. Baker, "Altitude and latitude variations in avionics SEU and atmospheric neutron flux", IEEE transaction on nuclear science, Vol. 40, 1993.
- [5] J. H. Adams Jr., R. Silberberg, "Cosmic ray effects on microelectronics" NRL memorandum report, 1986.
- [6] W. Hamming, "Error detecting and error correcting codes", Bell system technical journal, Aprile 1950.
- [7] G. Ladier, "Software Aspect of Certification in the Aerospace sector", Airbus, DO-178B/ED-12B, Novembre 2003.
- [8] "Overview of iROC Technologies Report: radiation results of the test of FPGA december 2005", Actel, Agosto 2006.
- [9] "Error detection and recovery using CRC in Altera FPGA devices", Altera, Application note 357, Gennaio 2007.