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# Measurement Techniques to Assess the Time Synchronization in Distributed Systems

Domenico Grimaldi, Francesco Lamonaca

*Dept. of Electronics, Computer and System Sciences, University of Calabria, 87036 Rende – CS, Italy*
*Ph.:+39 0984 494712, Fax: +39 0984 494713, {grimaldi, f.lamonaca}@deis.unical.it*
*http://www.deis.unical.it/html/leim.htm*

***Abstract*** - In the contest of the standard IEEE 1588, protocol for the synchronization of the node clock in Distributed System (DS), is of fundamental importance to assess the effectiveness of the synchronization. On the basis of this consideration, the aspect taken into account in the paper concerns the different measurement techniques pointed out in literature to evaluate the time delay occurring in (i) the DS among the synchronized node clocks, (ii) the telecommunication network respect to the reference clock, and (iii) the hardware and software path involved by the arrival of the command at the synchronized node and the execution of the relative action. The intent is to furnish a critical analysis of the measurement techniques, and to highlight the advantages and the limitation in the practical evaluation of the time delay.

## I. Introduction

In the Distributed Systems (DSs) the synchronization of the co-operating nodes is both an important service and a new challenging requirement that emerges in the contest of industrial automation application [1]-[3], monitoring system [4]-[7], inspection and management of strategic power plant [8]-[13], distributing computer network [14]-[16] and sensor network applications [17]-[20].
The practical requirements of the synchronization concern the correlation in the time domain of the operations given at each node and involve (i) the detection of the time delay among independent node operations, (ii) the compensation for the delay, and (iii) the implementation of the protocol to guarantee the accurate synchronized operations.
The synchronization procedures, available in the literature, operate on the clock of the network nodes. Among the various procedures, the Network Time Protocol, now established as the Internet standard protocol [21], is used to organize and maintain the clock synchronization of the PC to the time computer reference.
In order to address the needs of the local DS, the standard IEEE 1588 [22] proposes a protocol for the clock synchronization with sub-microsecond accuracy. In literature there are different type of implementation of the IEEE 1588. The researches try to minimize the effect of the non ideality of the particular implementation of the standard. The solution may be hardware, software or both. In this contest is of fundamental importance to assess the effectiveness of the synchronization and one actual aspect is the evaluation of the time delay occurring among the synchronized node clocks.
Another important aspect is represented by the time delay occurring between the arrival of the command at the synchronized node and the execution of the relative action. In particular, in the case the PC is connected to the node of the DS, the synchronization procedure operates on the clock, internal or external, of the PC. Therefore the PC can work on synchronized modality, and the delay time of received command can be detected. Nevertheless, the hardware and the software architecture of the path involved in the communication PC – final execution of the relative action can cause added time delay. The value of this last time delay can be comparable with the synchronization time delay of the node clocks [23]. This aspect is interesting for measurement applications, indeed the delay occurring among the start of the measurement procedures is depending not only by the delay occurring among the synchronized node clocks but also by the delay caused by the path involved by the commands from the PC up to le Measurement Instrument (MI). Therefore, in order to make exhaustive the analysis performed in the paper, the measurement technique of the time delay occurring in the path involved by the command is also taken into account.
On the basis of the previous considerations, different measurement techniques are pointed out in literature to evaluate the time delay occurring in (i) DS among the synchronized node clocks, (ii) in telecommunication network respect to the reference clock, and (iii) in the path involved in the communication PC-MI. In general, the measurement techniques are based on the evaluation in the time domain of the difference between two reference signals. This last can be realised in different manner (i) by time stamp of the clock at each of the synchronised nodes, (ii) by common sinusoidal signal sent to each input section of the synchronised nodes, (iii)

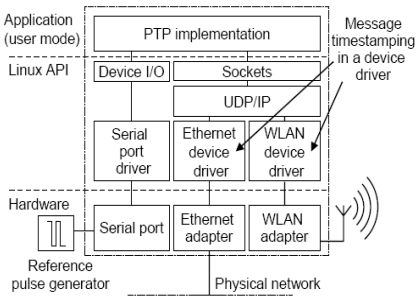


Figure 1 Architecture of Linux OS based prototype.

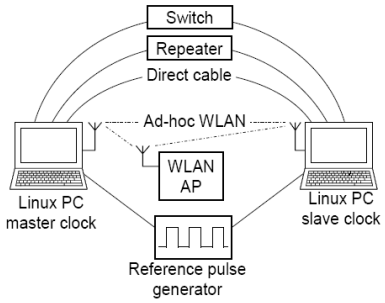


Figure 2 Measurement scheme for PC prototype.

by comparable signal generated at each output section of the synchronised nodes. The result of the measure represents the time delay of the synchronisation as much as the difference between the two reference signals is not influenced by causes not occurring in the actual establishment of the time delay under examination. Examples of influencing causes are (i) the time delay occurring to write the time stamp, and (ii) the functioning conditions in the test differently from the normal ones.

In the paper all these measurement techniques are taken into account with the intent to furnish a critical overview and to highlight the advantages and the limitation in the practical evaluation of the time delay, also.

The paper is organized as it follows. The technique to measure the synchronization time delay based on the time stamp is considered. Successively, the techniques based on common reference signal are analysed and the evaluation of specific parameters used to asses the quality in the telecommunication networks is described. Moreover the technique to measure the delay of the command into the path PC-MI is abstracted. Finally the critical analysis of these techniques is given in order to clarify their advantages and their limitations in practical applications.

## II. Synchronization time delay measurement based on time stamps

In [23] is presented the design and the implementation of two IEEE 1588 based prototypes for Wireless LAN (WLAN). The first one is implemented by using Linux PC platform and standard IEEE 802.11 WLAN with modifications to the network device driver. The architecture of the Linux PC based prototype is shown in Fig.1. The second one is implemented by an embedded WLAN development board that realizes the synchronization functionality by using an embedded processor with Programmable Logic Device circuits.

The performance of the Linux PC prototype is evaluated by external reference pulse generator. It is connected to a serial port on both master and slave nodes. When the slave nodes receives a rising edge on the serial port Clear-To-Send pin, it generates a reference timestamp. The Linux PC prototype measurement setup is shown in Fig.2. The prototype consists of a master and slave nodes, that are connected, in ad-hoc mode or with the access point, by WLAN technology. Changing the communication protocol, the performance of the LAN system obtainable by using (i) direct cable, (ii) repeater, (iii) switch can also be evaluated. Indeed, a fundamental assumption of the IEEE 1588 is that the one way delay between node master and node slave is the same of the one between node slave and master [22]. Different components adding in to the path, may not satisfy this assumption, degrading the accuracy of the synchronization of the clocks [22].

The mark operation of the timestamp just when the packet is at the output of the node, and the corrispective read operation at the input, is the second assumption of the IEEE 1588 standard [22]. In the case of node implemented with a PC, this second assumption can be not satisfy in User Space using the normal operating system [29]. The concurrent processes into the Linux OS, indeed, can interrupt the synchronization one introducing an unforeseeable latency. Therefore, the marking operation of the time stamping is moved in Kernel Space by modifying the driver of the board used to access the network.

The hardware solution better satisfy the two hypothesis of the IEEE1588. In order to evaluate the accuracy of the prototype, the PC needs. It is connected to both clocks via RS232 interface, collects the reference timestamps, and elaborates the data.

The solution based on the embedded WLAN development board permits to reach the average clock offset equal to 1.1ns. Differently, that obtained by both Linux OS and modified wireless driver permits to reach the average clock offset equal to 660ns.

In [24] the aspects concerning the effects of cross-traffic on the one-way delay of packets containing timing information, as well as the study of timestamp inaccuracies are taken into account. The investigation is performed by test bed designed to evaluate synchronization performances for a generic network environment in a variety of different conditions.

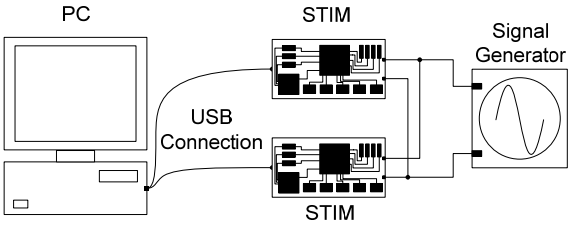


Figure 3 Experimental set up to evaluate the synchronization time delay between two Smart Transducer Independent Module.

## III. Synchronization time delay measurement based on common reference signal

In [25] is proposed the measurement technique of the time delay occurring among smart sensors, builded according to the recommendation of the standard IEEE 1451. The connection between the Smart Transducer Independent Module (STIM) and the Network Capable Application Processor (NCAP) is obtained by the Universal Serial Interface (USB). The block diagram of the configuration is depicted in Fig.3. The NCAP is implemented into the PC.

In order to evaluate the time delay of the synchronization between the two STIMs, the output voltage of the common signal generator is sent to the Analog/Digital converters equipping the input section of each STIM board. The start of the acquisition is synchronized by the preliminary exchange of messages between the NCAP and the STIMs in order to synchronize the local clocks of each STIM. After the acquisition, the samples are transferred to the PC by the USB. The data samples are processed according to the Transducer Electronic Data Sheet information of each STIM. The developed LabVIEW program performs a seven-parameter sine-fitting algorithm to estimate the acquired signal amplitudes, DC components, phase difference, and common frequency [26].

The versatility of the seven-parameter sine-fit enables the use of a different number of samples for each channel and also different sampling rates. After the estimation of the sine parameters, the phase difference is the measure of the delay between the acquisition start of both STIMs.

According to this technique, the statistical parameters characteristic of the STIM synchronization are possible to estimate thought multiple acquisitions.

## IV. Synchronization time delay measurement in telecommunication network

In order to asses the synchronization level between two clocks of the telecommunication network, two different families of tests can be executed [32].

The first is related to the frequency measurement and concerns the evaluation of the tolerance of the system to the frequency offset. The offset is introduced and the behaviour of the network components is observed.

The second is related to the phase measurement and concerns the measure of the jitter and the wander. The jitter is the periodic frequency variation above 10 Hz, the wander is the periodic frequency variation above μHz.

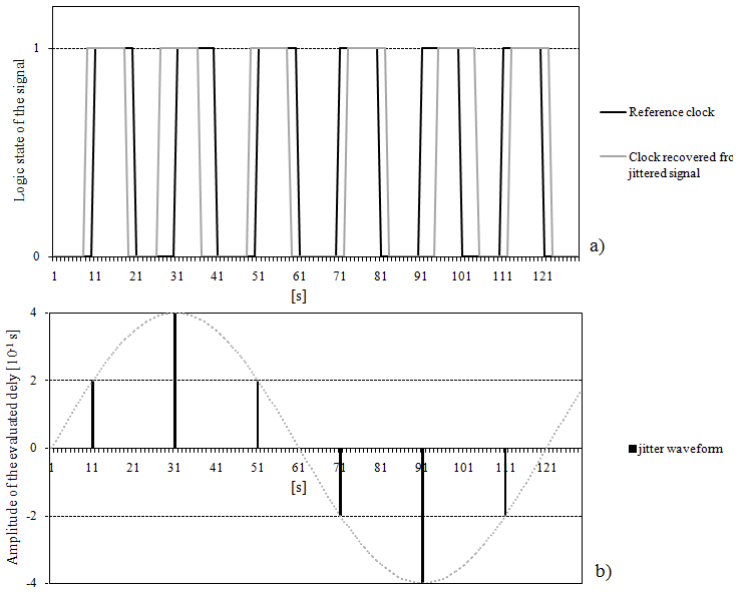


Figure 4 Phase offset measure: a) reference clock and clock recovered from jittered signal, b) waveform of the measured delay between the reference clock and clock recovered.

It is well known that the disruptive effect of the jitter depends on its frequency. Therefore, it needs to measure the magnitude of the jitter at different frequencies.

The phase measure consists in the comparison of the electrical signal of the clocks under examination with the reference one. The reference clock can be obtained from the same clock under test by filtering the frequency above the threshold of frequency equal to 10 Hz. The time delay between the rising front of the wave shape of the two clocks is taken into account, Fig.4a). The amplitude of the time delay evaluated for each rising front is depicted as time function, Fig.4b). The Discrete Fourier Transform of this function furnishes the information about the magnitude of the jitter at different

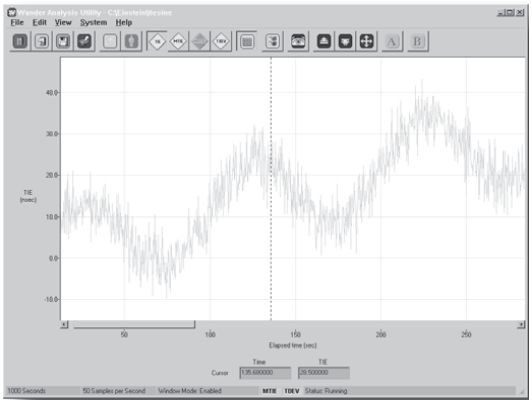


Figure 5 Time Interval Error variation versus time.

frequencies. In practical application it is useful to detect the number of times that the jitter peak exceeds the threshold value.

Moreover, three standardized jitter measures can be performed: (i) jitter tolerance, (ii) jitter transfer, and (iii) output (intrinsic) jitter.

In the first, the added jitter with established frequency and amplitude is imposed to the stand alone network element, that it is the Device-Under-Test (DUT). The output of the DUT is taken into account in order to relive the errors due to the not supported jitter. The test is performed by adding jitter at different values of frequencies and amplitudes to find the conditions at which first error occurs once the jitter tolerance is exceeding the specific masks [32].

In the second measure, the jitter transfer evaluation, the ratio between the jitter at the output and that at the input of the DUT is evaluated, for different jitter frequencies.

In the third measure, the output jitter, the amount of the jitter at the DUT output is evaluated, once no jitter to the input is fed.

In wander measurement, the comparison of the clocks under examination with the reference one is executed again. The measure is more difficult than the jitter one. Indeed, the wander frequency can be extremely low and the settling time of the internal reference is very long. Therefore wander measurement is only really meaningful where an external reference of known good quality can be used, for example the Synchronization Supply Unit or Building Integrated Timing Supply clock.

In particular, the wander measure consists in evaluating the time delay between the clock signal under test and the accurate reference one. This time delay is known as Time Interval Error (TIE) and it is usually expressed in ns. The TIE is initialized to zero at the start of the measurement interval. Fig.5 shows an example of TIE measure. If the TIE steadily increases (or decreases) with time, it means that the clock is running at different frequency from the reference clock.

Moreover, the long-term behavior and stability of the timing can be evaluated by the Maximum Time Interval Error (MTIE). The MTIE is calculated moving a variable window (observation interval) through the TIE values and latching the highest value of TIE for each observation interval. The derived plot of these latched maxima, as a function of the size of the observation interval, gives the MTIE result.

## V. Time delay measurement into the hardware and software path PC-MI

Often the MI is interfaced at the node of the DS by the PC and the synchronization procedure operates on the clock, internal or external, of this last. Therefore the PC can work on synchronized modality, but the hardware and software architecture of the path involved in the communication PC-MI can delay the commands [27-30].

In [27]-[30] different techniques to measure the delay of the commands are proposed. These techniques are performed in order to validate (i) different types of connection PC-MI, (ii) different performances of Operating Systems (OS), (iii) different setting up of Linux OS, and (iv) the performance of the Linux Real Time OS.

Each measurement technique is based on a common reference signal sent to the PCs in order to start the programmed operations in the synchronized modality. In particular, three PCs and an oscilloscope are used. One PC is configured as master that send the common reference signal to the slaves and elaborates the data acquired from the oscilloscope and transferred by GPIB interface. Other two PCs are configured as slaves. Each one represents the synchronised node of the DS. The oscilloscope measures the time delay occurring between the command that each PC sent to the MI by the ramp voltage at the pin#2 of the parallel port. The delay occurring between the commands is due to the configuration of both hardware and software of each PC.

The experimental set-up shown in Fig.6a) refers to the evaluation of the delay occurring when the common synchronization command is sent by WiFi connection. Fig.6b) refers to the evaluation of the delay occurring when the common reference signal is sent by wired connection on parallel port. Both the slave PCs are equipped by Linux OS and Linux OS RT, alternatively.

Another aspect investigated in the literature [31] is the estimation of the time delay occurring into the path involved by the command sent by a node and received by another one in the wireless connection. In particular, by starting from a detailed analysis of delay time occurring since a packet is build into the sender, and read into the receiver, the mathematical model of the delay is pointed out. Based on this model, the parameters involved

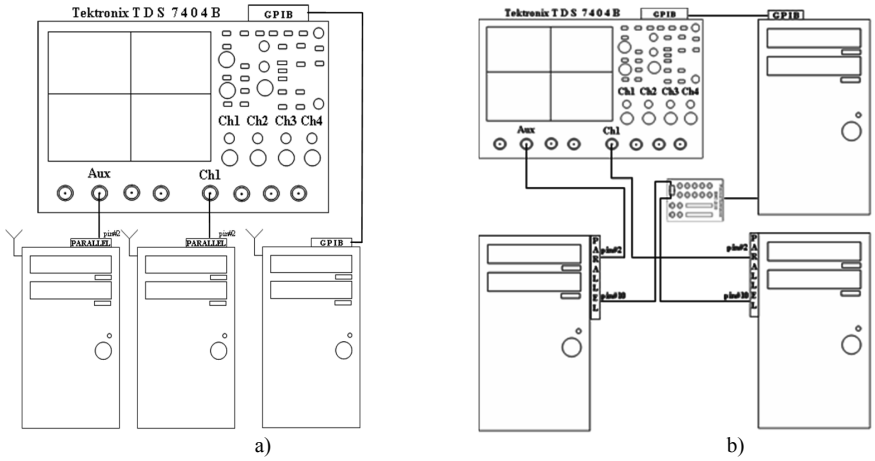


Figure 6 Experimental set up to evaluate the delay between the ramp voltage generated at the pin#2 of the parallel port of two slave PCs receiving from the master PC the synchronised start signal by a) the WiFi connection, and b) wired connection.

into the time delay are measured. The measure of these parameters is used into the mathematical model to estimate the delay between two Wireless Sensor Networks Node in function of the payload size, only.
The parameters bellowing the model represent the time intervals corresponding to the beginning and to the end of the sub-processes during a packet transmission. Therefore, the digital oscilloscope can be used to measure the time intervals of the various latency contributions. This approach leads to very accurate results, because no software-related delays affect the measurement process.

## VI. Remarks upon the measurement techniques to evaluate the synchronization time delay

In the following the remarks about the previous examined measurement techniques are given with the intent to highlight some interesting aspects that could be examined in the future researches.
The measurement technique based on the time stamp is sensitive to the modality to implement the time stamps. Indeed, the well established implementation according to the transmission protocol used in the communication network can significantly improve the measurement accuracy.
Moreover, the concurrent processes into the OS can influence the measurement accuracy, also. Indeed, the time stamp process can be interrupted by another concurrent process with higher priority. In this case the solution proposed and experimented in [24], concerning the modification of the kernel by means of proper module, can be a prospective way to be followed. The effectiveness of the solution could be improved by implementing and experimenting Real Time modules.
The measurement technique based on the common reference signal can be advantageously used in the case that the synchronization time delay ($\Delta_s$) is assessed to be lower than the period (T) of test signal. Otherwise, in the case $\Delta_s \geq T$, it occurs that the measured time delay ($\Delta$) is $\Delta = \Delta_s - kT$, where k is the integer part of the ratio $\Delta_s/T$.
The use of one shot rise time signal overcome the previous inconvenient, and if the delay is bigger than the observation window, only one rising signal can be detected.

## VII. Conclusions

The overview is given of the measurement techniques pointed out in literature to evaluate the synchronization time delay occurring in (i) the Distributed System among the node clocks, (ii) the telecommunication network respect to the reference clock, and (iii) the path involved in the communication PC-MI.
The techniques are grouped in three different categories on the basis of the modalities to evaluate the time delay: (i) by time stamp of the clock both at the sending and at the receiving of the command, (ii) by common sinusoidal signal sent to each input section of the synchronised nodes, (iii) by comparable signal generated at each output section of the synchronised nodes.
The intent of the examination of the different measurement techniques is: (i) to furnish a critical overview, and (ii) to highlight the advantages and the limitation in the practical evaluation of the synchronization time delay. This is of fundamental importance to assess the effectiveness of the node synchronization in the contest of the standard IEEE 1588.
As concluding remarks, some interesting aspects that could be examined in the future researches are shown.

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