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FPGA-based Compensation of Current Transformers

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Abstract- Voltage and current transformers are the most installed transducers in electrical power system and typically they are constructed to operate at industrial frequency, 50/60 Hz. On the other hand power quality analyses in the last years has assumed more and more heaviness in industrial environments, due to the presence of non-linear loads: they require measuring instrumentation with large bandwidth. Therefore in this paper a real-time digital technique for the compensation of current transformers, based on field programmable gate array, is presented: it implements a digital filter with a frequency response equal to the inverse one of CT. The compensated CT continues to be an analog device since the FPGA board is opportunely equipped with analog to digital and digital to analog converters. Experimental results have shown that the compensated CT improves performances of the original CT of a factor 24.

I. Introduction

The growing number of non-linear and unbalanced loads in the electrical systems makes the scientific interest in harmonic and inter-harmonic analysis increase. Nevertheless, the standards related to the type tests for accuracy of measuring instrument transformers [1], [2], which at now are the only ones to account when calibrating voltage or current transducers, establish the way to test the accuracy only at the rated frequency and amplitude, and they don't say anything about how to find the frequency response and the linearity of such instruments. This, on the other hand, is in contrast with other standards related to power quality phenomena [3], [4], in which requirements for harmonic measurement are established: a power quality instrument must have the capability to measure spectral components of the grid voltage at least up to 40th harmonic frequency. Of course, since the harmonic components have amplitude and frequency different from the fundamental one, the accuracy of power quality instruments, and thus of instrument transformers, has to be determined also in these situations.
Voltage and current transformers (VT and CT) are the most installed transducers in electrical power system and typically they are constructed to operate at industrial frequency, 50/60 Hz. It is clear that their substitution would require an unsustainable cost, even if justified by the growing cost linked to bad power quality firstly coming, in turn, from the lack of energy quality monitoring. Therefore, having the use of low cost devices, with which increasing measuring transformers accuracies, would be of great interest. In scientific literature several papers face the issue of compensating CT and VT [5]-[7]. They all present techniques for compensating measuring transformers only at industrial frequency. So, in this paper a technique for compensating current transformers in a wide frequency range, 10 Hz to 10 kHz, is presented. It is based on the identification of a digital filter implemented on an FPGA board, provided of analog to digital (ADC) and digital to analog (DAC) converters.
In section II compensation method is shown; since it utilizes data from calibration of CT, sec. III focuses on the description of an automated test system for the characterization of CT. Then, sec. IV presents experimental results related to optimization and compensation.

II. Compensation method

Far from power transformers, current transformers can be considered as linear devices basing on some considerations. In fact, non linearity is almost completely due to one phenomenon, which is the magnetic core saturation [8]: it is directly proportional to primary current r.m.s. and it is minimized by large turns ratio, small burden, small remanence flux, large core area and small secondary resistance. In general, current transformers are constructed in order to meet the last three requirements; regarding the burden, it has to be chosen according to the maximum power transferable from primary to secondary, in order to maintain accuracy class. Finally, for what concerns primary current r.m.s., according to [2] the accuracy class has to be maintained in the range of 5 to 120 % of the primary current: of course its r.m.s. depends on the amplitudes of fundamental and other frequency components. Anyway, since the contribution of a frequency component to the core magnetic flux is inversely proportional to its

frequency [8] and, in most cases, their amplitudes are much smaller than the fundamental one, they can be surely neglected. Therefore, under the assumption that primary current does not exceed 120 % of its rated value, a CT can be considered a linear device, as it is considered in most scientific papers proposing compensation techniques [5]-[7].
All the cited techniques, even if they reach considerable performances improvement factors in both ratio and phase errors, they do not consider the possibility of improving CT performances in a wider frequency range. As a matter of fact, for a linear system a frequency response can be defined and thus another linear system with a frequency response equal to its inverse can be found and it is called the inverse linear system of its. Such statement is at base of the proposed compensation technique: once the CT has been metrologically characterized and its frequency response found, cascading a device with a frequency response equal to CT's inverse one performances will be improved in a wide frequency range.

A. Identification procedure

If the CT has got a low linearity error, it can be considered as a linear system and its frequency response is given by (1):

$$Y(f) = \frac{1}{R(f)e^{-j\varphi(f)}} X(f) \tag{1}$$

where X is the input, Y the output, R and φ respectively the transduction ratio and the phase displacement defined in [9]. Therefore, in order to eliminate the frequency dependence in (1), a digital filter has to be found, which has got a frequency response given by (2):

$$H\left(e^{j2\pi f T_s}\right) = R(f)e^{-j\varphi(f)} = \frac{X(f)}{Y(f)} \tag{2}$$

where H is its frequency response and T_s is the sampling period. Such identification problem is an optimization problem and so an objective function has to be defined and minimized through an optimization algorithm.
The wider class of optimization problems existing in literature are constrained. The use of constraints is important, in fact, they allow to divide the search space into feasible and infeasible regions.
Constraints can be of two types:

1) equality and inequality constraints;
2) variable bounds.

The optimization problem here studied is nonlinear, inequality constraints and variable bounds (restricting each decision variable to take a value within a lower *(lb)* and an upper *(ub)* bound, and constituting a *decision variable space D*) are enforced. A solution that does not satisfy all the constraints and all the bounds is called infeasible solution, and it will be ignored. The problem related to the evaluation of the unknown coefficients of the digital filter can be formulated as an Inverse Problem (IP) [10]from the mathematical point of view, and solved by adopting optimization techniques [11].
The poles of the digital filter must be in the unit circle, in order to assure filter stability and this condition constitutes nonlinear inequality constraints. Lower and upper bounds, *lb* and *ub*, have been set respectively to -1 and 1, in order to restrict *D*: with this position, *D* is equal to $(-1,1)^{n+m-1}$, with *n* and *m* being respectively denominator and numerator lengths, instead of R^{n+m-1}, with *R* the set of real numbers, reducing computational burden of optimization problem without loss of generality [11].
The objective function (3) is composed by two pieces, the first piece takes into account the information about the magnitude response of the filter, while the second piece takes into account the information about the phase; the first addend is equal to the quadratic mean of the ratio, frequency by frequency, among compensated ratio error, defined in (4), and uncompensated one, defined in [9], while the second addend is equal in the structure but refers to phase displacement. Compensated phase displacement is defined in (5), uncompensated one in [9].

$$F = \frac{1}{2}\left(\sqrt{\frac{1}{N_f}\sum_{k=1}^{N_f}\left(\frac{\Delta R_C(f_k)}{\Delta R(f_k)}\right)^2} + \sqrt{\frac{1}{N_f}\sum_{k=1}^{N_f}\left(\frac{\Delta \varphi_C(f_k)}{\Delta \varphi(f_k)}\right)^2} \right) \tag{3}$$

$$\Delta R_C(f_k) = 100\left(\frac{|H(f_k)|}{R(f_k)} - 1\right) \tag{4}$$

$$\Delta \varphi_C(f_k) = \arg H(f_k) - \varphi(f_k) \tag{5}$$

Objective function depends on filter coefficients since it depends on compensated ratio error and phase displacement, which depend, in turn, on filter transfer function in (6): totally, it depends on n+m-1 variables. It is apparent that the less the objective function value the better the compensation made by the filter.

$$H\left(f_k\right) = \frac{\sum_{h=0}^{m-1} b_h e^{j2\pi h f_k T_s}}{1 + \sum_{h=1}^{n-1} a_h e^{j2\pi h f_k T_s}} \tag{6}$$

To numerically study the (3), a hybrid scheme based on the combination of a stochastic [12] and deterministic [13] approach have been adopted. In particular way, a genetic algorithm having a population size a value n greater the number of coefficients of the digital filter is chosen, and constrained by using the two different kinds of constraints, above mentioned, is initially run.
The combined use of the two approaches is related to the possibility to take advantages of both techniques. The efficiency of the deterministic algorithm depends on both the choice of the initial point, and the convergence to an optimal solution. Referring to the choice of the initial point, this difficulty can be overcome by means of the genetic algorithm; in the same way, the fact to first use a genetic approach to study the IP, and only after to use the deterministic approach, is related to the possibility to restrict the space of the possible solution.
A constrained deterministic approach based on the SQP (Sequential Quadratic Programming) algorithm is subsequently run with the aim to obtain an improvement in the search of the optimal solution. The optimal solution of the genetic algorithm has been chosen as initial point to run the deterministic algorithm. The choose of the SQP algorithm than other algorithms (such as the simplex method, that is a zero-order method) is related to the possibility to take into account the information about the derivative of the objective function, further on the fact that the problem must be constrained.
The procedure has got some parameters, which can be arbitrarily chosen: these are sampling frequency, filter numerator and denominator lengths. Regarding the first one, its value depends on the specific application and thus it must be chosen by the user: for the case at hand, as it will be seen in the next subsection, since the digital filter has to be implemented on the FPGA board with 200 kHz ADC and DAC, sampling frequency is chosen equal to 200 kHz. Regarding the others they cannot be independent variables of objective function: in fact, their sum represents the number of independent variables of the fitness function and every optimization algorithm requires that this number is fixed. In order to overcome this limit they are passed to the algorithm as parameters and the procedure is repeated a certain number of times, varying every run numerator and denominator lengths, with the aim of choosing their best values.
Identification procedure is made in this way: first of all transfer function defined in (1) is constructed in a numerical way, linearly interpolating experimental data from calibration. The optimization algorithm runs in three nested loops, varying numerator and denominator lengths; in the inner loop the procedure is repeated a certain number of times. This is required basing on the fact that the utilized hybrid optimization technique comprehends a stochastic algorithm which returns different results every run. The number of frequency points are chosen equal to four times the total number of coefficients. Among the solutions referring to the same numerator and denominator lengths, which come from the inner loop, the one which minimizes cost function is chosen.

B. Implementation on FPGA board

The identified digital filter represents the inverse linear system of the characterized CT. In order to real-time compensate the CT a digital processor, opportunely equipped with analog to digital and digital to analog converters, has to be used. For the case at hand, an FPGA board has been used. It has got an ADC and a DAC with 16 bit resolution and 200 kHz maximum sampling frequency for the first one, 1 MHz for the second. The block scheme of compensated CT is shown in Figure 1.
In Figure 4, I_1 is the primary current, I_2 the secondary current, V_2 the voltage across the shunt at the secondary winding, V_{2k} the sampled version of V_2, V_{2k}^* the filtered version of V_{2k}, V_2^* the analog version of V_{2k}^* and it is the output of the compensated CT. Such an instrument transformer continues to be an analog device, offering thus the possibility of being employed in whatever measuring system.

III. Current transformer metrological characterization

For the metrological characterization of current transformers an automated measuring station has been realized: it is based on a power source, numerically controlled, and a PXI platform. Its block scheme is

shown in Figure 2 and its features are described in [9]. The outputs of the reference shunt and of the CT are simultaneously sampled and acquired through data acquisition board and they are compared. The software for the automated measuring station has been implemented in LabWindows CVI, a C programming environment, measuring instruments oriented, distributed by National Instruments.
The measuring station is programmed in such a way that it automatically performs the desired number of tests in order to determine the mean transformation ratio, the frequency response and the linearity of the CT under test, as it is described in [9].
For the case at hand a CT with ratio 150/5 A/A, accuracy class 0.5 and rated power of 5 VA has been utilized; using three primary supplementary turns its rated ratio becomes 50/5 A/A. Preliminary test in order to determine ratio at rated frequency, 50 Hz, and rated current, 50 A, has been conducted: it is 10.01 A/A. The CT has been characterized in the frequency range of 10-10000 Hz at rated current of 50 A, using a resistive shunt of 100 mΩ at secondary winding. According to [1], [2] ratio error and phase displacement of CT are found and they are shown in Figure 3: it is evident that ratio error is equal to zero at 50 Hz.

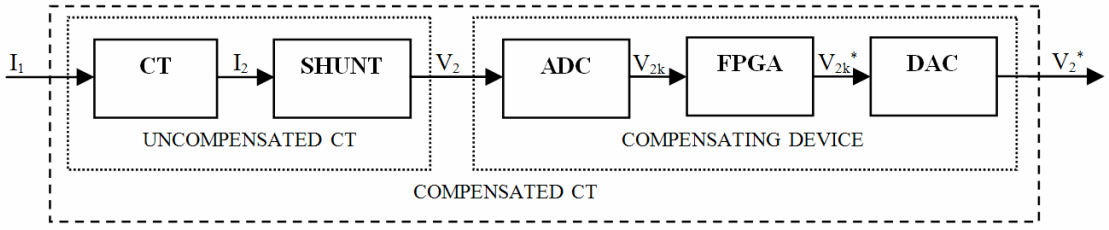

Figure 1. Block scheme of the compensated current transformer

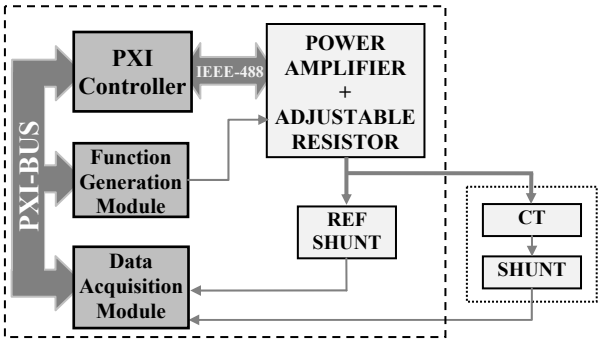

Figure 2. Block scheme of the realized calibration station.

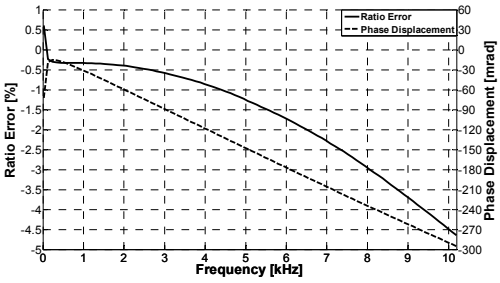

Figure 3. Ratio error and phase displacement of current transformer.

IV. Experimental results

Data available from calibration of CT are used in optimization procedure, in order to find the digital filter that minimizes ratio error and phase displacement of compensated CT. This digital filter is then implemented in the FPGA compensating device and the compensated CT is characterized with previously described automated measurement station. Optimization and compensation results are discussed in the next subsections.

A. Optimization results

Procedure described in sec. II.A has been used in order to identify a digital compensating filter for the utilized CT, whose metrological characterization is described in sec. III. As it is previously said, sampling frequency of digital filter is chosen equal to 200 kHz, since it is sampling rate of A/D and D/A converters of FPGA board. Denominator and numerator lengths, n and m, are chosen in the range of 5÷12 and population size of genetic algorithm 50 greater the $n+m$ value. The inner loop is repeated 3 times. To compare the improvements introduced by the different solutions, two indices have been used, as in formulas (7) and (8), where I_R and I_φ are, respectively, improvements in ratio error and phase displacement. In figures 4 and 5 I_R and I_φ for CT as functions of numerator and denominator lengths are shown. The best digital compensating filter, which minimizes objective function, has 11 zeros and 11 poles; numerator and denominator coefficients are shown in Table 1. Improvements in ratio error and phase displacement, coming from simulations for the adopted solution, are respectively equal to 24.4

and 22.8.

$$I_R = \frac{\overline{\Delta R^2}}{\overline{\Delta R_C^2}} = \frac{\sqrt{\frac{1}{N_f}\sum_{k=1}^{N_f}(\Delta R(f_k))^2}}{\sqrt{\frac{1}{N_f}\sum_{k=1}^{N_f}(\Delta R_C(f_k))^2}} \tag{7}$$

$$I_\varphi = \frac{\overline{\varphi^2}}{\overline{\varphi_C^2}} = \frac{\sqrt{\frac{1}{N_f}\sum_{k=1}^{N_f}(\varphi(f_k))^2}}{\sqrt{\frac{1}{N_f}\sum_{k=1}^{N_f}(\varphi_C(f_k))^2}} \tag{8}$$

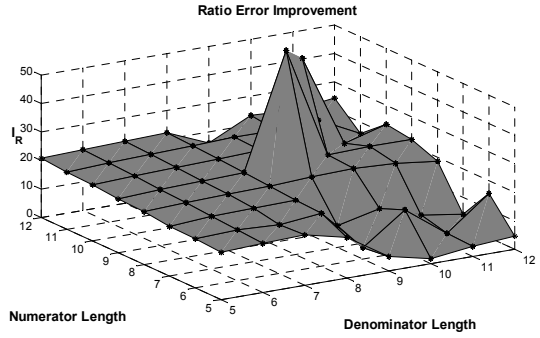

Figure 4. Improvement of ratio error as function of numerator and denominator lengths

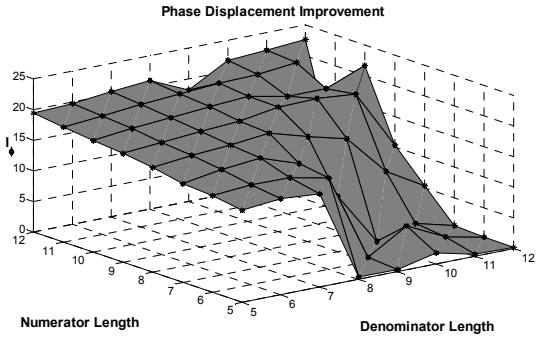

Figure 5. Improvement of phase displacement as function of numerator and denominator lengths

B. Compensation results

The identified digital filter, whose coefficients are shown in Table 1, has been implemented in FPGA board and the compensated CT has been characterized through the previously described automated measuring station. The same tests reported in sec. III have been performed.
Ratio error and phase displacement of compensated CT are shown in Figure 6. It can be seen that phase displacement of compensated CT is worse than uncompensated one: this is due to the fact that compensating device introduces a time delay related to A/D conversion, filtering and D/A conversion, and it adds a phase displacement, linear function of frequency, to the output of compensated CT. Total time delay has been measured and it is equal to 10.55 μs. Obviously, since it is constant, it can be eliminated in post-processing.
In Table. 2 mean quadratic values for ratio errors and phase displacements of uncompensated and compensated CTs and compensation improvements are reported. In it, *S* refers to simulation values, *M* to measurement values, *IS* is the improvement in simulation, *IM* the improvement in measurement, *IMpp* the improvement in measurement with data post-processing. Improvement in ratio error is approximately the same both in simulation and measurement. As it is said before, phase displacement has a worsening due to the time delay of compensating device; if the output of compensated CT is post-processed the improvement both in simulation and measurement is approximately the same.

V. Conclusions

In this paper a real-time digital technique for the compensation of current transformers in the frequency range of 10 Hz – 10 kHz, based on field programmable gate array, has been presented. It is based on the identification of a digital filter with a frequency response equal to the inverse one of CT. Once the CT has been metrologically characterized, thus finding its frequency response, filter coefficients are found through the optimization procedure; the compensated CT continues to be an analog device since it is obtained cascading the CT with an FPGA board, opportunely equipped with analog to digital and digital to analog converters, which implements the digital filter. Experimental results have shown that the compensated CT improves performances of the original CT; ratio error steps up of a factor 24.1.

Table 1. Coefficients of compensating digital filter

b_k	a_k
1.747893	1.000000
0.544851	-0.010405
-0.162473	1.006314
0.000000	0.000017
-0.002149	0.446846
0.510690	-0.012168
0.805931	0.575127
0.358222	0.034914
0.265825	0.750312
0.101732	0.030656
-0.055858	0.279981
0.134157	0.137621

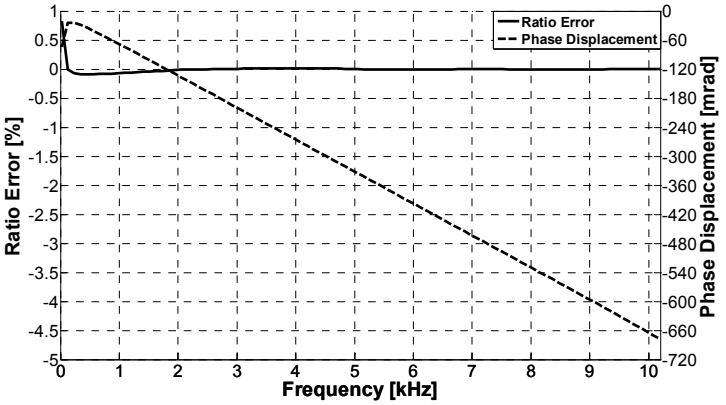

Figure 6. Ratio error and phase displacement of compensated CT

Table 2. Compensation improvements in ratio error and phase displacement

	Ratio error				Phase displacement				
	S [%]	*M* [%]	*IS* [p.u.]	*IM* [p.u.]	*S* [mrad]	*M* [mrad]	*IS* [p.u.]	*IM* [p.u.]	IM_{PP} [p.u.]
CT	2.17	2.17	24.4	24.1	173.1	173	22.8	0.44	22.7
Comp. CT	0.089	0.090			7.6	391.6			

Regarding phase displacement, it grows worse due to the presence of a time delay introduced by compensating device: since this time delay is constant it can be eliminated post-processing the output of compensated CT, reaching this way improvement factor of 22.7 also in phase displacement.
The presented technique, other than improving CT performances in a large frequency bandwidth, is effective also from another point of view: the improvement is obtained adding to CT a low cost device, increasing a little total CT cost. A CT with the same performance of the compensated CT has a cost larger than the original one about improvement factor obtained with compensation.
Future works will regard the enhancement of mathematical formulation of identification procedure, in order to account the phase displacement due to time delay of compensating device.

References

[1] "IEEE Standard Requirements for Instrument Transformers", IEEE Std. C57.13-1993, 1994.
[2] "Instrument Transformers-Part 1: Current Transformers", IEC Std. 60044-1, 2000.
[3] EN 50160, "Voltage characteristics of electricity supplied by public distribution systems", CENELEC, 1999.
[4] IEC EN 61000-4-30: "Testing and measurement techniques – Power quality measurement methods", 11/2003.
[5] Daponte, P.; "Electronically compensated current transformer modeling", Measurement, 15 (4), p.213-222, Jul 1995.
[6] Baccigalupi, A.; Liccardo, A.; "Compensation of Current Transformers", Instrumentation and Measurement Technology Conference Proceedings, 2007 IEEE, 1-3 May 2007.
[7] Slomovitz, D.; "Electronic system for increasing the accuracy of in-service instrument-current transformers", Instrumentation and Measurement, IEEE Transactions on, Volume 52, Issue 2, April 2003 Page(s):408 - 410
[8] Douglass, D.A.; "Current Transformer Accuracy with Asymmetric and High Frequency Fault Currents", IEEE Transactions on Power Apparatus and Systems, Volume PAS-100, Issue 3, March 1981 Page(s):1006 – 1012
[9] A. Delle Femine, D. Gallo, C. Landi, M. Luiso, "A technique for real-time correction of measurement instrument transducers frequency responses", International Instrumentation and Measurement Technology Conference Proceedings, 2008 IEEE, May 12–15, 2008.
[10] J. Kaipio, E. Somersalo, "Statistical and Computational Inverse Problems", *Applied Mathematic Sciences*
[11] K. Deb, "Multi-Objective Optimization using Evolutionary Algorithms", *Wiley*
[12] D. E. Goldberg, "Genetic Algorithms in Search, Optimization, and Machine Learning", *Addison Wesley*
[13] Coleman, T.F. and Y. Li, "An Interior, Trust Region Approach for Nonlinear Minimization Subject to Bounds," *SIAM Journal on Optimization*, Vol.6, pp. 418-445, 1996