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Electrochemical Impedance Spectroscopy Analyzer with Digital Potentiostat

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Abstract- The paper presents a prototype of EIS analyzer, which uses digital potentiostat/galvanostat. The separate paths and AD converters were used for sampling DC and AC components of signals proportional to current through and voltage across the impedance of the measured object. The converters are controlled by different processors, which performs functions tightly connected with realization of two tasks of EIS analyzer: potentiostat/galvanostat controlling and impedance measuring. In order to decrease the influence of the real-life parameters of used operational amplifiers and the parasitic capacitances on the error of impedance measurement, the correction taking those parameters into account has been used in the algorithm for determination of impedance parameters of the measured objects. Performed tests proved benefits appearing from correction implemented in the algorithm. The impedance measurement results of an example non-linear RC object with diode show that the relative error of modulus doesn't exceed +0.5/-1.0% and absolute error of argument was not greater than ±0.5°.

I. Introduction

Electrochemical impedance spectroscopy (EIS) is one of the most commonly used research methods for physico-chemical objects [1]. The instrument for EIS consists of potentiostat used for polarization of the tested object and impedance analyzer allowing to measure impedance spectra. On the basis of the measured impedance parts ($\mathrm{Re}Z_x$, $\mathrm{Im}Z_x$), the parametric identification of the object equivalent circuit is done. The equivalent circuit most commonly is given as multi-element two-terminal network containing from a few to several components. For the parametric identification, the CNLS method is used. The method is based on fitting object model parameters to the impedance spectrum [2].

The main difficulties of EIS realization lie in the measurement process. In case of multi-element models, the impedance measurements have to be done in a wide frequency range from relatively high (of an order of MHz) to very low (even down to 100 μHz). The additional problem is wide range of the measured impedance from below Ω to hundreds of MΩ. For EIS measurements, it is also important to assure the condition of the constant potential on the measured impedance Z_x, while simultaneously exciting the object with harmonic signal.

In the worldwide market, there are offered impedance analyzers from well-known manufacturers: Solartron (set: FRA 1255 or 1260 + electrochemical interface 1287) [3], Novocontrol (Material Analyzer BETA) [4], Zahner (Electrochemical Workstation IM6) [5]. For vector measurement of impedance, they are using analog phase-sensitive detection, which disadvantage is long measurement time especially at low frequencies. The available potentiostats and galvanostats are also based on analog technique. The consequence of this is high complexity of the EIS instrumentation which leads to high price (e.g. Solartron FRA 1255 + 1287 cost ca. 25000 GBP). Due to above reasons, there is the need of development of low-cost impedance analyzers with potentiostat/galvanostat functions.

To reach the target, the authors have developed EIS analyzer, in form of measurement module, designed to operate with personal computer. The new solutions have been used e.g. digital realization of potentiostat/galvanostat and digital signal processing (DSP) technique for measurement signal orthogonalization instead of analog phase-sensitive detection.

II. Standard circuit of potentiostat/galvanostat

The measurements of electrochemical objects require to assure specified measurement conditions. To set required value of potential or required value of current flowing throw the electrochemical cell the

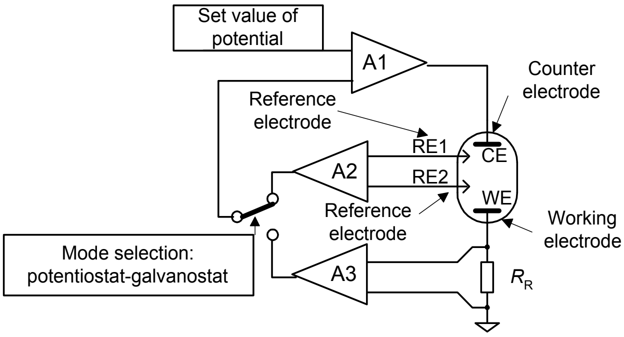

Figure 1. Block diagram illustrating how potentiostat/galvanostat works

potentiostats and galvanostats using analog negative feedback-loop are used. Standard circuit illustrating rule of potentiostat/galvanostat work [6] is shown in Fig. 1.

The value of the potential to be set is obtained as a sum of DC voltage setting the measurement condition and sinusoidal voltage used to measure impedance. Amplifier A1, thanks to feedback-loop, extorts current flow at the level necessary to keep potential between reference electrode (RE1) and working electrode (WE) at the programmed value (potentiostat mode) or sets the voltage to assure the cell current at the required level (galvanostat mode).

Amplifier A2, with high input impedance, measures voltage between reference electrodes RE1 and RE2 (when measuring using 3-electrode connection, RE2 electrode is connected to WE electrode thus eliminating the influence of the voltage drop caused by current flowing to WE electrode). Amplifier A3 measures voltage across reference resistor R_R, proportional to current flowing throw the electrochemical cell (R_R is changed decadely to set the range of the current measurement). Both signals can contain DC component (due to the operation point), as well as AC component (due to the impedance measurement).

The solution used for polarization of the tested object is based on analog negative feedback-loop and frequently leads to instability of the potentiostat circuit thus requiring limitation of the bandwidth of amplifier controlling CE electrode. To eliminate this unwanted phenomenon, the developed EIS analyzer realizes digitally controlled potentiostat setting required value of DC potential and amplitude of harmonic signal using D/A converters.

III. Architecture of the EIS analyzer

Assuming conception of digital potentiostat and an idea of impedance measurement based on DSP technique, the EIS analyzer was developed. The architecture of the analyzer is shown in Fig. 2. The analyzer contains excitation signal u_g generation path and two identical paths for processing of signals u_u and u_i extracted in input circuit. The signals u_u and u_i are proportional to voltage between electrodes RE1 and RE2 and to current flowing to electrode WE. In the generation block the sinusoidal signal is prepared using direct digital synthesis with the aid of DAC 1 and DC offset is prepared using DAC 2.

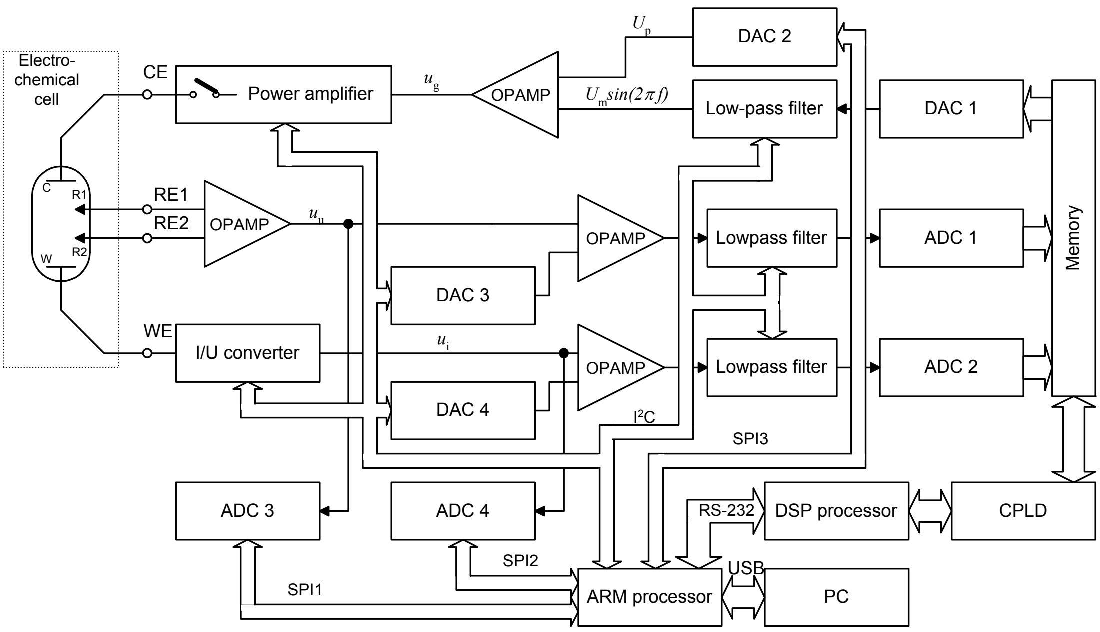

Figure 2. Block diagram of the EIS analyzer

The separate paths and A/D converters were used for sampling DC component of signals u_u (ADC 3) and u_i (ADC 4) and AC component (ADC 1 and ADC 2). D/A converters (DAC 3 and DAC 4) eliminating DC offset in both signals have been used for processing of AC signals, because DC offset is usually much greater than AC component amplitude does not allow to optimally select measurement range of A/D converters for harmonic signals. In order to avoid aliasing phenomenon, in AC paths low-pass filters with programmable limit frequency have been used. A/D converters for DC signals are controlled by ARM processor by SPI1 and SPI2 interfaces but converters sampling AC signals are controlled by DSP processor.
The assumed task allocation between processors is closely related to realization of two functions of the EIS analyzer – servicing of potentiostat/galvanostat circuits (processor ARM) and impedance analyzer (DSP processor). Additional task of ARM processor is communication with PC computer via USB interface. The method of the measure of the impedance parts of the tested object using discrete Fourier transformation (DFT) was implemented in DSP processor [7]. Below, main step of algorithm of impedance measurement were presented.

A. Impedance measurement algorithm

On the basis of two set of samples of harmonic signals u_i and u_u, acquired by converters ADC 1 and ADC 2 (with sampling frequency f_s), the DFT transform is calculated on the basis of definition by signal processor. As a result, discrete representation of sampled signals in frequency domain is obtained. These are sets U_i and U_u, respectively, which k line can be described by equations:

$$U_i[k] = U_i(k \cdot \Delta f) = \sum_{n=0}^{N-1} u_i[n] \cdot e^{-jk\frac{2\pi}{N}n}, \quad U_u[k] = U_u(k \cdot \Delta f) = \sum_{n=0}^{N-1} u_u[n] \cdot e^{-jk\frac{2\pi}{N}n}, \tag{1}$$

where: $k = 0,1,...N-1$, N – number of acquired samples,
$\Delta f = f_s/N$ –frequency resolution of the spectrum.

To obtain simple algorithm of DFT calculation and to avoid spectrum leakage, CPLD programmable circuit was used assuring synchronous generation of signal u_g (strobing od DAC 1) and sampling of the measurement signals by ADC 1 and ADC 2 converters. This way, the condition that the acquisition is performed in integer number of periods of the measurement signal (2) is fulfilled,

$$N \cdot T_s = l \cdot T \ , \tag{2}$$

where: T – measurement signal period, l – integer number (1-10000), $T_s = 1/f_s$.

what means that, for sinusoidal signals u_i and u_u, frequency spectra contain only one, non-zero line (l).
At the end of each measurement cycle, signal processor calculates also modulus and argument of measured impedance on the basis of the following formulas:

$$|Z_x| = R_R \left| \frac{U_u[l]}{U_i[l]} \right|, \quad \varphi_{Z_x} = \arg\left(\frac{U_u[l]}{U_i[l]} \right), \tag{3}$$

where: R_R – reference range resistor in I/U converter, performing conversion of the current flowing to WE electrode to voltage u_i.

B. Measurement cycle of the analyzer

The measurement process starts when set of given measurement points: measurement frequency f (sorted form highest to lowest), value of polarization U_p and the amplitude of sinusoidal signal U_m is written to memory of the analyzer.
At the first stage the DC condition of the measurement is determined. It was assumed that the object contains electrochemical cell, so in the fist step, when CE electrode is disconnected, the measurement of the open circuit polarization E_{oc} is performed by ADC 3. The obtained value after summing with the first given polarization U_p is used for programming DAC 2. Next, the CE electrode is connected and the measurement of DC component is repeated by ADC 3, allowing to enter correction in DAC 3, in order to obtain required value of DC polarization on the object ($E_{oc} + U_p$).
At the second stage, after measurement of DC component by converters ADC 3 and ADC 4, the compensation of the DC offset is performed in each AC channel using converter DAC 3 and DAC 4.
At the third stage, the correct impedance range is selected using resistors R_R. To do this, the given

measurement amplitude and frequency is programmed and the value of range resistor is increased (or decreased) to keep signal u_i in assumed range $<u_g^L, u_g^H>$, resulting from the range of the ADC 2.
At the fourth stage, the correction of the AC amplitude set coarsely at the second stage and the correction of the DC polarization set at the first stage is performed. The measurement of AC and DC components is performed and after calculations taking into account existing voltage divider the correction of the amplitude and the polarization is applied.
At the last stage, signal processor determines real and imaginary parts of impedance, and next the procedure is repeated for other measurement frequencies. After determining impedance spectrum for all selected measurement frequencies, the next value of DC polarization of the object is set and the algorithm is repeated from beginning.

III. Correction of the determined impedance parameters

The greatest influence on the accuracy of the determination impedance parameters of the measured object has the input circuitry of the EIS analyzer presented in Fig. 3. The object was connected using four-terminal connection with shielded cables. The influence of the capacitance of the cable shield on the Z_x measurement is eliminated by assuring almost-zero voltage between a hot-wire and a shield with the aid of voltage followers realised with operational amplifiers. To measure the current flowing through the Z_x the range resistor R_R changed decadely in a range of 0.1 Ω ÷ 10 MΩ has been used. The values of the R_R are selected in relation to $|Z_x|$ according to criterion: $0.01\ |Z_x| < R_R \le 0.1\ |Z_x|$. The fulfilment of the condition means that the resistance R_R is lower by at least order than $|Z_x|$. It is profitable solution due to decreasing common signal for differential amplifier of voltage across the measured impedance Z_x, but the solution causes the need of additional amplification (20 times) of signal across the resistor R_R. This way, the amplitude of signal u_i is comparable to the amplitude of u_u, taken directly by voltage followers and differential amplifier across the measured impedance Z_x.

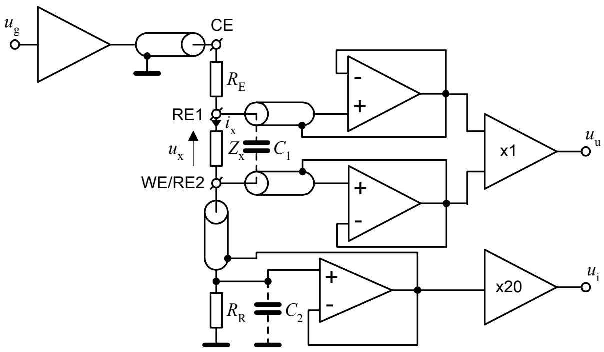

Figure 3. Block diagram of the input circuitry of the EIS analyzer

The use of formula (3) to determine parameters of the measured impedance is correct under condition that signals u_i and u_u extracted in the input circuitry, and than converted to digital representation are dependant only on current i_x through and voltage u_x across the Z_x. The performed analysis of the input circuitry shows that signals u_i and u_u are affected by unwanted parameters causing errors of the impedance measurement. The strong dependence of error of impedance modulus and argument on parameters of transfer function of the amplifier with gain equal to 20 in current measurement path and on parasitic capacitance (C_2) shunting range resistor R_R and parasitic capacitance (C_1) existing in parallel to the measured object (between terminals RE1 and RE2). So, there is a need of taking into account the real-life parameters of the input circuitry, which correct the extracted signals u_i and u_u. Taking into account the influence of main sources of errors, the formula for Z_m calculation was derived:

$$Z_m = \left(\frac{\dfrac{1}{R_R} + j\omega C_2}{\dfrac{20}{1+21/A_u}\dfrac{U_u}{U_i}} - j\omega C_1 \right)^{-1}, \tag{4}$$

where: C_1 – the sum of layout capacitance and not completely eliminated influence of capacitance of shielded cables,
C_2 – the sum of input capacitances of voltage followers and reed relays used to change current

measurement range by changing R_R value and layout capacitances,

$A_u = \dfrac{A_{DC}}{1 + j\dfrac{\omega}{\omega_{3dB}}}$ - is single-pole (ω_{3dB}) transfer function [8] of amplifier with gain equal to 20,

A_{DC} – open-loop DC gain of amplifier.

It was assumed, that the gain of the voltage followers is equal to 1 in the analyzed frequency range. The assumption results from fulfillment of the following conditions:

- The unity-bandwidth of the amplifier is a few tens times greater than the maximum measurement frequency,
- The voltage followers are realized using the same amplifiers and thanks to calculation of the ratio of the signals in both paths, the elimination of gain-errors can be obtained.

In the differential amplifier and in the amplifier with gain equal to 20, the resistors with 0.01% tolerance and 5ppm/°K temperature coefficient were used, assuring negligible influence on the error of impedance measurement.

In order to show benefits appearing from the use of formula (4), the reference (0.01%) 1 kΩ and 1 MΩ resistors were measured using EIS analyzer and the modulus and argument of their impedance were determined using equations (3) and (4). In formula (4) the parameters C_1, C_2, ω_{3dB} and $A_{DC,}$ on the basis of the analysis of the input circuitry realized with amplifiers OPA627. Because for OPA627 $f_{3dB} = 20$ Hz, $A_{DC} = 800000$, differential capacitance is 8 pF and common capacitance is 7 pF, after estimation of layout capacitances, it was assumed that $C_1 = 4$ pF and $C_2 = 20$ pF. The relative error of modulus and absolute error of argument of impedance for both cases is presented in Fig. 4.

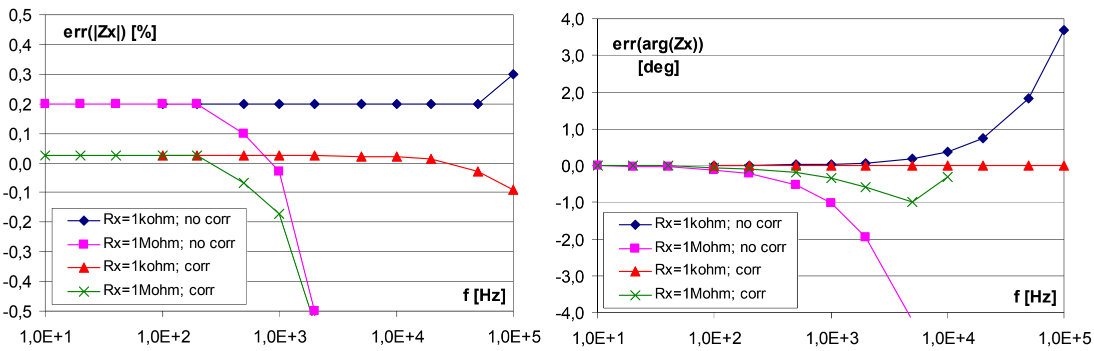

Figure 4. The relative error of modulus and absolute error of argument of the impedance of resistors 1 kΩ and 1 MΩ

When analyzing graphs it can be noted, that the usage of (4) gives much better improvement of the accuracy in case of resistor 1 kΩ than in case of resistor 1 MΩ. This is a result of much lower influence of capacitances C_1 and C_2 on the measurement accuracy when measuring low impedance (100 Ω), and only the parameters of a amplifier with gain equal to 20 are influencing the measurement accuracy and only for frequencies greater than 1 kHz.

Resuming, the proposed formula (4) significantly increases the impedance measurement accuracy and was implemented in the software of PC computer controlling the EIS analyzer.

V. Experimental results

The tests of the realized EIS analyzer were performed. Example results in 3-terminal connection (connected terminals WE and RE2 at working electrode) of the measurement of non-linear object with diode and RC components shown in Fig. 5 were presented in Fig. 6 as Bode plot. The measurements were performed in series of 10 measurement at each frequency and for 4 values of DC polarization: 0 mV, 200 mV, 400 mV, 600 mV with 20 mV AC amplitude.

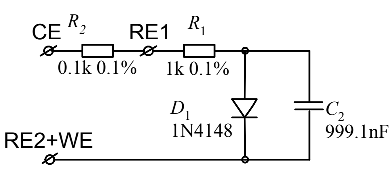

Fig. 5. Non-linear test object with diode and RC components

In order to compare obtained results (on the basis of (3)) with theoretical characteristics of the tested object simulated with Spice, the errors of the impedance measurement were determined. Relative error of impedance modulus measurement does not exceed ±1,5%, and a absolute error of impedance argument ±2°, respectively, in a whole range of the measurement frequency. Highest values of the error have appeared at high band of measurement frequencies (> 1 kHz) and are caused by parasitic capacity in the input circuit of the analyzer and phase shift entered by amplifiers in I/U converter. Using formula (4), which takes into account real-life parameters of input circuitry, the increase of measurement accuracy was obtained, because the impedance modulus error doesn't exceed +0.5/-1.0%, and impedance argument error ±0.5°, respectively, in the measurement frequency range from 10 Hz to 100 kHz.

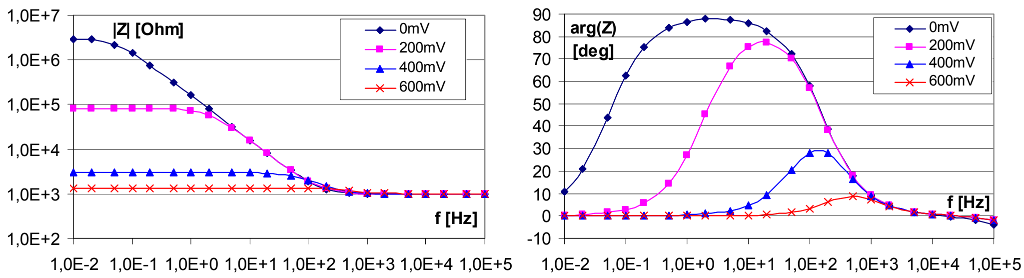

Figure 6. The results of the measurement of test object from Fig. 5

VI. Conclusions

The developed and realized prototype of the EIS analyzer can characterized by the following features:

- Impedance measurement range 0.1 Ω<$|Z_x|$<100 MΩ (in 8 subranges);
- Measurement frequencies range of impedance spectroscopy 100 μHz to 100 kHz;
- DC polarization (in potentiostat mode) programmed in range of ±10 V with 16-bit resolution (current up to ±1A in galvanostat mode);
- Amplitude of the measurement signal programmed in range 1 mV÷1 V (with 1 mV step).

The analyzer uses new circuit and software solutions. It can be found in phase-sensitive detection , where DFT was used for determination of the orthogonal parts of measurement signals and digital mode of potentiostat/galvanostat extorting programmed value of DC offset and amplitude of harmonic signal with the aid of D/A converters. The use of DSP technique to determine components of measurement signals allows to obtain wide range of measurement frequencies, especially very low (from 100 μHz), assuring simple construction of the analyzer.

A formula for determination of the measured impedance was implemented in the PC software controlling EIS analyzer. The formula takes into account the real-life parameters of the input circuitry and performs a correction to decrease the influence of parasitic capacitances and real parameters do used operational amplifiers on the accuracy of impedance measurement. The performed tests proved benefits arising from the usage of the correction, because the relative error of impedance modulus doesn't exceed +0.5/-1.0% and the absolute error impedance argument was not greater than ±0.5° in the whole measurement frequencies range from 10 Hz to 100 kHz.

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