ESD Immunity Tests in System Designs

LucianToma[1], Alexandru Salceanu[1], Mihai Cretu[1]

[1] "Gh. Asachi" Technical University, Department of Electrical Measurements and Materials, Bd. Mangeron, nr. 53A, 700050 Iasi , Romania

Abstract: Soft errors as well as damage can be caused by ESD in electronic systems. Such effects have resulted in many problems with companies and customers incurring large costs. Effects on system immunity from printed wiring board layout will be covered and examples of field problems described. Suggestions on how to avoid such problems are given.

I. Introduction to ESD tests

The influence of design at the circuit board and system level on ESD immunity of electronic systems is well documented. However, designers are often forced by cost, time to market, and space limitations to make compromises. Hard data and real experiences on the impact of ESD immunity of circuit board and system design make it easier for designers to make a case to include needed design features.

Data is presented below on two test boards that graphically illustrate how strongly board layout can affect ESD immunity. In addition, experiences in the field are given which reinforce the importance of good design.

A. Diving Path Test Board

Figure 1 shows a test board that is double sided copper with two test paths. The paths are about 30 cm in length. One path is routed from an SMA connector to a 47Ω load and the other crosses through the two ground planes and travels one third of the distance on the opposite side of the board before reaching the load resistor. The two ground planes are connected together at the SMA connectors and at the load resistors. Small gauge copper wire held in place by tape forms the paths which have a nearly 50Ω characteristic impedance.

ESD current from a 3 kV contact discharge is injected onto the ground plane as shown in Figure 1 at the right edge of the board and exits from the left side.

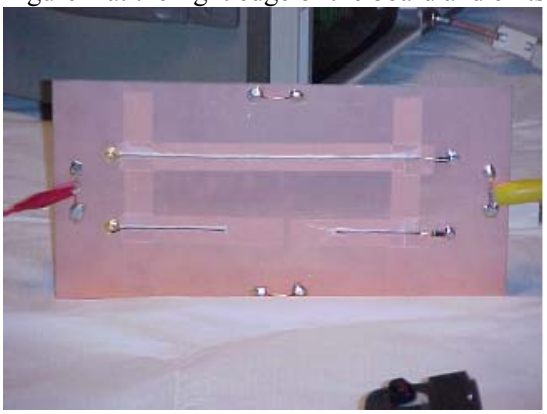

Figure 1. Test Board with Two Test Paths

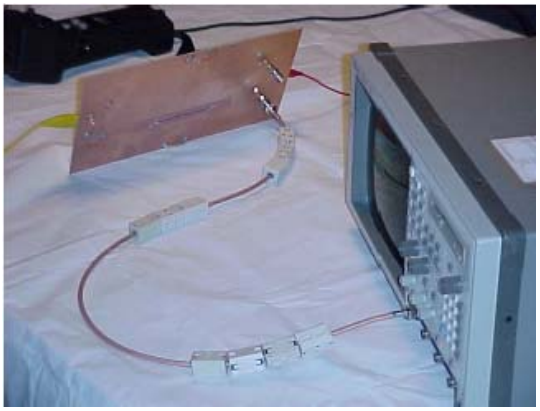

Figure 2. Connection to Oscilloscope

Figure 2 shows the back of the board and the connection to the scope. Ferrite cores are used to prevent ESD current from diverting to the coaxial cable and the scope chassis. Figure 3 shows the complete test setup.

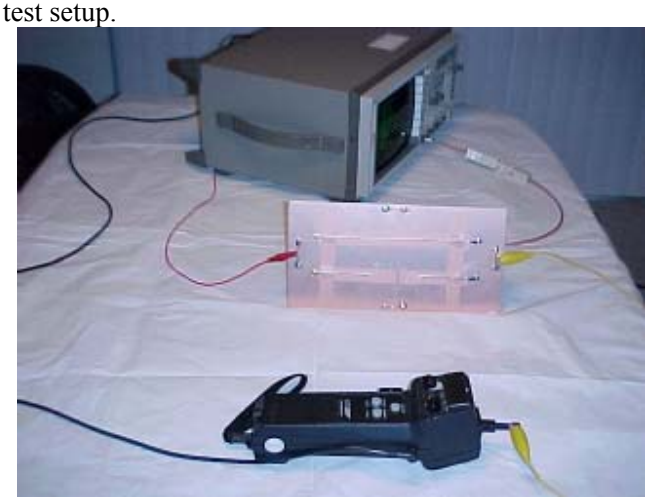

Figure 3. Complete Test Setup

Figures 4 and 5, respectively, show the apparent signal generated by the ESD across the 47Ω loads for the straight path and the path that crosses through the ground planes. The difference between the two cases is striking.

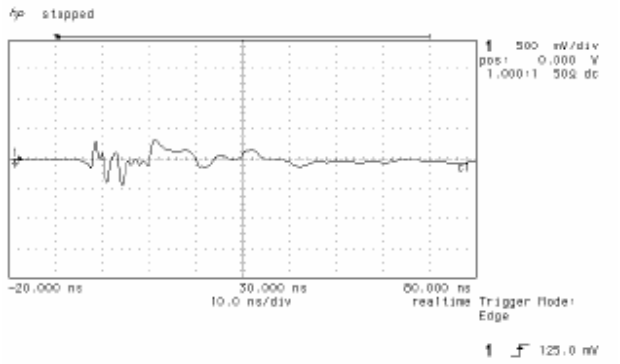

Figure 4. Apparent Signal on Straight Path

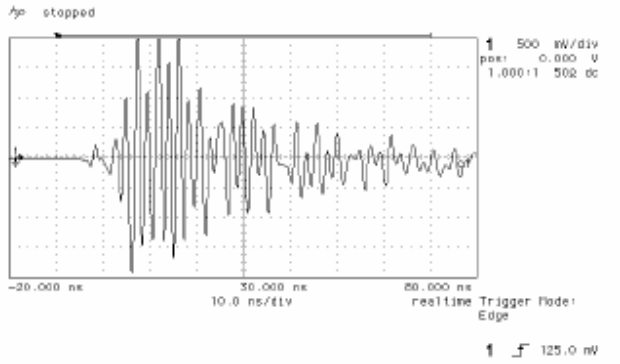

Figure 5. Apparent Signal on Path Crossing Planes

The interference generated in the straight path, Figure 4, was less than 500 millivolts. In the path crossing through the ground planes, the interference was greater than 2 Volts! That value is easily enough to corrupt a 5 volt logic signal.

Crossing through two ground planes (or any conducting planes) puts the interplane impedance in the return path of the signal loop formed by the signal path and its return in the ground plane. As can be seen, this can be a significant effect.

B. Split Plane Test Board

Figure 6 shows the board use for the test. Construction was similar to the previous test except than one of the paths crossed a break in the ground plane. The board was about 20 cm in length.

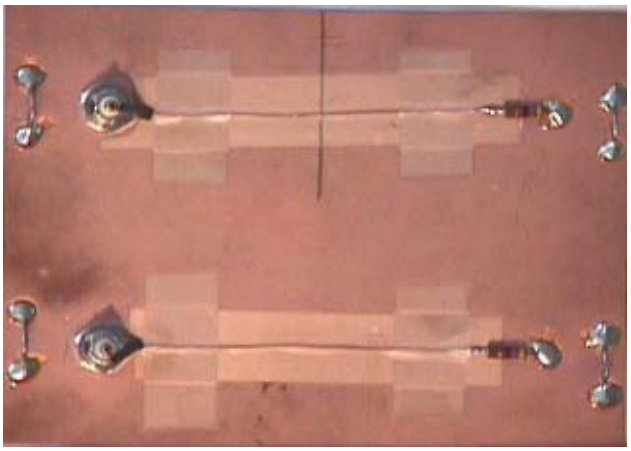

Figure 6. Split Plane Test Board

The test setup is also similar to the first test and is shown in Figure 7. The ferrites used to prevent the ESD current from ending up on the front of the scope are plainly visible. Figure 8 shows the interference into the straight path from a 4 kV contact discharge. The amplitude is about 300 mV peak, not enough to be a problem for most logic families.

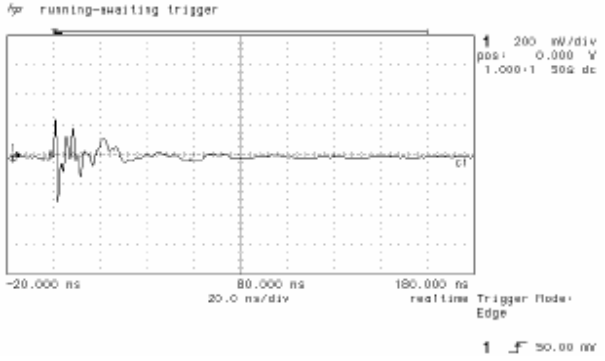

Figure 8. Apparent Signal on Straight Path

Figure 9 shows the interference to the path crossing the break. The amplitude has increased to about 3.5 volts, enough to corrupt most any logic signal!

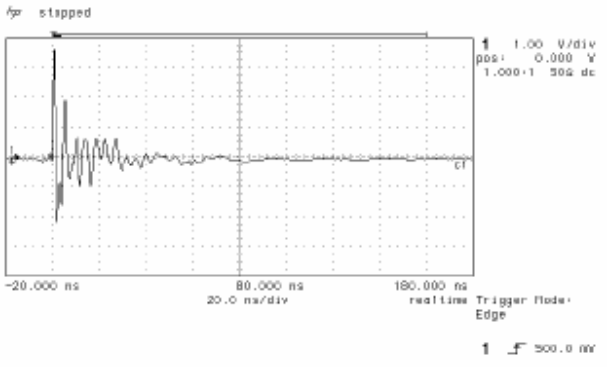

Figure 9. Apparent Signal on Path Crossing Planes

The reason for the large increase is that the signal and it's return path form a large loop. The ESD current must share part of the loop with the signal return. The common part of the loop is on the ground plane around the end of the slit.

II. Conclusions and Summary

Data and examples have been presented that show how important good design practices are to the ESD immunity of an electronic system. Often these design practices are very inexpensive or even free if included early in system design. However, added after the design is complete or in production, these techniques can add significant cost and schedule delays to a system. The authors hope that this paper raises awareness of these issues in the design community.

References

[1] Douglas C. Smith, *High Frequency Measurements and Noise in Electronic Circuits*
[2] Michael Mardiguian, *Electrostatic Discharge: Understand, Simulate, and Fix ESD Problems*, 2nd Edition 1992, Interference Control Technology, Inc. Gainsville, VA
[3] Moyer T., Gensel R., Kunkel H., *Update on ESD testing according to 61000-4-2*, EM Test.
[4] Colectiv internațional, 2002, Electromagnetic Compatibility. Theory Manual (capitolul 8, "ESD & Transient Problems" şi capitolului 12, "ESD & Transient Tests"), Warwick University Press
[5] Colectiv internațional, 2002, Electromagnetic Compatibility. Practical Manual (capitolul 4, "EMC Management & Company Awareness"), Warwick University Press