Nonlinear voltage divider

As. Ing. C. Dughir[1], Prof. Dr. Ing. A. Ignea[2], As. Ing. G. Găşpăresc[3],
Sl. Dr. Ing. A. Vârtosu[4]

[1] *"Politehnica" University of Timisoara, Electronics and Telecomunications, V. Pârvan 2A, 30022, Timisoara, Romania, +40256403365, ciprian.dughir@etc.upt.ro*
[2] *"Politehnica" University of Timisoara, Electronics and Telecomunications, V. Pârvan 2A, 30022, Timisoara, Romania, +40256403365, alimpie.ignea@etc.upt.ro*
[3] *"Politehnica" University of Timisoara, Electronics and Telecomunications, V. Pârvan 2A, 30022, Timisoara, Romania, +40256403365, gabriel.gasparesc@etc.upt.ro*
[4] *"Politehnica" University of Timisoara, Electronics and Telecomunications, V. Pârvan 2A, 30022, Timisoara, Romania, +40256403365, adrian.vartosu@etc.upt.ro*

Abstract - This paper is focused on how to implement a nonlinear voltage divider used in the electrical power network disturbances measurement system preconditioning circuit. The voltages acquired from the electrical power network have amplitudes between 0.2 kV and 10 kV, values which are very high for an acquisition board. These amplitudes must be reduced to the values accepted by the acquisition boards: ±10V. If the signal from the electrical power network is divided with a linear voltage divider, the smaller variations around the nominal values of the voltage on the electrical power network can not be detected. This is the reason to prefer the use of a nonlinear voltage divider.

I. Introduction

The main problem in the electrical power systems is monitoring and detecting the disturbances. Because the multitudes of types the disturbances are, each disturbances with her specificity, it's difficult to detect and capture such types of disturbances. The common types of disturbances are that can produce little variations of the power system voltage around 230V. Another type of disturbances is the disturbances with amplitudes over 2 kV and under 10 kV, caused by lightings. These specifically types of disturbances are very dangerous for the equipments connected to the electrical power network, causing malfunctions or, in the worst cases making the equipments out of service.

II. The Method

The method proposed in this paper use three linear voltage dividers and three channels of an acquisition board to emulate a nonlinear voltage divider.
The signal from the electrical power network is applied to the inputs of three voltage dividers, each of them having a different division ratio. The outputs of the dividers are limited to ±10V and then are applied to the three channels of an acquisition board. The bloc diagram of the circuit is presented in Figure 1.

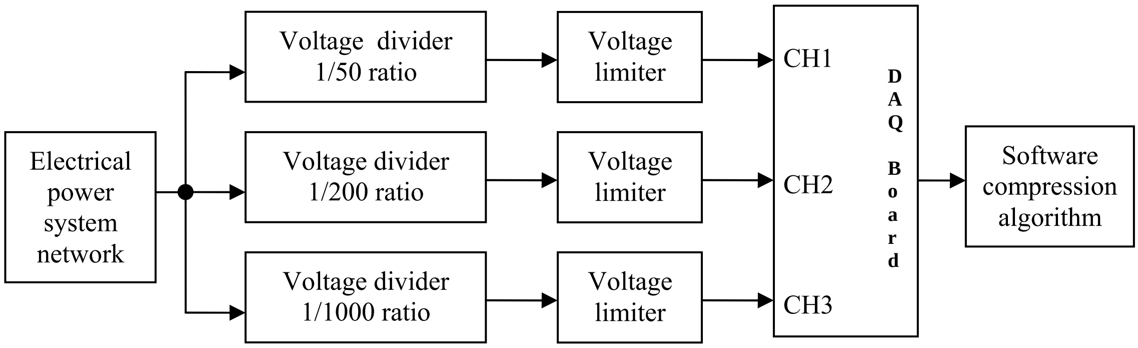

Fig. 1. Bloc diagram of the nonlinear voltage divider

The voltage limiter circuit is used because the maximum supported voltages applied to the acquisition board are ±10V. The acquisition board make itself hardware and software limitation to ±10 V for the signals out of the input range. The limitation circuit is still required because the high voltage values that can appear at the output of the voltage dividers. For example, if a signal with 10 kV amplitude is applied to the input of the first voltage divider, the output value will be 200 V, value too high to be applied at the input of the acquisition board.
The transfer function of the three voltage dividers is shown in the Figure 2. All three signals from the voltage dividers are limited to a constant value C = 10V. To simplify the presentation, the algorithm is presented only for positive input signals, the algorithm being similar for the negative input signals.

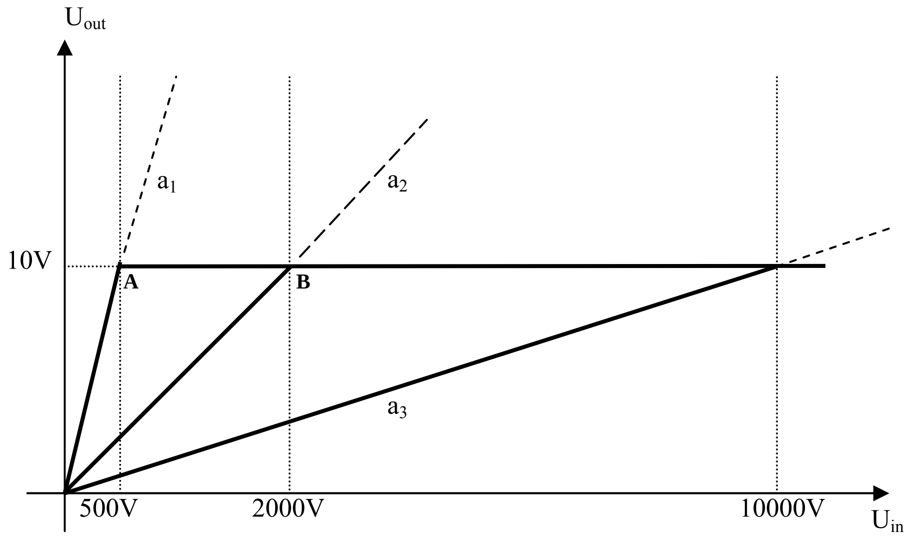

Fig. 2. Transfer function of the voltage dividers

In the Figure 2, a1, a2 and a3 are the slopes of each voltage divider transfer functions. The A point is the intersection between the second voltage divider transfer function and the line x=500V, the B point is the intersection between the third voltage divider transfer function and the line x=2000V. If is considered the A point being characterized by (x1, y1), and the B point characterized by (x2, y2), it can translate the second transfer characteristic with C1 = 10V-y1, and the third transfer characteristic with C2 = C1 + 10V - y2, resulting the characteristic presented in the Figure 3. A supplementary software processing is required in order to remove the unwanted portions of the transfer characteristic. This is realised by the compression algorithm presented in the Figure 4.

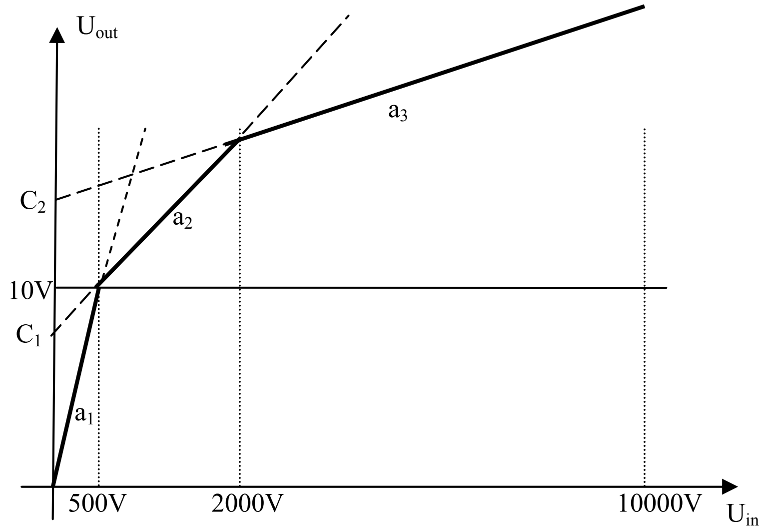

Fig. 3. Transfer function of the nonlinear voltage divider

Using a software algorithm the signals from the three input channels can be merged in a single signal with a nonlinear transfer function presented in the Figure 3.
The software algorithm calculate the values of C1 and C2 constants, and then acquire a sample on each of the three channels, the samples are then processed and as the result is obtained a compressed signal with the transfer function as in the figure 6a. The values of the first cannel are used on their entire voltage range, the second channel values are used only in the 0.5 kV – 2 kV range, and the values of the third channel are used only in the 2 kV – 10 kV voltage range. This can decrease the performance of the voltage divider.

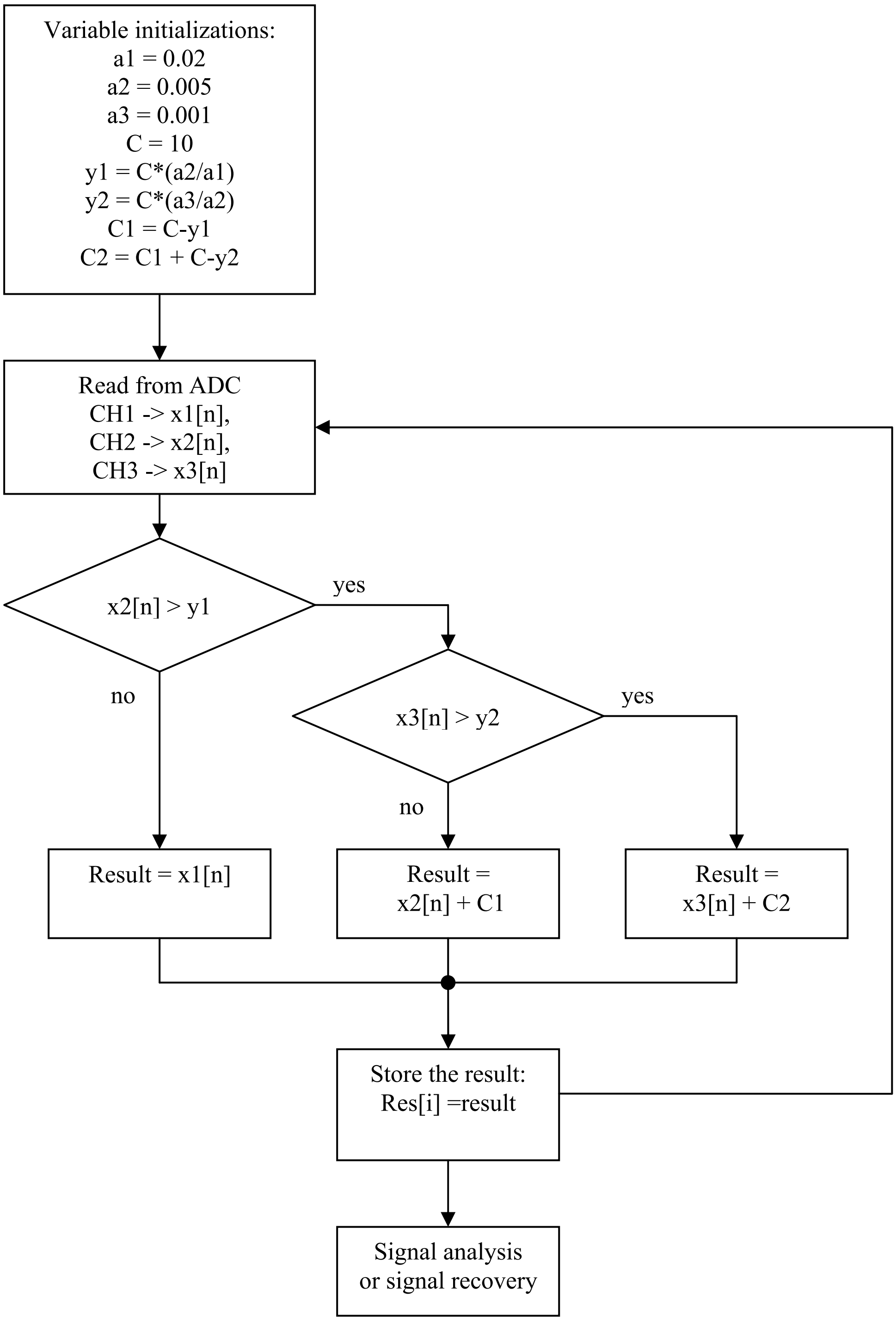

Fig. 4. The nonlinear voltage divider signal compression algorithm.

The signal form the output of the software compression module can be used as it is, or can be decompressed for easier use. The decompression algorithm can be applied to the compressed signal or can be implemented in the software algorithm that makes the signal analysis. The reconstruction algorithm is presented in the Figure 5.
The output signal can be easily recovered to its initial shape by applying an inverse function to the nonlinear voltage divider output signal.

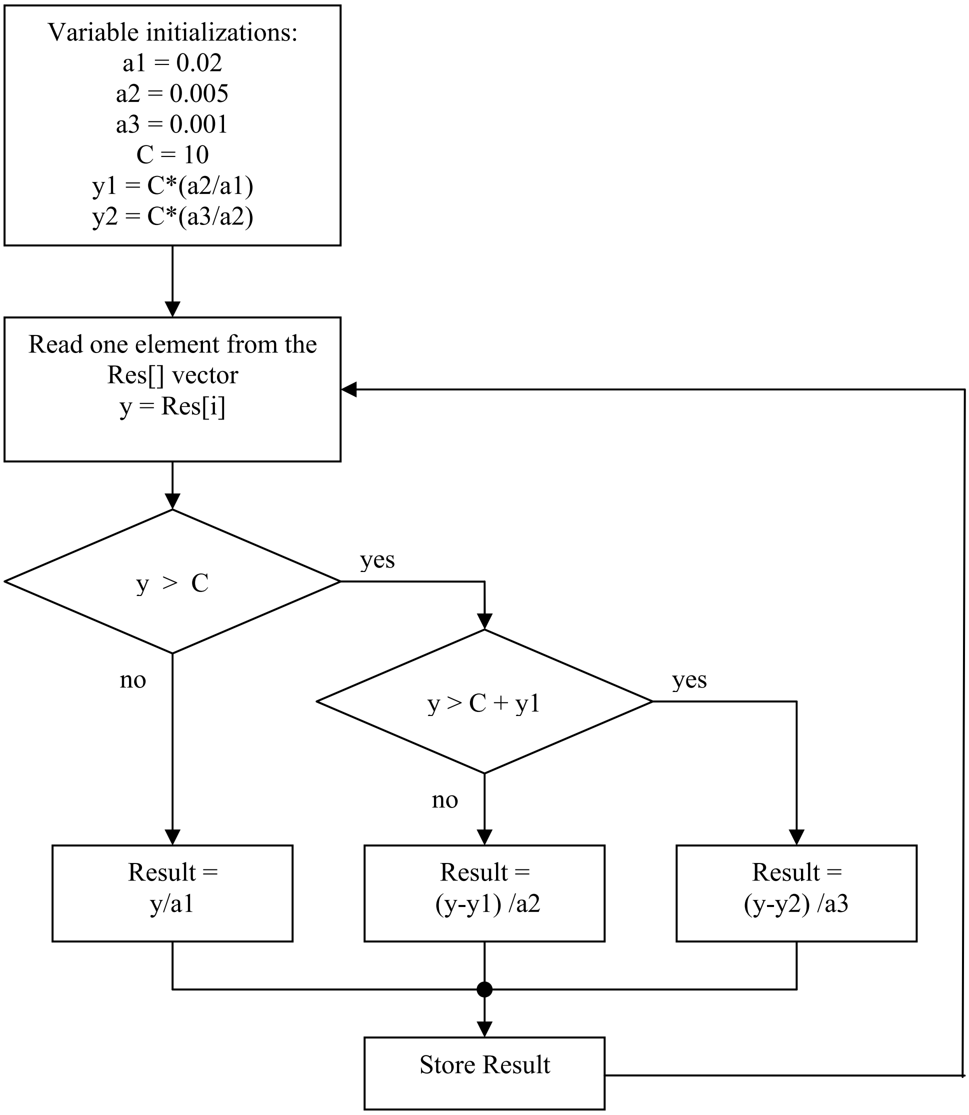

Fig. 5. The algorithm for the reconstruction of the signal

III. Experimental results

The circuit was simulated using the Matlab 7 tool. The simulated characteristic of the nonlinear voltage divider is presented in the figure 6a. The simulated characteristic of the recovered signal is presented in the figure 6b. At the input of the recovery circuit presented in the figure 5 is applied the signal from the output of the compression circuit. The signal on the recovery circuit output is similar with the signal on the input of the nonlinear voltage divider circuit as can be observed in the Figure 6b.
The characteristics of the signals acquired on the three channels of the acquisition board are presented in the Table 1. In this project a 16 bit 32 channels acquisition board made by National Instruments, model NI PCI 6254M is intended to be used. Because of the very high frequency spectral components of the disturbances, especially for disturbances with very high amplitudes, a 1MSPS sampling frequency is required. To prevent any unwanted disturbance which can appear on the way from the voltage dividers to the Analog-to-Digital Converter (ADC), the differential mod must be used on the acquisition board.

Table 1

Voltage range	0 – 0.5 kV	0 – 2 kV	0 – 10 kV
Voltage resolution	7.63 mV	30.5 mV	152.6 mV
Quantization levels for 7.63mV voltage resolution	65536	262123	1310616
the number of bits needed	16 bits	18 bits	21 bits

The number of quantization levels N_q for each voltage range is calculated with the following formula:

$$N_q = \frac{Voltage\ \ range}{Voltage\quad resolution} \tag{1}$$

where voltage resolution is defined by:

$$q = \frac{Voltage\ \ range}{2^n - 1} \tag{2}$$

n being the ADC number of bits. The number of bits n, for a given quantization levels N_q can be calculated with the formula:

$$n = int[log_2(Ql) + 0.5] \tag{3}$$

The smaller voltage resolution (7.63 mV) is obtained in the range of 0 – 0.5 kV. The maximum voltage resolution (152.6 mV) is obtained on the voltage range of 0 - 10kV (see table 1). By using a single voltage divider in the range of 0 – 10kV, and a 16 bit acquisition board, the signals with the amplitude lower than 0.5kV will use only 3276 quantization levels. At a voltage resolution of 152.6 mV, this is equivalent to the use of a 12 bits ADC.

$$N_q = \frac{0.5\,kV}{152.6\,mV} = 3276 \tag{4}$$

$$n = int[log_2(3276) + 0.5] = 12 \tag{5}$$

To implement a voltage divider with a single division ratio covering the voltage range from 0 to 10 kV with a voltage resolution of 7.63 mV, a 21 bit A/D converter is needed (Formula 7). In practice, instead of a 21bits ADC, a 22 bits ADC must be used, because the ADC's can only have an even number of bits.

$$N_q = \frac{10\,kV}{7.63\,mV} = 1310616 \tag{6}$$

$$n = int[log_2(1310616) + 0.5] = 21 \tag{7}$$

Using only a part of the acquired signal in the range of 0.5 kV – 2 kV and 2 kV – 10 kV, the effective bit resolution for the second and third voltage divider is decreased by one bit (Table 2). This is not a problem, in this voltage ranges the 15 bit being enough.

Table 2

Voltage range	0 – 0.5 kV	0.5 – 2 kV	2 – 10 kV
Voltage resolution	7.63 mV	30.5 mV	152.6 mV
Quantization levels used in the voltage range	65536	49180	52428
The number of bits used	16 bits	15 bits	15 bits

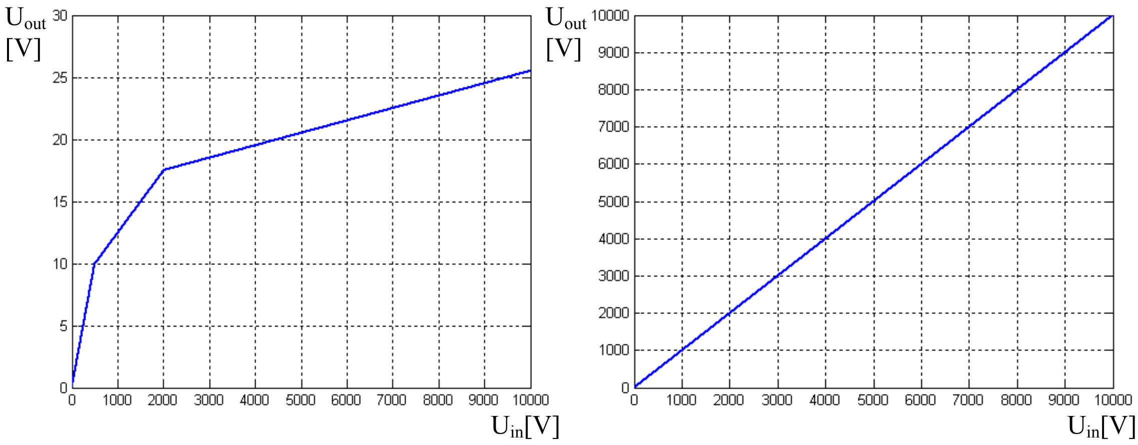

Fig. 6.
a) The transfer function of the nonlinear voltage divider circuit simulated in Matlab
b) The transfer function of the recovery circuit simulated in Matlab

IV. Conclusions

The nonlinear voltage divider transfer function presented in this paper is similar to the transfer function of a nonlinear voltage divider circuit presented in [1], [3] and [4], realized with operational amplifiers and diodes. The circuits realized with diodes have the disadvantage of rounded transfer function breakpoints and a high terminal instability. The circuit proposed eliminate this inconvenient.

This voltage divider can be successfully used as preconditioning circuit in an electrical power disturbances monitoring system. In these systems the main concern is to detect the small disturbances around the nominal voltage of the electrical power network (230V). The resolution for the signals with higher amplitudes is not so critical. It is important to detect the presence of the high amplitude disturbances and to preserve their shape, measuring their amplitude with high accuracy is not very important. Depending on the disturbances detection software algorithm, the nonlinear voltage divider output signal or the recovered signal can be used.

Compared to the methods who analyze all the three channels of the ADC [2], this method has the advantage to reduce the number of calculus made by the software application.

A 1MSPS 22 bit ADC is very expensive, compared with 3 1MSPS 16bits ADCs.

The division ratio of each of the three voltage dividers must be measured and preprogramed in the software application.

This nonlinear voltage divider can be hardware implemented using three simple frequency compensated resistive voltage dividers.

References

[1] C. Dughir, G. Găşpăresc, "Preconditioning Circuit for Electrical Power System Disturbances Measurement", Buletinul Stiintific al Universitatii "Politehnica" din Timisoara, septembrie 2006, Timisoara, Tom 51(65), Fascicola 1, 2006, ISSN 1583-3380, p. 164-170

[2] C. Dughir, G. Găşpăresc, "Three Channels Analysis System for Electrical Power System Disturbances Measurement", Buletinul Institutului Politehnic Iaşi, Tomul LII (LVI), Fasc. 5b, pag. 1007, Iasi, 2006

[3] Ciugudean, Mircea, *Circuite integrate liniare-Aplicații*, Editura Facla, Timişoara, 1986.

[4] Georges Asch et collaborateurs, *Les capteurs en instrumentation industrielle*, Imprimeie Gauthier-Villards, France, septembre 1991.

[5] Ciprian Dughir, "Detecting symmetrical disturbances in electrical power systems", Doctor Etc 2005, Timişoara, 22 September 2005.