Time and Frequency Domain Tests for ΣΔ Modulators

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Abstract –The paper deals with the classification method of some architectures of ΣΔ modulators. The classification is based on the analysis of the different trends of the output signals characterizing some ΣΔ modulator architectures. The method operates (i) by feeding the ΣΔ modulator with sinusoidal signal, and (ii) by analysing the output signals in the time or in the frequency domain. The classification consists in (i) distinguishing between low pass and band pass ΣΔ modulator, (ii) identifying both the Single Quantizer Loop (SQL) and the Multistage Noise Shapers (MASH) architecture, (iii) evaluating the levels of the quantizer block inside the SQL architecture, and (iv) detecting the number of cascaded stage inside the MASH architecture. In order to validate the proposed method, numerical tests are performed by referring to the noumerous architectures of ΣΔ modulators proposed in the relevant literature.

I. Introduction

The key factors assuring the large employment of the Sigma-Delta Analogue to Digital Converter (ΣΔ ADC) are: (i) the architectural enhancements of the ΣΔ modulator [1], and (ii) the programmability of the digital decimation filter to support various telecommunication standards for multimode radio receivers [2], [3]. Remarkable interest is devoted in literature [4] to the architecture of the ΣΔ modulators because they establish the fundamental characteristics of the ADC. The ΣΔ modulator is a non-linear system and it includes: (i) analogue input filter, (ii) quantizer block, and (iii) Digital to Analogue Converter (DAC) [4]. The characteristics and the connections of these blocks determine the different architectures of the ΣΔ modulators.
Two different ΣΔ modulator architectures can be defined: (i) Low-Pass (LP) and Band-Pass (BP) [5]. The quantizer block can work with one level or several levels and it is the cause of the quantizer error that is shaped by the modulator's noise transfer function. The noise shaping is achieved by creating a feedback loop around the cascade of the analogue input filter and the quantizer block. The number of quantizer levels establish the bit number of the DAC [6]. Therefore, different architectures can be defined on the basis of the quantizer levels. Moreover, the number of the cascaded feedback loops determines the architecture order [7]. Usually, only one quantizer is included in all the previous considered architectures. These architectures are denoted as Single Quantizer Loop (SQL) [8]. In order to overcome the stability problems affecting the high order SQL architectures, the Multistage Noise Shapers (MASH) architectures are taken into account [9]. The MASH architecture consists of the cascade of a number of stages each one constituted by a SQL and feed by the quantizer error of the previous one.
The output signals of the previous considered architectures are characterized by quite different trend according to their different behavior. These different trends can be advantageous utilized to infer from the output signal the fundamental and useful parameters characterizing the architectures of the ΣΔ modulators. These parameters permit (i) to detect and to monitoring the operating conditions, (ii) to assess the correctness of the operating conditions, (iii) to detect the causes of miss functioning, and (iv) to classify the different architectures of the ΣΔ modulators.
The paper deals with the classification method of the architectures of the ΣΔ modulators by analyzing the trend of the output signals. The classification permits (i) to recovery the information for the reconstruction of the behavioral model of the modulator architecture, (ii) to overcome the problems arising from the non reliable a priori knowledge of the modulator architecture, and (iii) to define homogenous classes grouping the ΣΔ modulator architectures that can be used for addressing the design and the testing recommendations.
The classification method pointed out is organized with a hierarchical structure: the result of every test selects and configures the parameters of the successive test. The method operates as follows: (i) the ΣΔ modulator is feed by sine wave at a quarter of the sampling frequency, (ii) the output signal is acquired and analyzed in both the time and frequency domain. In the frequency domain the classification method operates (i) to distinguish between LP and BP ΣΔ modulator, and (ii) to identify both the SQL and the MASH architectures. In the time domains it operates (i) to evaluate the levels of the quantizer block inside the SQL architecture, and (ii) to detect the number of cascaded stages inside the MASH architecture. In order to validate the proposed method numerical tests are performed by referring to the numerous architectures of ΣΔ modulators proposed in the relevant literature.

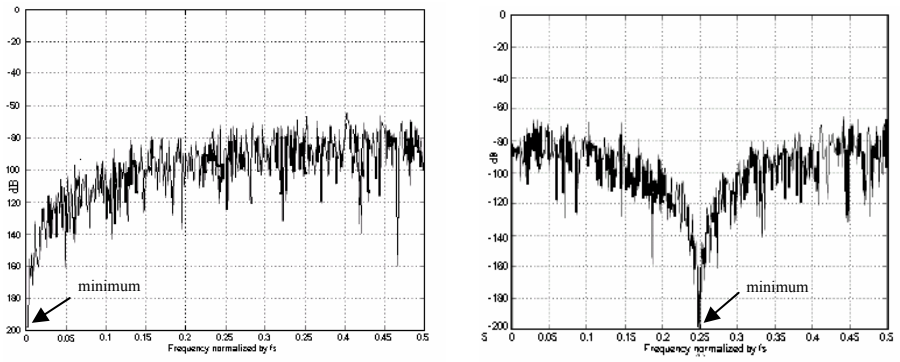


Fig.1 PSD shape of LP (left) and BP (right) ΣΔ modulator.

II. The classification method

The classification method is composed by a series of specific tests organized by means of the hierarchical structure. These tests are pointed out on the basis of the behavioral characteristics of the ΣΔ modulators available in the relevant literature. In the following the tests are discussed on the basis of the execution order.

A. LP / BP test

The first test detects if the modulator is LP or BP. To determine this propriety, the input sine wave at the frequency equal to a quarter of the sampling frequency is used. This particular frequency can be accepted from both the modulator type. In particular, the output signal of the modulator under test is analyzed in the frequency domain. The minimum of the fitting curve of the Power Spectral Density (PSD) permits to classify between the LP and BP architectures. For the LP modulator this minimum is located at the beginning of the PSD as shown in Fig.1 (left). For the BP modulator the minimum value is located at the quarter of the sampling frequency, as shown in Fig.1 (right).

B. SQL / MASH test

The classification among the SQL and the MASH architectures is performed on the basis of the slope of the decreasing zone characterizing the noise shaping, reported in Fig.2.

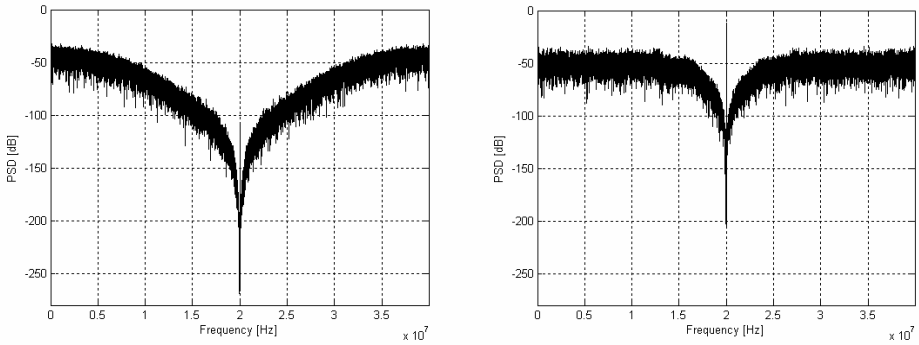


Fig.2 Normalized PSD of MASH (left) and SQL (right) BP architecture.

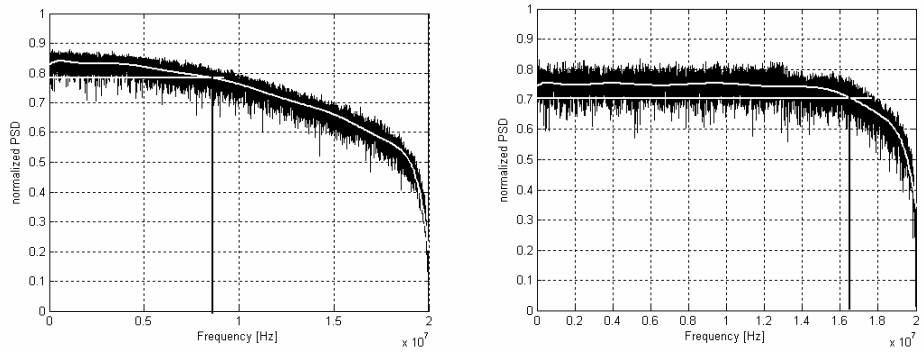
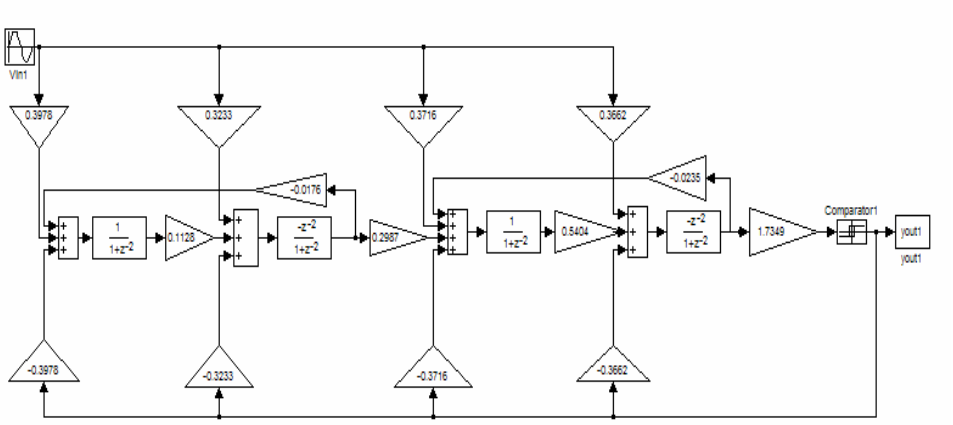
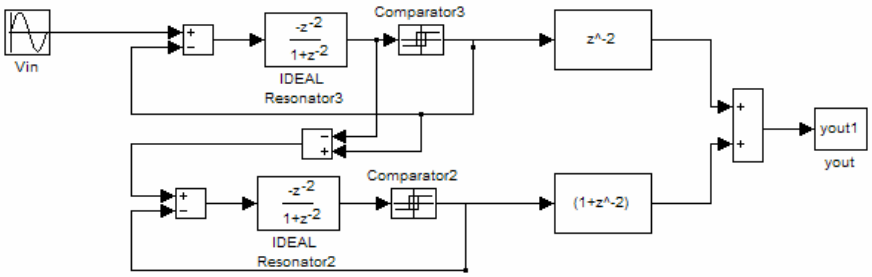


Fig.3 Evaluation of f_k for MASH (left) and SQL (right) BP architecture.



a)



b)

Fig.4 Architecture of a) SQL BP and b) MASH BP.

The test is based on the analysis of the normalized PSD of the output signal. The basic steps constituting the test are: (i) the PSD is evaluated and only the frequency range between [0, fs/4] is considered, (ii) from the resulting points of the PSD the tenth order polynomial fitting curve is estimated, (iii) the frequency f_k, defined as that corresponding to the reduction of 0.05 of the maximum value of the fitting curve of the noise shape, is detected, and (iv) the parameter ζ is defined as:

$$\zeta = \frac{f_k}{f_w} \tag{1}$$

where: f_k is the knee frequency evaluated on the normalized PSD as shown in Fig.3, and f_w is the center band frequency of the modulator. The classification among the SQL and the MASH architectures depend on the value of the parameter ζ. In order to determine the threshold value, numerical tests was performed by using numerous architectures. As a result, $\zeta<0.65$ identifies MASH architecture, $\zeta>0.65$ identifies SQL architecture. Fig.4 shows some example of SQL BP and the MASH BP architectures that can be distinguished on the basis of the proposed classification test.

C. Number of level / stage test

Once the architecture type is determined, it is necessary to evaluate the number of the levels for the SQL modulator and for the MASH modulator. This analysis is developed in the time domain. In particular, the analysis of the output signal permits to evaluate (i) the level number of the quantizer for the SQL architecture, as shown in Fig.5, and (ii) the level number related to the cascaded stages for the MASH architecture, as shown in Fig.6. Indeed, the characteristic levels pointed out in the output signal have correspondence to (i) the levels of

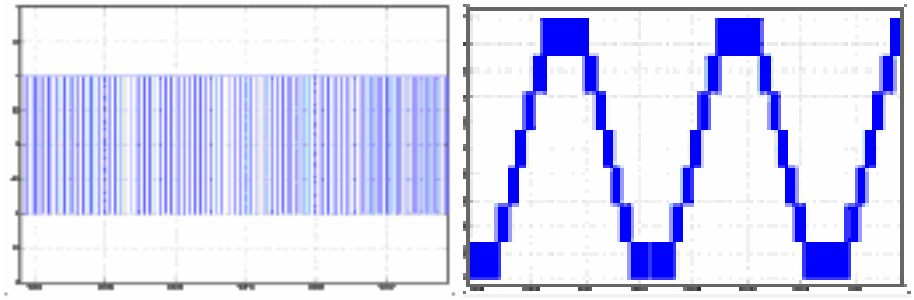


Fig.5 SQL output with one bit (left) and 3 bit (right) quantizer.

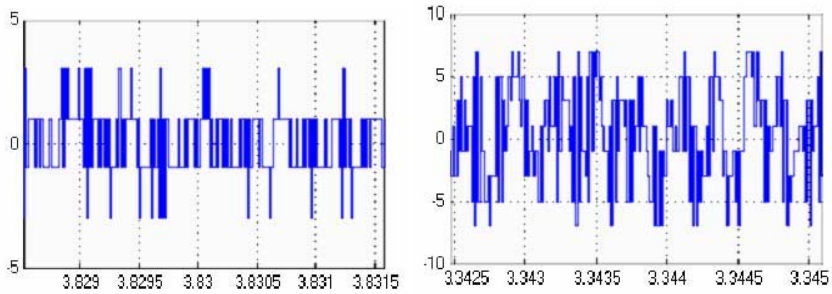


Fig.6 MASH output with 2 stages (left) and 3 stages (right).

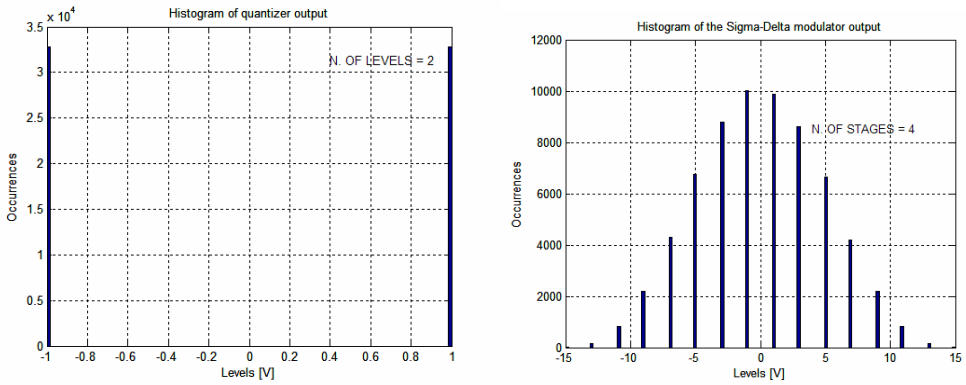


Fig.7 Histogram test corresponding to two levels SQL (left), and 4 stages MASH (right).

the quantizer, for SQL architecture, and (ii) the number of cascaded stages, for MASH architecture.
Moreover, denoted by n_l the number of the levels detected on the output signal, the quantizer bit number for SQL architecture is:

$$n_x=\log_2 n_l \quad . \tag{2}$$

In the case of the MASH architecture, the stage number is:

$$n_s=\log_2 n_l \quad . \tag{3}$$

The evaluation of n_l is performed by means of the occurrence histogram of the levels detected on the output signal, as shown in Fig.7.

D. SNR trend analysis

To detect the ΣΔ modulator architecture, another test can be followed. This test utilizes the Signal to Noise Ratio (SNR) evaluation with different amplitudes of the input sine wave. The distinction between the SQL and MASH architecture is obtained by the analysis of the resulting SNR trend. In particular, Fig. 8 shows the trend of the estimated SNR versus the amplitude of the input sine wave. For

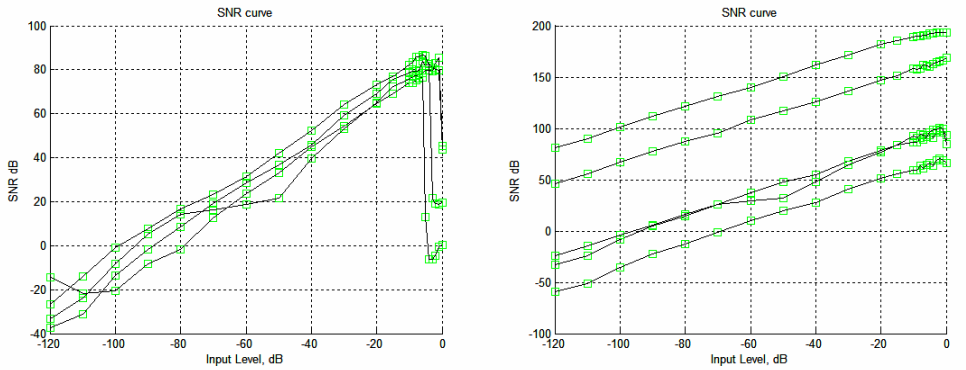


Fig. 8 SNR trend versus the amplitude of the input sine wave for SQL ΣΔ architectures (left), and MASH ΣΔ architectures (right).

the SQL modulator there is a substantial decreasing of the curve for the values of the input signal amplitude near the full scale of the modulator. This behaviour is absent in the case of the MASH modulator. Consequently, it is necessary (i) to know the full scale of the modulator, and (ii) to determine the SNR curve versus the input signal amplitude. If non monotonic trend is shown the modulator is SQL type, else it is a MASH modulator.

Conclusions

A classification method for different architectures of ΣΔ modulators has been presented. The classification consists in (i) distinguishing between low pass and band pass ΣΔ modulator, (ii) identifying both the Single Quantizer Loop (SQL) and the Multistage Noise Shapers (MASH) architecture, (iii) evaluating the levels of the quantizer block inside the SQL architecture, and (iv) detecting the number of cascade stage inside the MASH architecture.
The classification method operates by analysing the output signal in both the time and frequency domain. It is the first step towards a complete test procedure (i) to assess the correct functioning of the ΣΔ modulators, and (ii) to detect the causes of miss functioning.

References

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