Measuring And Interpreting the CMOS IC Variable Input Impedance Versus ESD Stress

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Abstract- The paper presents a comparative method (and the related results) for measuring the various impedances of a Si-gate CMOS digital circuit, very useful for the study of the dual input protection configuration, with respect to an ESD pulse. The results of the performed measurements are interpreted according to the behaviour of the two main protective circuits and are useful to verify the waveform at the output of a self-manufactured ESD tester, the load values being essential.

1. Introduction

The integration density in modern circuitry and the connected power efficiency are gradually improving. This permanently existing trend towards microelectronics was accompanied by higher susceptibility to radiated or conducted fields and fast transients. Consequently, the up-to-the-minute test methodologies came down at the component (ICs) level, allowing a more precise location of the "trouble" than testing the subassembly or the equipment. Within this area, the ESD is to be blamed for most of the failures in electronics. A covering test must be truthful and with guaranteed reiteration. A test must be close to reality (compulsory for the foresight of the reliability of the IC in an usual device) and repeatable, for consistently finding the problems and evaluating the accomplishment of the achieved solutions.

2. Starting point

While testing the real applicability of a modified version of the Human Body Model for ESD events versus some 4HCxx-series (Si-gate CMOS integrated logical circuits, pin compatible with Low power Schottky TTL), we measured variable input impedance during the occurrence of the ESD event, more precisely, during the incidence of the discharge current.

In essence, with HBM is modelled the discharge from the fingertip of a standing person delivered to the device, by a 100 pF capacitor discharged through a switching component and a 1,5kΩ series resistor into the component [1].

We consider that an important advantage of this model is its capability of accepting automated tests. Integrated circuits being involved, we chose the option with the IC firmly inserted in its socket, the so-called Socketed Discharge Option for HBM. Assuming this model and in accordance to EIA/JESD22-A114-A, the ESD protection of the above mention series exceeds 2000V.

For measuring the IC impedances, we used a comparative methodology developed in [2], with the test set-up presented in figure 1. The IC was successively replaced by three precision (high voltage) resistors, having 100, 200 and respective 400 Ω.

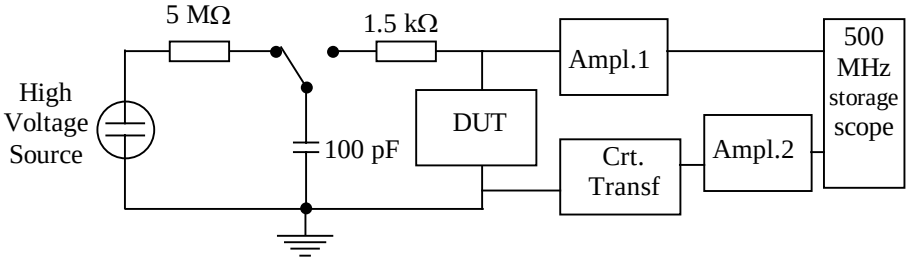

Figure 1**.** The test set-up for measuring the IC input impedance

The IC is inserted in the test system and contacted through a relay matrix. ESD stress is gradually applied and the post stress I-V current traces are examined to see if the devices fail. According to ESD Association recommendations, we reduced the number of zaps per stress level and polarity from 3 to 1

and also the minimum time interval between zaps has been reduced from 1 second to 300 milliseconds. Also, the maximum rise time for a HBM waveform measured through a 500Ω load was increased from 20 to 25 nanoseconds [2].

The voltage-drop across the DUT was registered on the scope (floating measurement). The store writing speed is of 2500cm/μs, enabling storage of single-shot rise–time to 1,3ns (bandwidth DC to 500MHz). The voltage amplifier (Ampl.1) is a two-channel, 1 MΩ input also having bandwidth 500 MHz, while the current amplifier (Ampl.2) is a single channel one, 50Ω input. The associated current waveforms were represented on the scope by using a calibrated current transformer. By comparing the peak currents through the device to the peak currents through the resistors, was possible to determine the effective impedance levels of the devices. This relative technique for impedance measuring has the advantage of annulling the influence of common modes or stray, parasitic coupling capacitance.

The essential result was that, according to the level of the applied ESD pulse, the values for the measured impedance were different.

3. Behaviour of IC's Protection Structure to ESD menace

While testing the CMOS gate entrance with progressive growing voltages [3], we measured the following impedances of four degrees of magnitude:

1. Input voltage < 15 V, Z_{input} = MΩ (protection not yet activated).
2. 15V< Input voltage<200 V, Z_{input} = 500-800Ω (clamping diode, figure 2, acting like a voltage limiter is quickly activated).

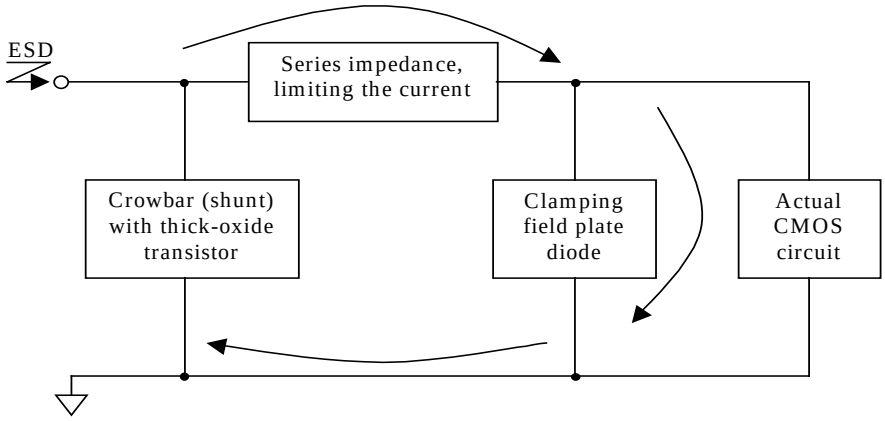

Figure 2 ESD protection structure, explaining variable input impedances

3. ESD pulse about 1KV, Z_{input} = 130-180Ω,the thick-oxide transistor is partially activated, shunting the majority of the entrance current.
4. ESD pulse greater than 1KV, lasting for many μs, Z_{input} = 10-15Ω, crowbar fully activated.

The protective structure must reduce not only the voltage, but also the peak power in the digital circuit. The peak power threat depends on the peak current and its square. Considering the time delay for the opening of the protective structure, the rise-time of the current has its significance for the peak power. Considering the energy accumulated in the protective device, the peak current is not determinant, but the entire current over time. So, we can appreciate that the energy threat is linked with the whole ESD current waveform and its square value, not only with its peak current.

4. Penetration of the ESD-induced electromagnetic fields

An accidental loop could be formed between the output of the here studied digital circuit and the input of the following one, [4]. The discharge current, established through the protective element has the role of the emitting monopole antenna. The magnetic field is to be blame for the differential-mode perturbation, while the electric component is responsible for the common-mode voltage, mainly upsetting the ungrounded elements. A part of the ground structure has its own characteristic impedance, determined by the width, length or diameter. Also significant are any discontinuities, in mechanical junctures, involving reflections with influences on the current waveshape. A penetration loop could be established between the traces of the printed circuit board, or between the connection wires. The

passage of the discharge current through the protective path generates a time-varying electromagnetic field, inducing a differential-mode voltage in series with the loop, while the common-mode voltage is referred to the general ground. By superposing the differential and the common mode induced voltages we have a total voltage at the receiving gate that must be lower than noise margin of the "attacked" gate, not to produce any upset.

The highest induced voltage is associated with the first peak of the discharge current. For facilitating the worst-case induction evaluation, it is advisable to "finish" the discharging path in its characteristic impedance. Such a potential accidental loop is presented in figure 3.

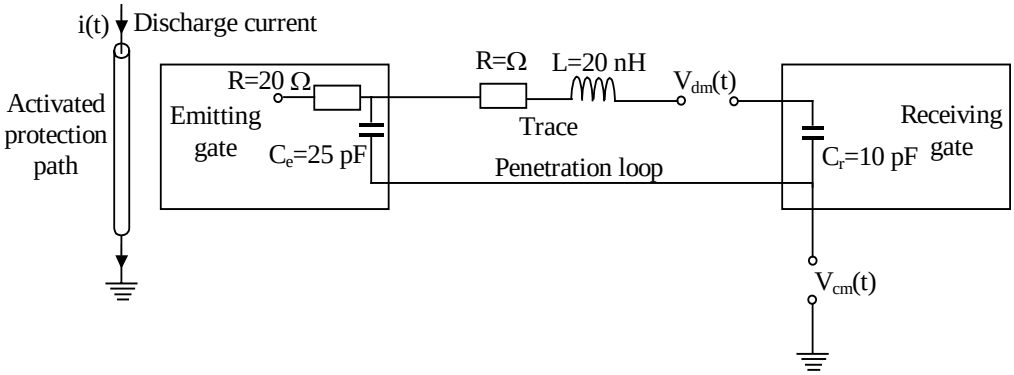

Figure 3. Accidental receiving loop antenna involving digital circuits

The trace inductance was evaluated at about 20 nH, while its resistance is around 1Ω. The chosen values in figure 3, for modelling the "emitting" gate and the 'disturbed" gate are a reasonable approximation for the selected digital family. While the arcing from the discharge path to circuitry is almost always destructive and the surface charging of ungrounded circuit elements could also be damaging, the induction of differential mode voltage in circuit loop has quite dissimilar behaviour. The resulting "hang-up" could be solved by a simple switch off/on of the system power.

5. Conclusions

Just simple extrapolation of any already certified data in the "existent word" could offer sometimes-wrong conclusion, ESD complexity being "harder" than any model or previous attempt. When designing and verifying an ESD tester, the load impedance is fundamental to assure the realism and the repeatability of the experiment, through a waveform quasi-similar with the genuine encountered one. The here measured input impedance of a dual protected Si-gate CMOS quad 2-input NAND circuit has values spread from 30Ω till 800Ω (during the three different phases when ESD threat is maximum). It is advisable to the output currents of the simulator into minimum two representative loads.

Acknowledgements

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