Voltage to Frequency Converter and Fractional Frequency Divider Based on Modified Sigma-Delta Converter

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Abstract **-** Voltage to frequency converter (VFC) is an oscillator whose frequency is linearly proportional to control voltage [1-11]. In this paper, the New Synchronous Voltage to Frequency Converter (NSVFC) or "sigma delta" (Σ-Δ) voltage to frequency converter is described. This NSVFC works similarly as conventional synchronous voltage to frequency converter (SVFC) [12], but it has a better frequency spectral property then other SVFC and therefore it is possible to used as fractional frequency divider and also building block in fractional phase locked loop (PLL). An experimental NSVFC was constructed and simulated to verify operation of the converter [13]. Analysis and prototype of NSVFC is described.

I. Converter description

In Figure 1 the NSVFC block diagram is shown. Only one-shot is added and connected to comparator output in compare to common Σ-Δ converter. Figure 2 shows waveforms of this NSVFC. Number of pulses is same as for usual Σ-Δ SVFC [2] and NSVFC [13]. The output frequency f_O is given by (1):

$$f_O = f_{CLK} (1 - V_i / V_R) / 2 \qquad \text{[Hz, V]} \qquad (1)$$

where V_i is input voltage, V_R is reference voltage and f_{CLK} is clock frequency. It is important to note, that for NSVFC this equation is limited for V_{imin} given by (2). The minimal input voltage value V_{imin} for NSVFC:

$$V_{imin} > 2 f_{CLK} V_R t_{dC} \qquad \text{[V, Hz, sec]} \qquad (2)$$

where t_{dC} is comparator time delay. E.g. for $f_{CLK} = 10$ *kHz,* $V_R = 5$ *V* and $t_{dC} = 200$ *ns,* the minimal value $V_{imin} > 0.02$ *V*. This disadvantage was in final design removed by additional logic.

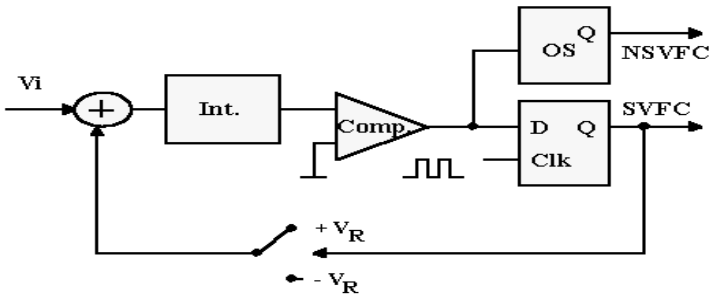


Figure 1. NSVFC - New Σ-Δ voltage to frequency converter. Int. - integrator, Comp. - comparator, V_i - input voltage, V_R - reference voltage, D - flip flop, OS - one shot.

II. NSVFC output frequency evaluation

The key to Σ-Δ modulator is the integrator. At each conversion, the integrator keeps a running total of its previous output and its current input. The output from the integrator is feed to 1-bit analog/digital converter (ADC). This is simply a comparator with its reference input at a level of half the input range, 0 V in this case. The ADC output feeds a 1-bit digital/analog converter (DAC) which has output levels equal $+V_R$ or $-V_R$. A summing amplifier completes the loop by summing the current input signal and the previous sample DAC output. The aim of the feedback loop is to try to maintain the average output change of the integrator at the comparator reference level, 0 V. From this, the output frequency f_O can be derived and is given by (1), [14].

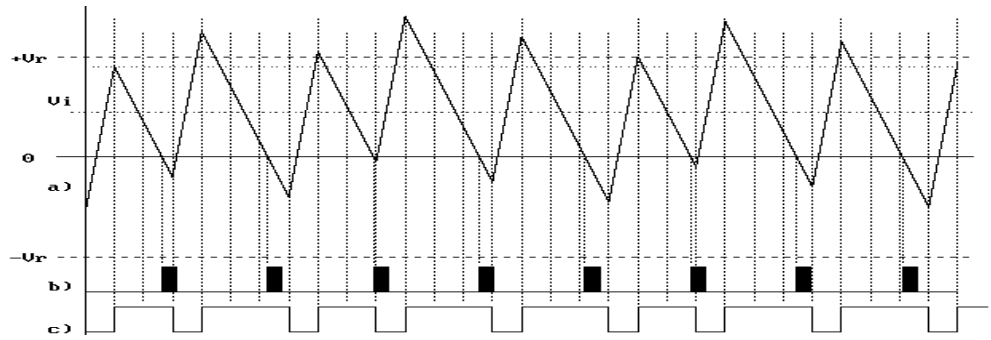


Figure 2. Waveforms of SVFC (a, c) and NSVFC (a, b, c). a) integrator - output voltage, b) one shot output, c) D-flip flop output. $V_i = 1.8$ V, $V_R = 4$ V, period of one shot is $3.636\ T_{clk}$

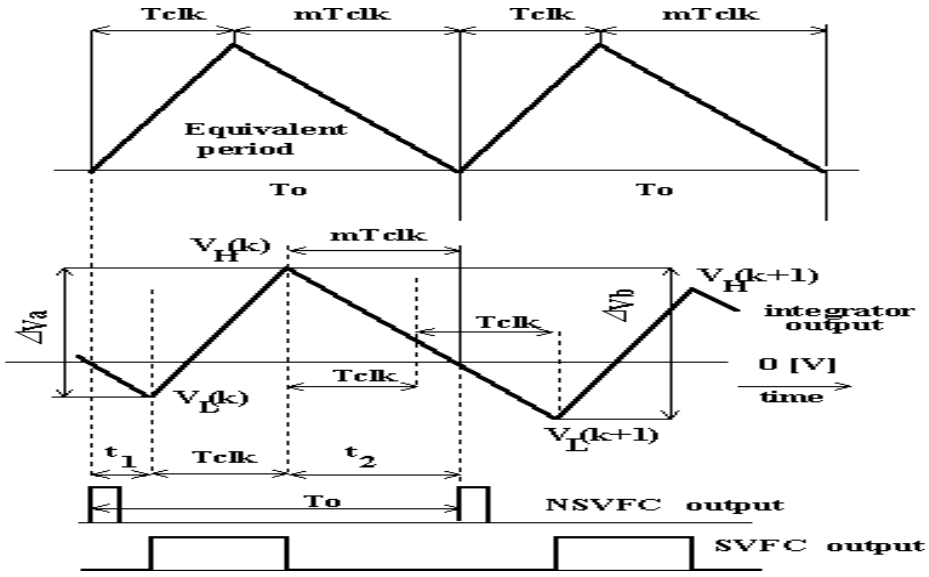


Figure 3. NSVFC waveforms and equivalent period time diagram (top) and detailed waveforms of the integrator, D flip-flop SVFC and one shot NSVFC outputs, $n=2$ in this figure $(nT_{clk}= 2T_{clk})$.

A. Output frequency evaluation for ideal NSVFC

For this ideal NSVFC it is supposed, that comparator has a zero time delay and noise value voltage on second comparator input is zero. Output period for NSVFC can be determined from Figure 3.

It is supposed, that $V_R > V_i$, where V_R is reference voltage and V_i is input voltage. The $V_L(i)$ and $V_H(i)$ are voltage at integrator output.

The negative slope is $C(V_R - V_i)$ while positive slope is $C(V_R + V_i)$ where C is the integrator time constant. Moreover

$$t_1 = \frac{-V_L(k)}{C(V_R - V_i)} \tag{3}$$

and

$$t_2 = \frac{V_H(k)}{C(V_R - V_i)} \tag{4}$$

Also $V_H(k)-V_L(k)=C(V_R + V_i)T_{clk}$. The period is $T_0 = t_1 + t_{clk} + t_2$, as a result

$$T_o = \frac{-V_L(k)}{C(V_R - V_i)} + T_{clk} + \frac{V_H(k)}{C(V_R - V_i)} = \frac{V_R + V_i}{V_R - V_i} + T_{clk} = 2T_{clk}\frac{V_R}{V_R - V_i} \tag{5}$$

The from (5) the output frequency f_0 is:

$$f_0 = f_{clk}(V_R - V_i)/2V_R \tag{6}$$

where $f_{clk} = 1/T_{clk}$

From (6) is shown, that ideal NSVFC output frequency is linearly dependent on input voltage (f_{clk} and V_R are constants) [15].

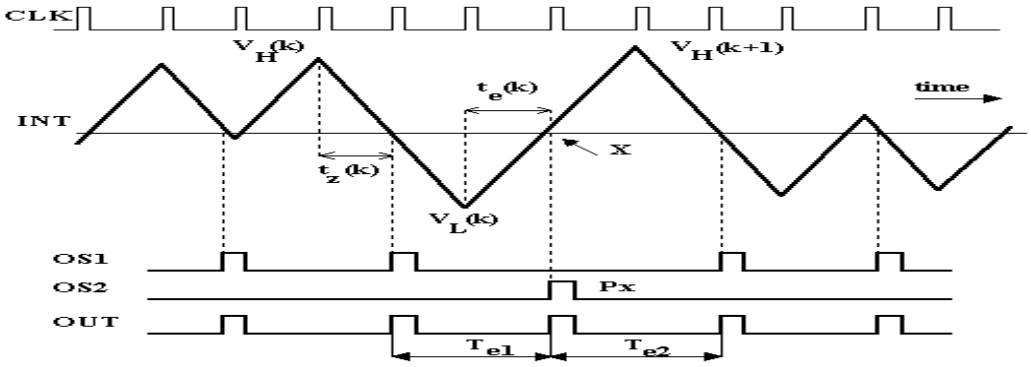


Figure 4. Time diagram for real converter - output frequency evaluation

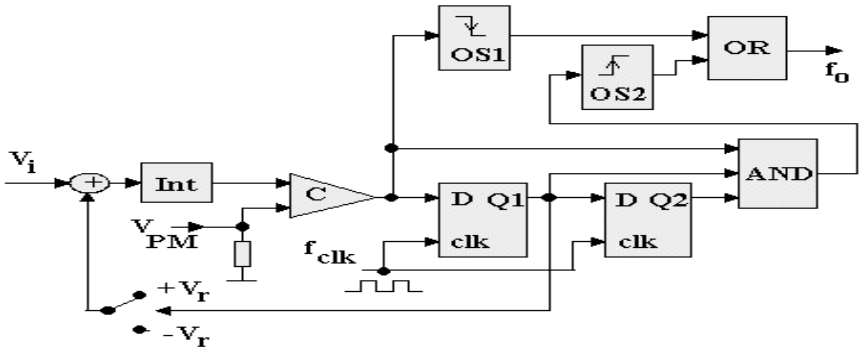


Figure 5. NSVFC2 - Block diagram. Int. - integrator, Comp. - comparator, V_i - input voltage, V_R - reference voltage, V_{PM} - input voltage for phase modulation, D - flip flop, OS - one shot, AND, OR - log. function.

B. Output frequency evaluation for real NSVFC

In this part, error caused by comparator delay, comparator hysteresis or voltage change on second comparator input is described. This error is displayed on Figure 4 and is sign by X point. The error can arise especially when input voltage $V_i \approx 0$. The error occur when 2 clock cycles are need for $V_L(k)$ to $V_H(k+1)$ transition [16]. In this case, this must be detected and output pulse is generated, when integrator output voltage on one comparator input is greater than voltage on second comparator input (it is important to note, that in ideal condition, output pulse is generated only when voltage on integrator output is lower then voltage on second comparator input - leading edge of integrator output). The additional logic is used for this purpose. The block diagram of this NSVFC2 is shown in Figure 5.

Output period T_0 from Figure 4 is given by:

$$T_{e1} = T_{clk}\,[n(k) - t_z(k) + t_e(k)] \tag{7}$$

For $T_{clk} = 1$, $V_i << V_R$ output period ${}^1T_{e1}$ is given by:

$${}^1T_{e1} = ceil(V_H(k)/(V_R - V_i)) - V_H(k)/(V_R - V_i) + |V_L(k)/(V_R + V_i)| \tag{8}$$

where Ceil(.) - Converts a numeric value to an integer by returning the smallest integer greater than or equal to its argument. E.g. Ceil(9/3)=3, Ceil(9.01/3) =4.

In (8) $ceil(V_H(k)/(V_R - V_i))=2$ and $V_H(k) \approx V_R$ and $|V_L(k)| \approx V_R$ for $V_i \approx 0$. Hence:

$${}^1T_{e1} = 2 - V_R/(V_R - V_i) + V_R/(V_R + V_i) \approx 2(1 - V_i/V_R) \tag{9}$$

Similarly the output period ${}^1T_{e2}$ is given by:

$${}^1T_{e2} = 2 - t_e(k) + V_R/(V_R - V_i) = 2 - V_R/(V_R + V_i) + V_R/(V_R + V_i) \approx 2(1 + V_i/V_R) \tag{10}$$

Equations (9) and (10) for T_{clk} are simplified to:

$$T_{e1} \approx 2T_{clk}\,(1 - V_i/V_R) \tag{11}$$

and T_{e2} is given by:

$$T_{e2} \approx 2T_{clk}\,(1 + V_i/V_R) \tag{12}$$

III. Simulation results

Simulations were performed to validate the results of mathematics analysis. These results (Figure 2) were obtained programming of SVFC and NSVFC equations. The SVFC and NSVFC has also been simulated in system level by SIMULINK (MATLAB). Figure. 6 shows the frequency spectrum of the output waveforms. Figure 7 shows the waveforms with errors, which are corrected by additional logic used in NSVFC.

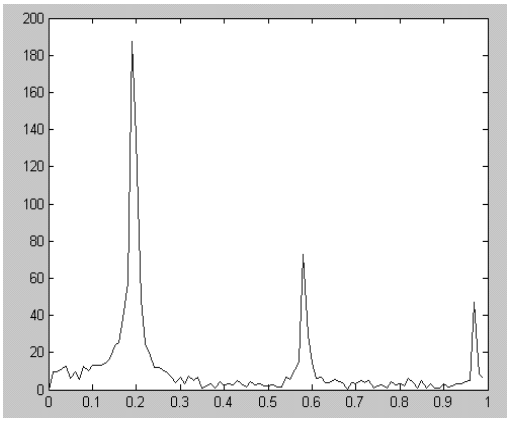


Figure 6. Frequency spectrum of NSVFC.

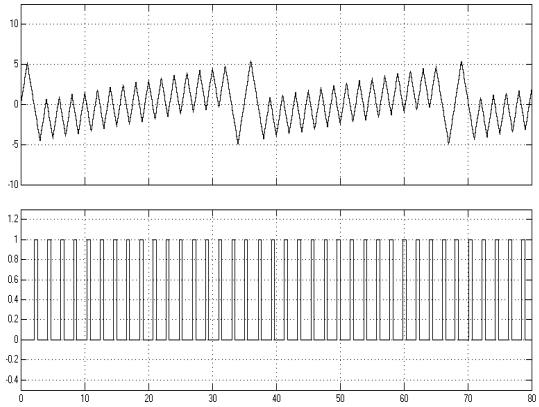
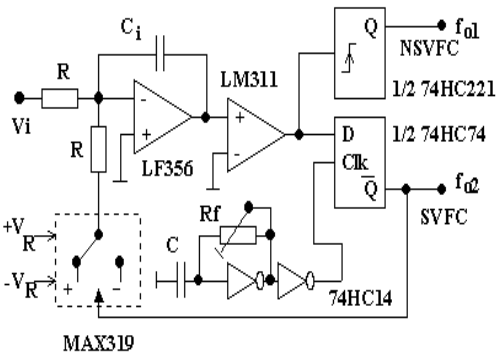


Figure 7. Simulated waveforms (with errors). Errors are corrected by additional logic.

IV. Experimental results

Commercially produced SVFC AD7741 and AD7742 [2] were tested and also NSVFC was realized and tested [14], [15], [16], [17]. In Figure 8, experimentally realized NSVFC simplified circuit diagram is shown. The voltage/frequency characteristic and frequency spectrum was measured. In Figure 9, graph of measured voltage/frequency characteristic of experimental NSVFC is shown.



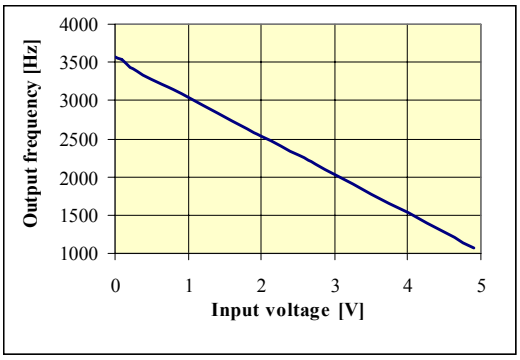


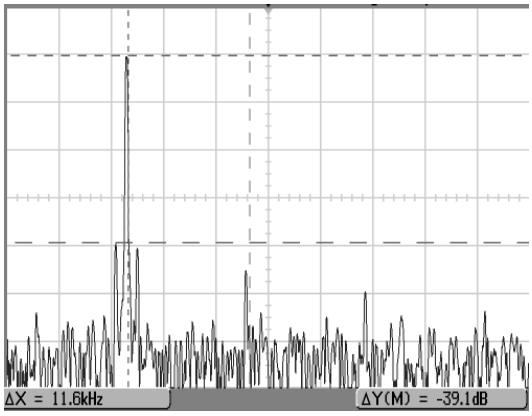
Figure 8. Experimental NSVFC simplified circuit diagram. Figure 9. Graph of voltage/frequency characteristic of realized experimental NSVFC.

In so far used type of SVFC, because the output pulses are synchronized to a clock, they are not equally spaced. This need not affect the user of a SVFC for A/D conversion, but it does prevent its use as a precision oscillator. Despite this disadvantage the improvement in performance makes the SVFC ideal for the majority of high-resolution VFC applications.

In Figure 10, the frequency spectrum of SVFC is shown and in Figure 11, the spectrum of NSVFC is displayed. From Figure 11 can be seen, that spurious spectral lines are rejected and therefore, NSVFC can be used as voltage controlled fractional divider in some applications. In practice, it is important to avoid saturation of integrator output, especially for fractional divider application, where input frequency is changed. Therefore, input frequency ($f_i \equiv f_{CLK}$) must be higher than:

$$f_i > 2V_R / R_i C_i V_{SAT} \quad (13)$$

where R_i, C_i are integrator resistor and capacitor and V_{SAT} is integrator saturation voltage.



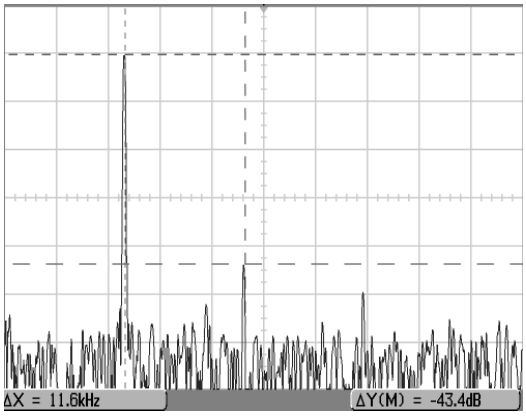


Figure 10. The frequency spectrum of traditional Σ-Δ V/f converter. Figure 11. The frequency spectrum of new, modified Σ-Δ V/f converter (NSVFC).

V. NSVFC application in fractional phase locked loop frequency synthesizer

The fractional frequency synthesizer is similar to the divide-by-N phase locked loop (PLL), however, with assistance of the NSVFC, the output frequency of the voltage-controlled oscillator (VCO) is not restricted integral multiples of the reference signal only. Therefore reference frequency can be higher than the step size and overall division can be reduced. The main motive for using fractional PLL architecture is to improve phase noise; however, increasing reference frequency makes it possible to improve switching speed as well by increasing loop bandwidth. With NSVFC, fractional frequency synthesizer can be simply realized [17].

The block diagram of experimental fractional PLL synthesizer is shown in Figure 12. If the VCO is locked to the reference frequency, then:

$$f_d = f_r \quad (14)$$

where is f_r reference frequency and f_d is frequency on the output of NSVFC. Because this frequency is given by (15):

$$f_d = f_o (1 - V_i / V_R)/2 \quad (15)$$

where f_o is frequency of VCO, therefore after substituting for f_d from (15) into equation (14), frequency of VCO is given by (16):

$$f_o = 2f_r \, 1/(1 - V_i / V_R) \quad (16)$$

The VCO frequency f_o can be changed according equation (16) by means of changing V_i.

The fractional frequency synthesizer using NSVFC was build. The frequency spectrum was the same as in Figure 11.

VI. Conclusions

A new type sigma-delta voltage to frequency converter circuit has been presented in this article. A prototype system was constructed to verify operation of the converter. Analysis, simulation and experimental sample of new type voltage to frequency converter were described. The NSVFC simulation results and measured results were compared. From analysis, simulation and measured results can be seen very good agreement from different point of view. It was pointed out that this new converter has better properties than other synchronous types of VFC. This main disadvantage of SVF described above was removed in new type of NSVFC. The applications NSVFC fractional phase locked loop frequency synthesizer was also presented. This type of voltage/frequency converter can be used for high output frequency (similarly as Direct Digital Synthesis), but it has pulse output and can be voltage or digitally (by means of D/A converter) controlled.

Because output pulses are equally spaced in NSVFC (some spurious spectral lines are rejected), this device can be used also as fractional divider.

ACKNOWLEDGMENT

This research work has been supported by New Technologies - Research Center in West Bohemian Region LN00 B084 and partly also by Spezial-Electronic (Maxim IC's).

References

[1] Sangil Park, Ph. D., *Principles of Sigma-Delta Modulation for Analog-to-Digital Converters*, Motorola Application Notes APR8, 1999.
[2] *Single and Multichannel, Synchronous Voltage-to-Frequency Converters*, *AD7741, AD7742*, Analog Devices 1999.
[3] *Analog Multiplexers/Switches*, Maxim 1995 New Releases Data Book, Vol. IV.
[4] Gilbert B., Grant D., *Applications of the AD537 IC Voltage-to-Frequency Converter, AN277*, Analog Devices.
[5] Jung W., *Operation and Applications of the AD654 IC Voltage-to-Frequency Converter, AN278*, Analog Devices.
[6] Gilbert B., Kitchin C., Weigel K., *Build Fast VCAs and VCFs with Analog Multipliers, Voltage-to-Frequency Converter, AN309*, Analog Devices.
[7] Martin S., *Using AD650 Voltage-to-Frequency Converter As a Frequency-to-Voltage Converter, AN279*, Analog Devices.
[8] Jung W., Riskin J., Counts L., *Circuits Ideas for IC Converters, AN343*, Analog Devices.
[9] Bryant J., *Ask the Applications Engineer-3, V/F Converters, AN361*, Analog Devices.
[10] Klonowski P., *Analog-to-Digital Conversion Using Voltage-to-Frequency Converters, AN276*, Analog Devices.
[11] Zuch L., *Voltage to Frequency Converters, Data Acquisition and Conversion Handbook*, Datel-Intersil, 1980, pp. 199 - 227.
[12] Stork M., "Modified Σ-Δ Voltage to Frequency Converter", *4-th International Conference on Advanced A/D and D/A Conversion Techniques and Their Applications. IMEKO TC-4*, Prague, June 2002, ISBN 80-01-02540-3, pp. 211 - 214.
[13] Stork M., "New Fractional Phase-Locked Loop Frequency Synthesizer Using a Sigma-Delta Modulator", *14th International Conference on Digital Signal Processing, DSP 2002*, Santorini - Greece, July 2002, ISBN 0-7803-7503-3, Volume 1, pp. 367 - 370.
[14] Stork M., "New Σ-Δ Voltage to Frequency Converter", *the 9th IEEE International Conference on Electronic Circuits and Systems, Proceedings*, Dubrovnik, Croatia, September 2002, ISBN 0-7803-7596-3, Vol. II, pp. 631 - 634.
[15] Stork M., "Voltage to Frequency Converter", *12th IMEKO TC4 International Symposium, Electrical Measurements and Instrumentation*, Zagreb, Croatia, September 2002, ISBN 953-96093-8-0, Proceedings Part 2, pp. 464 - 467.
[16] Stork M., Kaspar P., "Fractional Phase-Locked Loop Frequency Synthesizer", *Proceedings SCS 2003, International Symposium on Signal, Circuits and Systems*, Iasi, Romania, July 2003, ISBN 0-7803-7979-9, Volume 1 of 2, pp. 129-132
[17] Stork, M., "Voltage to frequency converter with phase modulation possibility", *In ELECO ´2003*. Istanbul : UMUT Matbaacilik, 2003. s. 131-135. ISBN 975-395-667-3.