# Capacitance Measuring System Based on Modified Sigma-Delta Converter

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***Abstract-*** The paper brings new information about capacitance measuring system based on modified sigma-delta converter (MSDC) with compensated loop based on phase locked loop (PLL). The consist of the 2 current sources and can be used for non-electrical quantity which will break the value symmetry in circuit, e.g. light intensity can be also measured with photodiode connected parallel to current source. Measuring system can work in open loop (direct sigma-delta converter) or closed loop (PLL). The system has the voltage and digital output and in closed loop can be supposed as a voltage controlled oscillator which is locked to input clock frequency. The simple flip-flop sensor for capacitance, or some other measuring is also described. In this paper, short information concerning of the system and experimental results are shown.

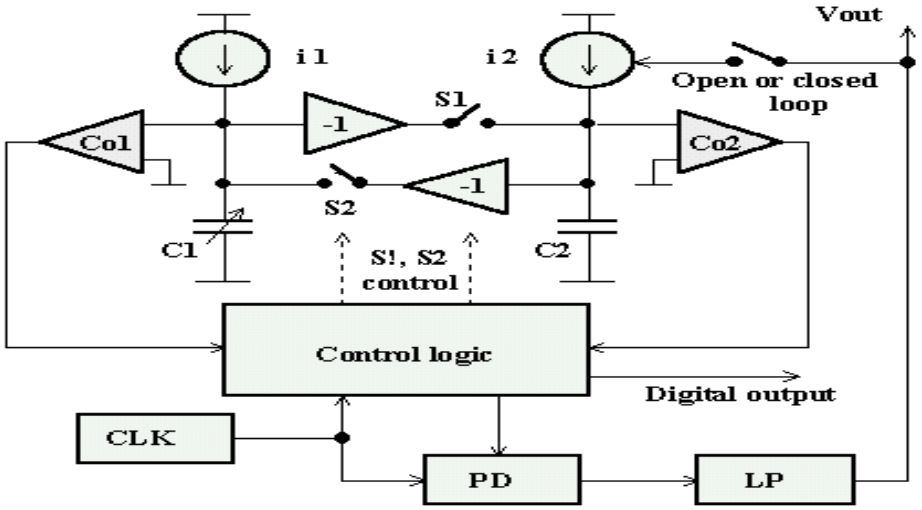


Figure 1. Block diagram of MSDC measuring system. *C1* - measured capacitance, *C2* - fixed capacitance, *Co1; Co2* - comparators, *CLK* - stable clock, *PD* - phase detector, *LP* - lowpass filter, *i1* - fixed current source, *i2* - voltage controlled current source, *S1; S2* - switches.

## I. System description

The block diagram of the Σ-Δ (sigma-delta) measuring system with compensating loop is shown in Figure 1. When the switch (closed/open loop) is open, the system work as conventional Σ-Δ converter [1, 2]. Voltage on $C_1$ is given (for $i_1 = constant$) by (1):

$$V_{C1}(k) = (1/C_1)\, i_1\, T_{CLK} + V_{C2}(k\text{-}1) \tag{1}$$

and voltage on $C_2$ is given by (2):

$$V_{C2}(k) = (1/C_2)\, i_2\, n\, T_{CLK} + V_{C1}(k\text{-}1) \tag{2}$$

where $T_{CLK}$ is clock period and $n$ is integer value. For $C_1 < C_2$ is given by (3):

$$n = ceil(C_1/C_2) \tag{3}$$

where *ceil(.)* converts a numeric value to an integer by returning the smallest integer greater than or equal to its argument. E.g. *ceil(9/3)=3*, but *ceil(9.01/3)=4.*

When the switch (closed/open loop) is closed, the system work as phase locked loop. In this case, the different values of $C_1$ and $C_2$ are compensated the changing of $i_2$. It is important to note, that for equally spaced output pulses (system used as oscillator), additional pulses are generated by control logic [3, 4, 5].

It is important to note, that instead of variable $C_1$, variable can be used $i_1$ , or constant $i_1$ and variable current source in parallel with $i_1$ e.g. photodiode for light intensity measurement.

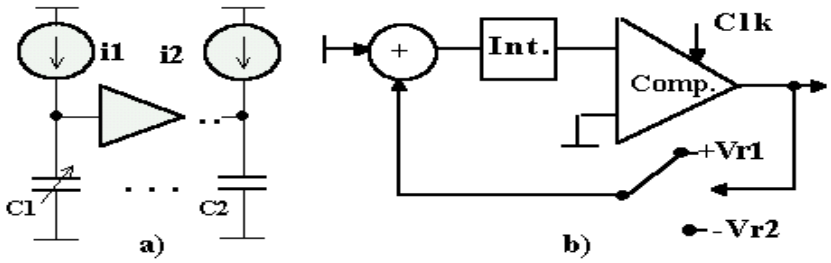


Figure 2. a) The MSDC simplified block diagram (only $C_1$ is affected) is equivalent to conventional Σ-Δ converter b) with zero input voltage and different reference values voltage sources $+V_{r1}$, $-V_{r2}$. Int - integrator, Comp - clocked comparator.

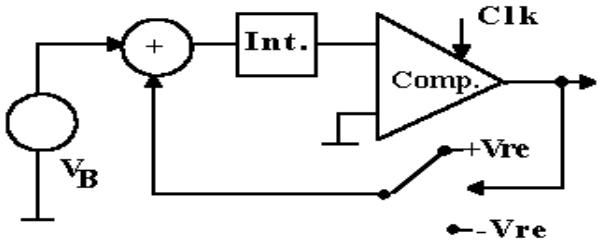


Figure 3. Σ-Δ converter with zero input voltage and different reference values of voltage sources (Figure 2 b)) is equivalent to Σ-Δ converter with the bias input voltage $V_B$ and $\pm V_{re}$ reference voltage.

### II. Modified sigma-delta converter output frequency determination

For evaluation of MSDC output frequency (in open loop), the equivalent circuit scheme was derived. It can be derived, that for MSDC with $C_1$ is changed, equivalent conventional Σ-Δ converter with zero input voltage and different reference values of voltage sources can be used (Figure 2 a) and b)) and this converter (Figure 2 b)) is equivalent to Σ-Δ converter with input bias voltage $V_B$ and $\pm V_{re}$ reference voltage (equivalent reference voltage). Equivalent reference voltage $V_{re}$ is given by:

$$V_{re} = \frac{|V_{r1}| + |V_{r2}|}{2} = \frac{C_1 + C_2}{2} \tag{4}$$

and input bias voltage $V_B$ is:

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$$V_B = \frac{|V_{r1}| - |V_{r2}|}{2} = \frac{C_1 - C_2}{2} \tag{5}$$

where $V_{r1} > V_{r2}$ and $C_1 > C_2$. Output frequency for equivalent Σ-Δ converter with input bias voltage $V_B$ and $\pm V_{re}$ reference voltage is given by (6):

$$f_O = f_{CLK} (1 - V_B / V_{re}) / 2 \qquad \text{[Hz, V]} \tag{6}$$

after substitute (4) and (5) in (6), the MSDC output frequency (in open loop) is:

$$f_O = f_{CLK} C_2 /( C_1 + C_2) \qquad \text{[Hz, F]} \tag{7}$$

or for $i_1$ and $i_2$ output frequency is:

$$f_O = f_{CLK} i_1 /( i_1 + i_2) \qquad \text{[Hz, A]} \tag{8}$$

From (7) and (8) is shown, that MSDC output frequency is nonlinearly dependent on capacitance (or current) changes. Graph of the relative output frequency on capacitance value change is shown in

Figure 4. In closed loop (phase locked loop), the $i_2$ is changed, so that change in $C_1$ or $i_1$ is compensated.

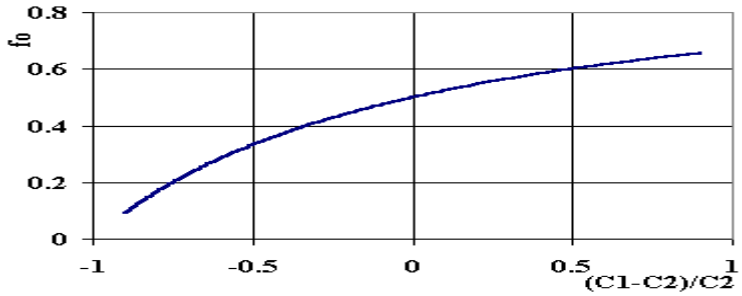


Figure 4. Graph of the relative output frequency ($f_{CLK}$ =1) in dependence on capacitance $(C_1 - C_2)C_2$ change in open loop system.

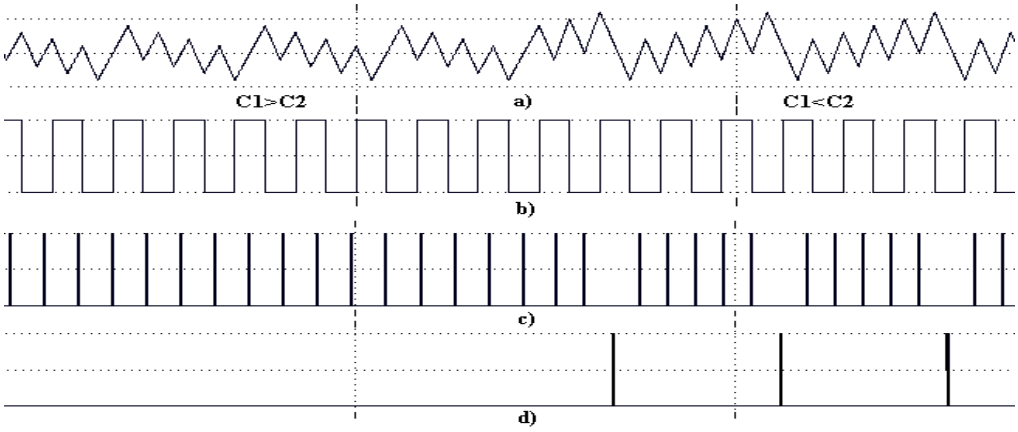


Figure 5. Open loop system time diagram. a) voltage on $C_1$, b) $f_{CLK}$ /2 pulses, c) pulses generated by Co1 comparator, d) additional pulses generated by logic.

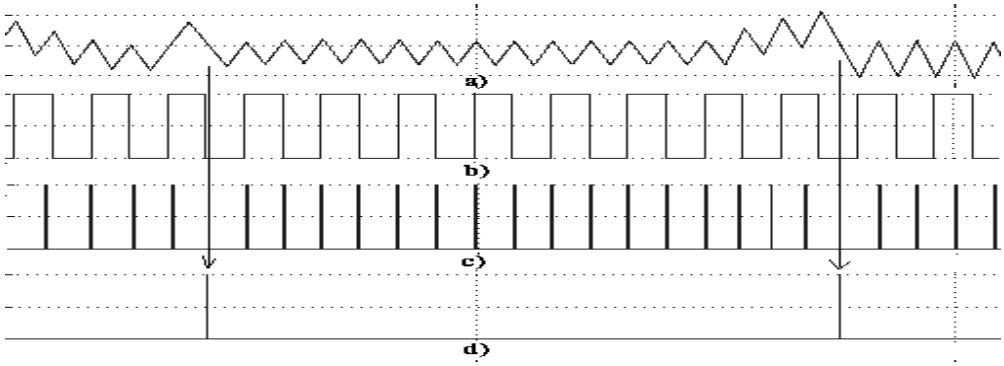


Figure 6. Closed loop (PLL) system time diagram. a) voltage on $C_1$, b) $f_{CLK}$ /2, c) pulses generated by Co1 comparator, d) additional pulses generated by logic

### III. MSDC simulation results

Simulations were performed to confirm the results of mathematics analysis. These results were obtained programming of MSDC equations. The MSDC has also been simulated in system level by SIMULINK (MATLAB). Simulation results (time diagram) of open loop system for *C1* value step change are shown in Figure 5. For open loop output evaluation, the output frequency of MSDC can be measured. Closed loop results are displayed in Figure 6. In booth time diagrams, additional pulses are generated so that output pulses = c) + d) are equally spaced. Simulation results for step change of $C_1$ (or in $i_1$) is shown in Figure 7, response on sinusoidal changes is shown in Figure 8. For this simulation, simple EX-OR phase decoder and 3-order Butterworth low-pass filter were used (9):

$$F(s) = \frac{1}{s^3 + 2s^2 + 2s + 1} \tag{9}$$

Analog output of the MSDC is on the low-pass filter output. Digital output can be derived on the phase detector output by means of counter and digital filter.

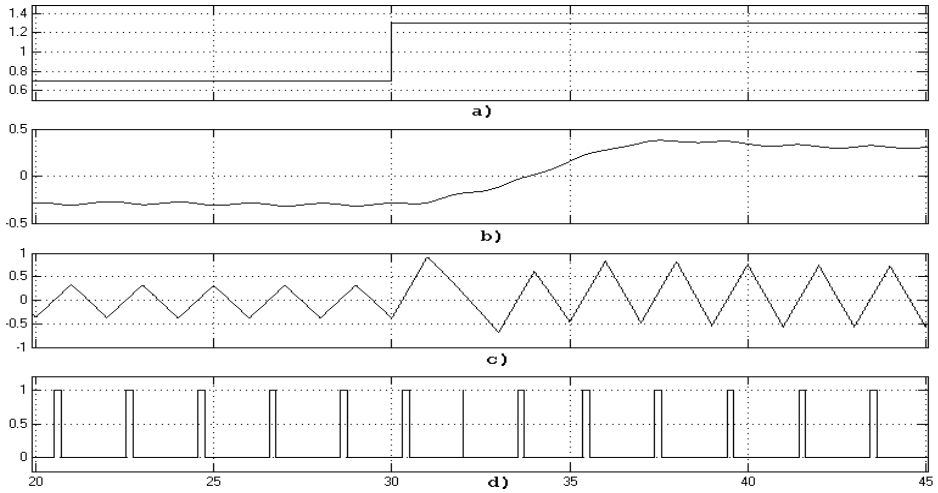


Figure 7. Step response of MSDC (closed loop). a) input step change, b) voltage on lowpass filter output, voltage on $C_1$, d) pulses generated by Co1 comparator and correction logic (narrow pulse is added by correction logic).

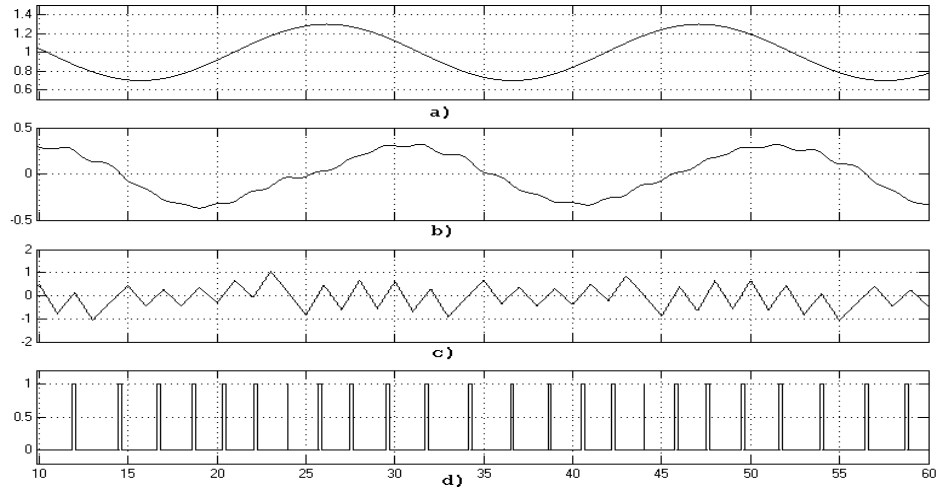


Figure 8. Sinusoidal response of MSDC (closed loop). a) input signal, b) voltage on lowpass filter output, c) voltage on $C_1$, d) pulses generated by Co1 comparator and correction logic (2 narrow pulses are added by correction logic).

The closed loop of MSDC can be improved by using a sequential phase detector and charge pump, which has a "Neutral" position. When the loop is phase-locked, there is a very little phase error, and booth of the sequential phase detector will be low. Hence, at phase-lock, the loop filter is connected to an open circuit that does not generate noise.

## IV. Flip-flop sensor

The standard flip-flop sensor (FF) consisting of 2 transistors and 2 resistor and additional parts [6]. The principle of measurement is based on the fact, that the measured non-electrical quantity breaks the value symmetry of the inverters of the FF [7]. Measured quantity can be compensated by the compensating voltage $V_C$ (or current) so that symmetry is recovered [8]. The analog and digital FF auto-compensative system is shown on Figure 9 a,b. Instead of simple transistors, the fast analog

switches were used [9]. In Figure 10 and 11, the simulations are shown, in Figure 12 and 13 experimental time diagrams are displayed. Assume, that $C_1 > C_2$, while the other parameters are identical, therefore voltage $V_2$ increases faster than $V_1$ and therefore when reach the Co2 comparator voltage, S1 is switched on and pulse is generated by means of OS2 one-shot. This pulse is processed in amplifier and integrator and compensating voltage $V_C$ is decreasing so that symmetry is recovered after several cycles. The compensating voltage $V_C$ can be computed from (10):

$$V_C \approx \frac{R(C_1 - C_2)}{C_1 + C_2} I_S \approx \frac{R\Delta C}{2C_S} I_S \tag{10}$$

where $R=R_1 + R_2$ and $I_S = I_1 + I_2$ (currents through $R_1$ and $R_2$). When the symmetry in FF is restored, the pulses on one-shots outputs (OS1 and OS2) appear alternately. This is shown in Figure 10, 12 and 13.

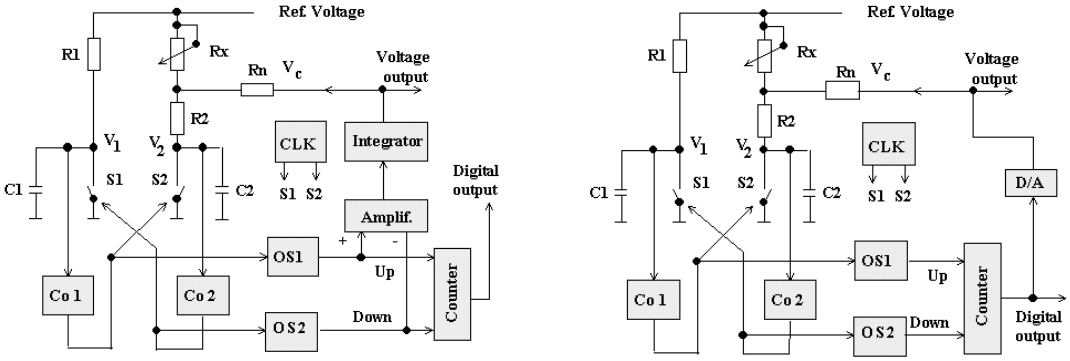


Figure 9 a) FF with analog feedback, b) FF with digital/analog feedback. Co - comparator, OS - one-shot, S1;S2 - analog switches, D/A - digital-analog converter.

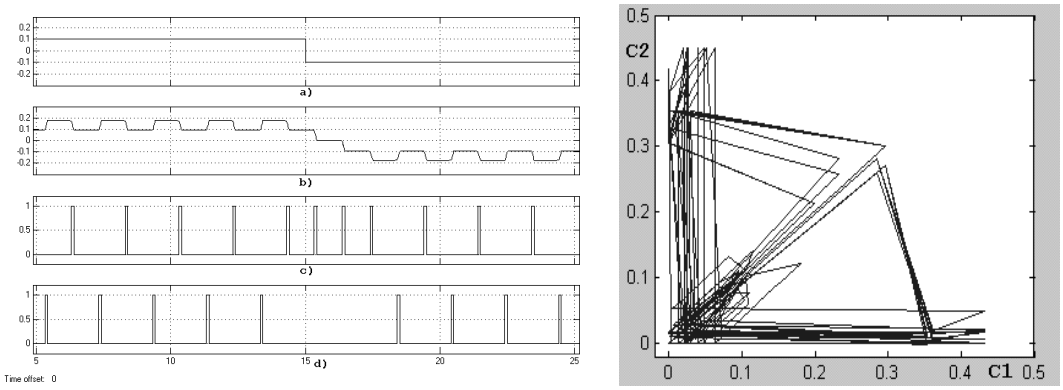


Figure 10. a) Input step change, b) Compensating voltage, c) OS1 pulses, d) OS2 pulses
Figure 11. Voltage on C1 and C2

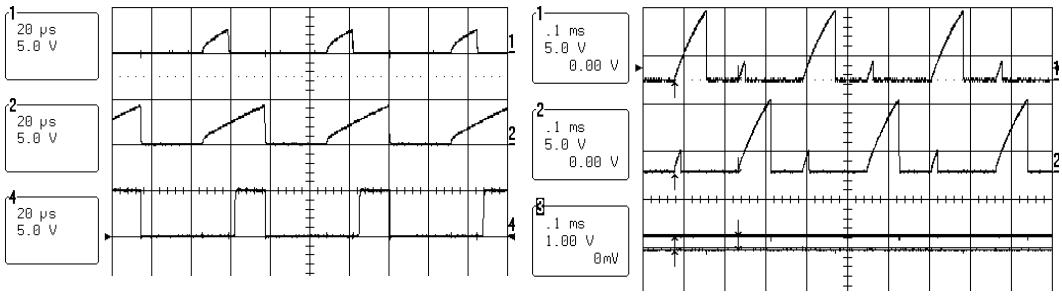


Figure 12. Measured time diagrams during - no symmetry, $C_1 < C_2$, [1]- voltage on C1, [2]- voltage on C2, [4]- Co2 (comparator) voltage.
Figure 13. Time diagrams - symmetry recovered, [1]- voltage on C1, [2]- voltage on C2, [3]- compensating voltage.

## V. Conclusions

Non-expensive measuring capacitance within the range of few pF is more and more important because of using e.g. micromachined ultrasound transducers in a wide variety of applications such us as medical imaging, acoustic vision, proximity detection etc.

In this paper, a two new method for non-electrical quantities, especially capacitance were presented. The first one is based on modified sigma-delta converter with compensated loop based on phase locked loop. This system can work in open or closed loop and has a fast response, but is more expensive and complicated.

The second system is based on flip-flop sensor with auto-compensating possibility. This system is simple and can be simply integrated, but it hasn't a fast response. Booth systems is possible to use for capacitance measuring in range of few pF, and are capable to give output information in analog or digital version.

The systems were mathematically solved, simulated and partly experimentally developed. The results of simulations and measuring are also presented in this paper.

## ACKNOWLEDGMENT

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