

Design, implementation and performance evaluation of a fully programmable twin-channel time interval generator

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Abstract – A programmable time interval generator, which is characterized by a resolution below the 50 ps, has been designed and fully implemented. The very high time-resolution is achieved by means of the synchronization between a down-counter and a digitally synthesised sinusoidal signal, whose phase can be tuned with a 14-bit resolution. The generator prototype presents two identical synchronized channels, whose outputs can be merged on the same time-axis allowing for high flexibility in the generation of the overall time interval sequence.

I. Introduction

Reliable and high-performance time-axis implementation is an essential issue in the design of modern instrumentation. Focusing the discussion on sampling instruments (even though several other applications could be considered), the increasing need for both wider digital bandwidth and improved accuracy has led in the last years to the identification of refined sample processing algorithms, which are based on non-conventional sampling interval generation. Since such numerical procedures take advantage from the acquisition of signal samples at *non-uniformly* distributed time instants (according to deterministic and/or stochastic mathematical laws), highly flexible and fully programmable architectures are needed, which are aimed at the time-domain control of digital acquisition channels within the measurement set-ups.

In this paper, the techniques adopted for the design and implementation of a time interval generator capable of synthesising sequences of pulses, which can be very different from those usually associated with conventional periodic sampling, are described. The system is based on two identical and separately programmable channels, each characterized by a very high time-resolution, which is obtained exploiting the synchronization between a sinusoidal signal with numerically-controlled phase and the output of a programmable digital counter. The instrument achieves the highest flexibility when the outputs of the two channels are merged on the same time-axis: under such operation the overall sequence of pulses can be generated according to almost *any* theoretical algorithm.

II. The system architecture and techniques adopted

In order to synthesise two gate pulses placed at a predetermined distance along the time-axis, a simple down-counter can be used. The time interval $\Delta T_k = t_{k+1} - t_k$ can be generated by initializing the counter internal state to the ratio $N_k = \Delta T_k / T_C$ (T_C being the period of the clock applied to the counter), starting the count process at the instant t_k and exploiting the end-of-count gate transition as a trigger for the generation of the pulse, which represents the right-bound of the interval. This basic, simple procedure is clearly affected by a finite time-resolution T_C , whose minimum value is strongly limited by the technology adopted for the counter implementation.

When a very high resolution is needed (say below 1 ns) an extended architecture can be taken into account, which preserves the reliability of moderately low-clocked digital counters and at the same time allows for a time-resolution several orders of magnitude higher than the clock cycle. In this paper a two-channel time interval generator is presented, which is characterized by a time-resolution below 50 ps. Figure 1 describes the main functional blocks within each channel. The sequence of intervals along the system time-axis is pre-computed by a 32-bit, 150-MHz Digital Signal Processor (DSP) (controlling *both* channels) according to the desired algorithm and stored into the RAM memory banks available on the board. A Complex Programmable Logic Device (CPLD) is in charge of passing the data both to a down-counter and a 14-bit phase-

programmable sinusoidal synthesiser (represented in the figure simply by its output D/A converter), whose output waveform is synchronised to the internal state of the counter as shown in Fig. 2. In order to generate the k th time interval ΔT_k , the counter is initialized to the state N_k and starts to count as in the basic solution. In the meanwhile, the synthesiser registers are programmed to cause a proper phase shift $-\Delta\phi_k$ in its output: in correspondence with the end-of-count gate

signal (which is sent to the D input of a very fast Flip-Flop device), a time delay $T_k^{(\phi)}$ occurs before the sinusoidal signal assumes a positive value (i.e., at the zero-crossing) and a transition at the output of the Flip-Flop is obtained. The overall time interval ΔT_k is therefore the result of three successive time contributions:

$$\Delta T_k = (N_k^{(init)} T_C - T_{k-1}^{(\phi)}) + N_k T_C + T_k^{(\phi)} \quad (1)$$

$N_k^{(init)}$ being the number of clock cycles needed for the initialization of the counter registers before the k th counting process starts. Equation (1) shows the flexibility of the designed instrument. The use of a 150-MHz counter allows for the presence of long time intervals (> 1 s) in the generated sequence without problems of count overflow, while the finely 14-bit tuneable time $T_k^{(\phi)}$ leads to a theoretical time-resolution of 0.6 ps, independently of the ΔT_k duration. Since the DSP unit controls both channels, time sequences can be generated with even more flexibility by considering the two outputs as merged along the *same* time-axis. In particular, this allows for the generation of sequences according to special-purpose algorithms, whose application can theoretical lead to couples of adjacent pulses with *infinitesimal* time separation. This is the case of randomized sampling techniques adopted for alias-free, wide-band spectral analysis [1-3].

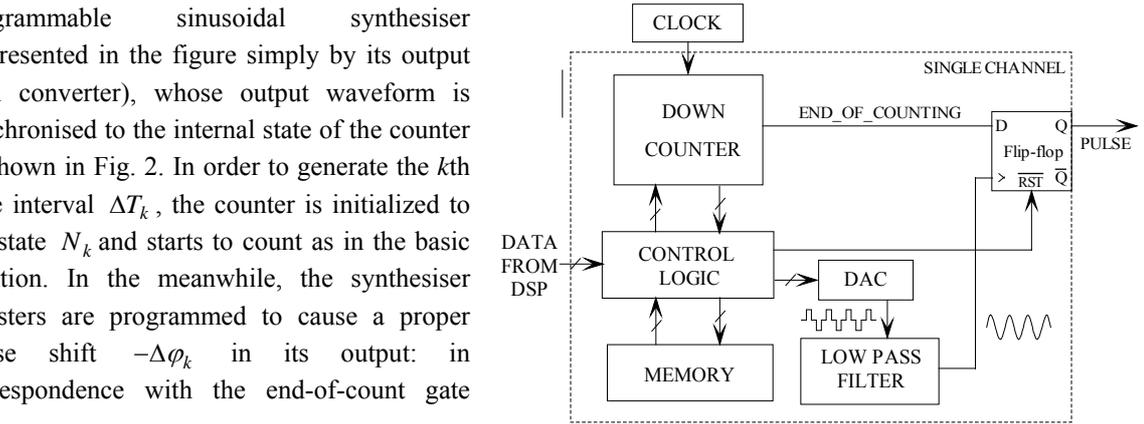


Fig. 1 – Functional blocks within the architecture of each channel of the proposed time interval generator.

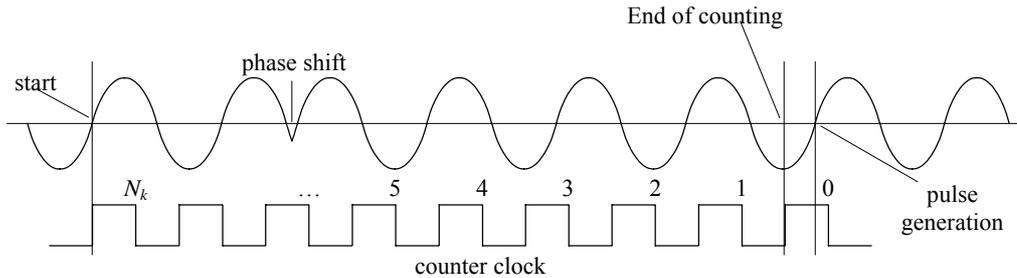


Fig. 2 – Time diagram showing the synchronization between the output of the 14-bit phase-varying sinusoidal synthesiser and the internal state of the down-counter.

III. Hardware implementation

The proposed time interval generator has been implemented through a couple of separate boards, in order to achieve the maximum flexibility. A mother-board based on a TMS320C6711 32-bit floating point 150-MHz DSP device is in charge of controlling the overall system. The DSP is supported by 128 kB of flash memory, which contains the main code, and 16 MB of SDRAM for data storage and processing. The mother-board is provided with a JTAG connector for emulation and debugging, as well as an expansion daughter card interface, which allows for the interconnection with external additional boards. By means of this digital

interface, a daughter-board has been connected to the DSP one, on which the time interval generation hardware is mounted. This board is based on the Analog Devices AD9852 frequency-tuneable Direct Digital Synthesis (DDS) device. The main features of this component are: 300-MHz internal clock frequency, 12-bit DAC, internal ultra-high speed comparator (3-ps rms jitter), internal look-up table for cosine signal generation. In Fig. 3 the operation principle of a frequency-tuneable DDS is illustrated. An n -bit variable-modulus counter (without carry) with internal phase register is implemented in the circuit before the sine lookup table. The output of the phase register is a digital saw-tooth with variable period. If T_c is the period of the clock signal, the period T_o of the output sinusoidal signal is expressed by the following equation:

$$T_o = \frac{2^n}{M} T_c \quad (2)$$

where n is the number of bits of the phase register (48 in the AD9852) and M is the counting process modulus, i.e., the value by which the phase register increments at each counting step.

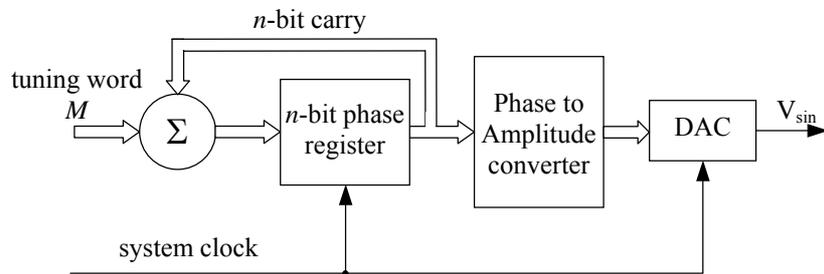


Fig. 3 – Operation principle of a freq-tuneable DDS

By exploiting such a DDS device, the synthesis of sinusoidal signals with different frequencies, which depend on the value of M , is possible. In addition, the phase of the generated sinusoidal signal can be set to a pre-determined value as well, by mean of a 14-bit phase-offset register available within the architecture of the DDS device.

The AD9852 is also provided with an internal down-counter (update clock counter). The DDS device external clock frequency has been set to 50 MHz, while the internal frequency f_c achieves the 300 MHz (by using the internal clock multiplier). The 32-bit down-counter has been then clocked at 150 MHz ($f_c/2$), so the maximum duration of the generated time interval is approximately equal to 28.6 s. The value $f_o = 100$ MHz has been chosen for the frequency of the synthesised sinusoidal signal. From this last value, remembering that the phase register is 14-bit wide, it can be deduced that the theoretical resolution of the generated time interval is less than 1 ps. Obviously, the presence of undesired effects within the circuit, such as the phase-noise of the synthesised sinusoidal signal, the jitter at the gate level and the noise at the input of the Flip-Flop, introduce an uncertainty of the actual interval width, which can be estimated to the value of several tens of ps. This uncertainty should be taken into account when choosing the resolution by which each time interval has to be generated. In fact, this parameter should be quite higher than the uncertainty, in order to make negligible the non-idealities and achieve a reliable implementation of the resolution value at the output of the instrument.

In order to reduce the computational load of the DSP device, the time interval generator is equipped with 2 MB of RAM that can be exploited for the storage of digital data, which codify the width of a large number of time intervals to be generated in sequence. Thus, a new sequence of intervals can be computed by the DSP, while the first one is being physically generated by the hardware (Fig. 4).

The output of the DDS D/A converter are the samples of a sinusoidal signal in differential form (three samples per period): in order to obtain a smoother, sinusoidal-like signal, an antialias low-pass (7th order elliptical) filter with a cut-off frequency of 100 MHz has been implemented at the output of the DAC. The output of the filter is applied to the clock input of a LVPECL (Low Voltage Positive Emitter Coupled Logic)

Flip-Flop device (MAXIM MAX9381), whose D input is controlled by the end-of-count gate transition at the output of the down-counter (Fig. 1).

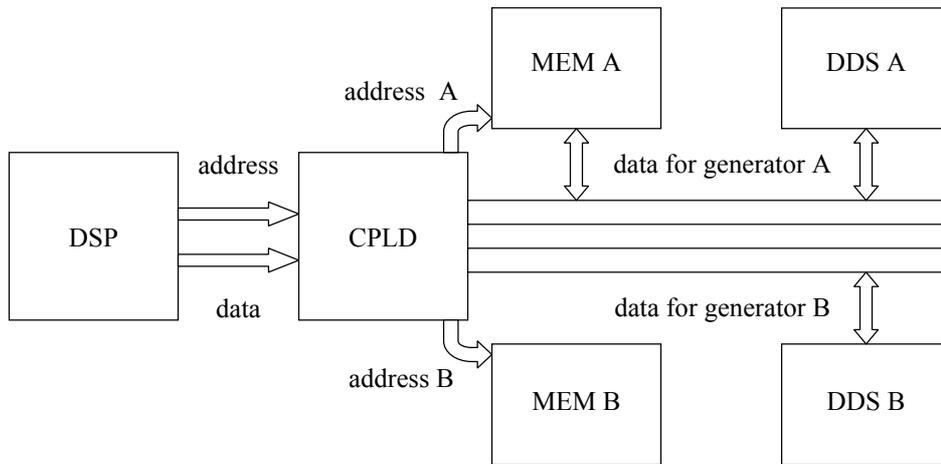


Fig. 4 – Twin-channel block diagram of the generator control circuit.

IV. Experimental results

| Time interval (ms) | Jitter (ps) | Number N of measurements |
|--------------------|-------------|----------------------------|
| 0.01 | 32 | 10000 |
| 0.01 + 1 ps | 34 | 10000 |
| 0.02 | 36 | 10000 |
| 0.02 + 1 ps | 37 | 10000 |
| 1 | 35 | 1000 |
| 1 + 1 ps | 35 | 1000 |
| 10 | 70 | 1000 |
| 10 + 1 ps | 70 | 1000 |

Tab. 1 – Statistical analysis of jitter in the generation of time intervals of equal duration.

In this section, some experimental results, which have been obtained in order to test the performance of the time interval generator prototype, are presented.

Tables 1 and 2 give results for two different tests:

- Tab.1: jitter statistical analysis (3σ) performed by operating the prototype for the generation of N time intervals of equal duration. The experimental mean value of the time interval duration differs from the nominal value of 5÷10 ppm, according to the DDS oscillator specifications.
- Tab.2: statistical analysis on the mean value and standard deviation dispersions when generating successive time interval sequences, each described by a gaussian distribution with nominal, predetermined expected value and standard deviation.

| Mean value (nominal) (ms) | Standard deviation (nominal) (ns) | Mean value dispersion (σ) (ns) | Standard deviation dispersion (σ) (ns) |
|---------------------------|-----------------------------------|---|---|
| 0.01 | 1 | 0.02 | 0.02 |
| 0.01 | 10 | 0.2 | 0.3 |
| 0.01 | 100 | 2 | 3 |
| 0.01 | 1000 | 10 | 30 |
| 1.0 | 1 | 0.05 | 0.02 |
| 1.0 | 100 | 3 | 3 |
| 1.0 | 10000 | 400 | 400 |
| 1.0 | 100000 | 10000 | 10000 |

Tab. 2 – Statistical analysis of the dispersion of mean value and standard deviation in sequences of time intervals with predetermined gaussian distribution.

V. Conclusions

A twin-channel, fully-programmable time interval generator, which is capable of providing time sequences according to a wide set of both deterministic and/or stochastic analytical algorithms, has been designed, implemented and tested. The solutions adopted within the system architecture have allowed to achieve a time-resolution below the 50 ps, independently of the duration of the generic time interval inside the sequence. In addition, the synchronization between the two independently programmable channels available into the instrument allows for the generation of special purpose, ultra-short time intervals, like those which are essential to the implementation of non-conventional sampling strategies.

VI. Acknowledgements

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