ΣΔ-Based Removal of Unwanted Spectral Components for Sinewave Synthesis

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***Abstract*-**This paper addresses the generation of spectrally pure sinewaves by combining the feedback structure of a ΣΔ loop with digital cancellation of unwanted spectral components in the output signal. In particular, the non-linearities of the in-loop Digital to Analog Converter (DAC) are compensated by applying a digital pre-distortion to the DAC input, and the feedback architecture is used to enhance the performance of the all digital estimation and cancellation algorithm.

I. Introduction

Direct Digital Synthesis (DDS) of spectrally pure sinewaves is the subject of various research activities, because the high stability and frequency resolution achievable with respect to analog solutions make this technique useful for testing purposes [1]. DDS relies on a Digital-to-Analog Converter (DAC), which generates a digitized version of the desired signal using data stored in a Look-Up Table (LUT). Finally, the DAC output is often filtered in the analog domain for smoothing purposes [2][3]. With such an architecture, the non-linearity of the DAC greatly affects the spectral purity of the generated signal, causing unwanted spectral components [4]. Various solutions have been considered in the literature to mitigate such effect [2][5]. For example, in [2] a spectrum analyzer is used for estimating the phase of undesired spurious components in the analog domain. Then, the spurious components are removed by acting on the DAC input. A similar technique is followed in this paper. In fact, the presented solution, based on a modified ΣΔ architecture, estimates both amplitude and phase of the DAC generated narrow-band components in the digital domain and removes them by pre-distorting the DAC digital input. It is shown, by means of both simulations and experimental verification, that this technique effectively removes most significant undesired spectral components introduced by the DAC. As the presented technique is an all-digital one, it allows the implementation of low-cost signal generators with a high Spurious Free Dynamic Range (SFDR).

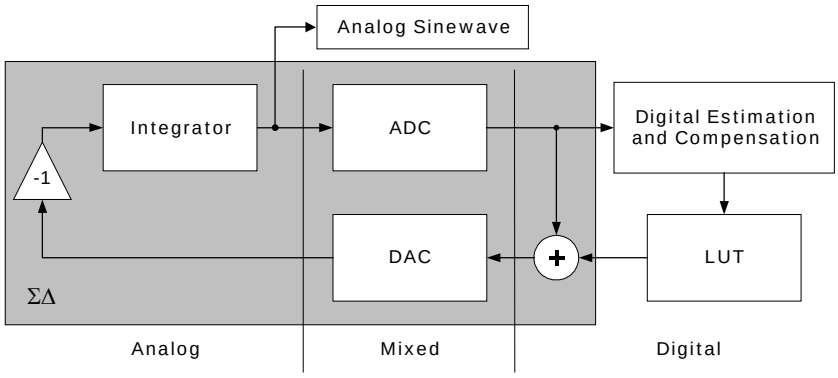


Fig. 1: The modified ΣΔ architecture

II. All-digital removal of unwanted DAC spectral components

Fig. 1 reports the considered 1st order ΣΔ modified architecture used for the sinewave synthesis. The system input is moved from the input of the integrator to the digital input of the DAC, and is stored in the LUT. The DAC produces an amplitude quantized analog signal, which is then smoothed by the integrator. As reported in section I, the DAC non-idealities introduce unwanted spectral components which reduce the system SFDR. In order to remove such terms, the output sinewave is sampled and

quantized by the forward path Analog to Digital Converter (ADC). Then, the ADC output is digitally processed, and a Fourier analysis is carried out for measuring amplitude and phase of unwanted terms. Notice that, in order to estimate the parameters of such components at the output of the DAC, the closed loop discrete time transfer function relating the DAC output and the integrator output is properly kept into account. It is worth of notice that the estimation of DAC induced harmonics may be carried out without resorting to a feedback architecture, but in this case the ADC non-linearity should be much lower than the DAC one. In fact, under such conditions the Fourier analysis cannot distinguish between harmonic components generated by the DAC and those introduced by the ADC. Thus, a digital pre-distortion algorithm may attempt to correct harmonic components due to the ADC, generating cancellation terms which would appear as unwanted components at the DAC analog output. Conversely, when a feedback architecture is adopted, provided that deep overloading is avoided, the ADC noise and non-linearity do not significantly influence the measurement results. In fact, in this case the system is desensitized with respect to the ADC non-linearities and noise. The characterization results are used to update the LUT, inserting for each detected unwanted component a canceling term, with the same amplitude and a relative phase shift of π radians, which is added to the ADC output in the feedback path. Provided that the DAC does not present strong non-linearities, such a strategy is expected to cancel or strongly reduce any unwanted spectral component. It is worth of notice that each time a spectral component is corrected, the DAC may introduce new harmonics or spurious terms, because of its non-linear behavior. Thus, an iterative algorithm has been applied, which identifies and cancels unwanted spectral components one at a time, always choosing the one with the largest magnitude. The cancellation of a single component is also iterative, and it has been observed that less than five cycles are usually needed to completely remove an undesired term. Thus, after a training phase, the LUT stores a pre-distorted signal capable of removing all of the significant harmonics and spurious terms introduced by the DAC, and the estimation algorithm can be disabled. Observe that the presented methodology relies on destructive interference to cancel unwanted spectral components. Thus, the algorithm requires that the phase of each harmonic is measured with very high accuracy. This implies that the cancellation algorithm is to be repeated every time the sinewave frequency is changed. Moreover, in order to minimize noise effects and improve estimator accuracy, the phase is estimated by performing a Discrete Fourier Transform (DFT) analysis on the average of several sinewave records [6][7]. Since the signal is obtained from a look-up table, synchronization, needed to effectively combine different records in the DFT analysis, is easily achieved. Notice that the record length may be arbitrarily chosen, depending on the desired signal frequency and duration, the DAC sampling rate, and the LUT capacity. Hence, the proposed technique is suitable for the synthesis of a testing signal, which usually requires the generation of a given number of stimulus samples. As shown in the following sections, the considered procedure has been successfully applied to improve the output SFDR of a simulated 8 bit DAC by over 10 dB, and in an experimental setup the SFDR of a 16 bit DAC by nearly 15 dB.

III. Analysis results

The algorithm described in section II has been validated using behavioral simulations of an 8 bit DAC with unitary valued Full Scale *FS*, affected by a Gaussian distributed Integral Non-Linearity (INL), with standard deviation σ_{DAC} equal to $\Delta_{\mathrm{DAC}}/3$, where Δ_{DAC} is the DAC quantization step. In order to analyze the effect of forward path non-idealities, an 8 bit ADC has been considered, with *FS*=1 and Gaussian distributed INL with standard deviation σ_{ADC} equal to $\Delta_{\mathrm{ADC}}/3$, where Δ_{ADC} is the ADC quantization step. Fig. 2(a) and 2(b) report the spectrum, estimated at the output of the integrator, of a low frequency carrier with amplitude A=0.5, respectively before and after applying 18 times the iterative digital pre-distortion algorithm. The initial content of the LUT was the desired carrier, affected by a dither, white and uniformly distributed in $[-\Delta_{\mathrm{DAC}}/2, \Delta_{\mathrm{DAC}}/2]$ [8]. Phase estimations were carried out by averaging and FFT analyzing 30 consecutive quantized sinewave records, collected at the ADC output [6][7]. It has been observed that the proposed algorithm, obtained using records of 2^{14} sinewave samples, quickly converges to a highly pure signal. In fact, several low frequency harmonics were already canceled after three iterations, and after eleven cycles there were only very small residual components at low frequencies.. As shown in Fig. 2(b), after 18 iterations, the unwanted component were mostly reduced to the noise floor, greatly enhancing the SFDR. Moreover, the number of iterations needed to obtain a pure sinewave is actually lower than the number of uncompensated harmonics of Fig. 2(a). This is because, due to the feedback loop, the unwanted components reenter the DAC and introduce their own harmonics. Moreover, it can be observed that the noise floor in Figs 2 is nearly flat. This is due to the fact that at the output of the integrator both ADC and DAC error powers are not spectrally shaped by the $\Sigma\Delta$ loop. The small residual shaping in Fig. 2(a) and 2(b) is due to the

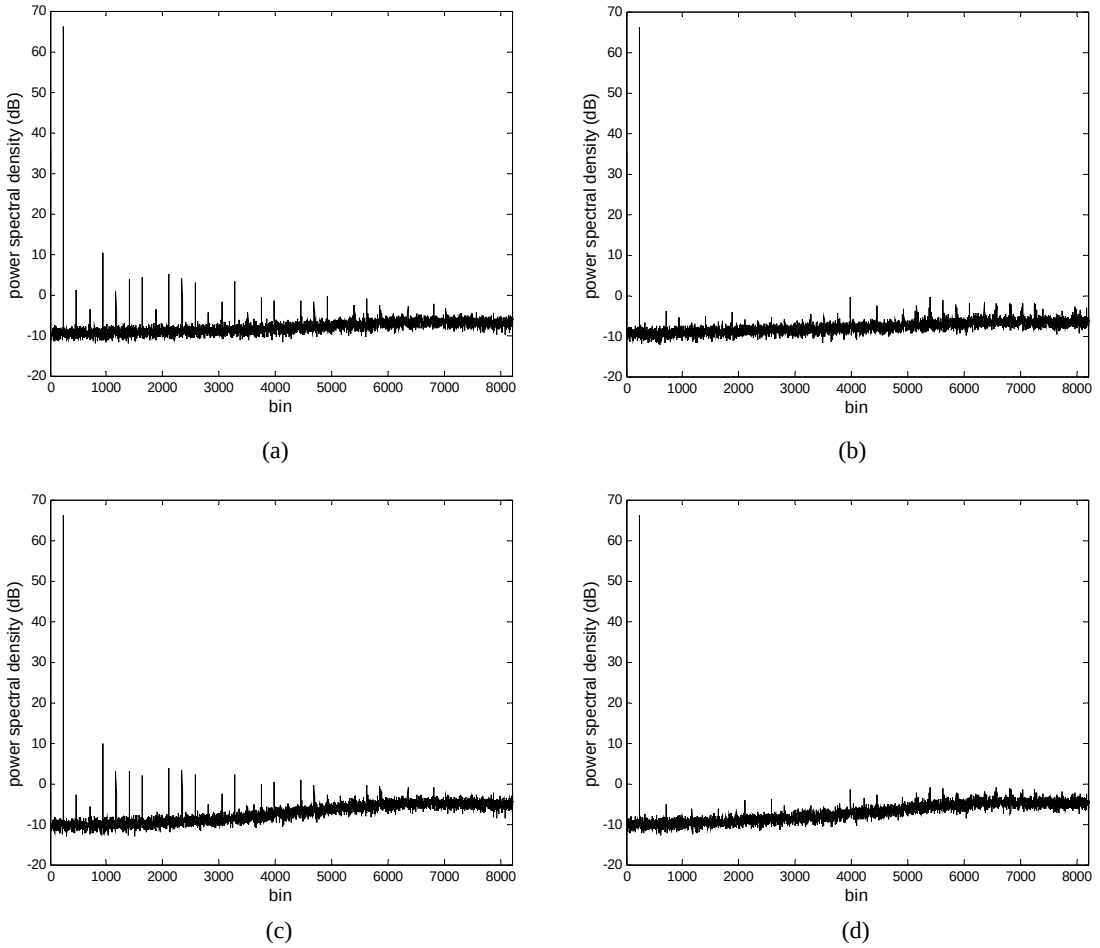


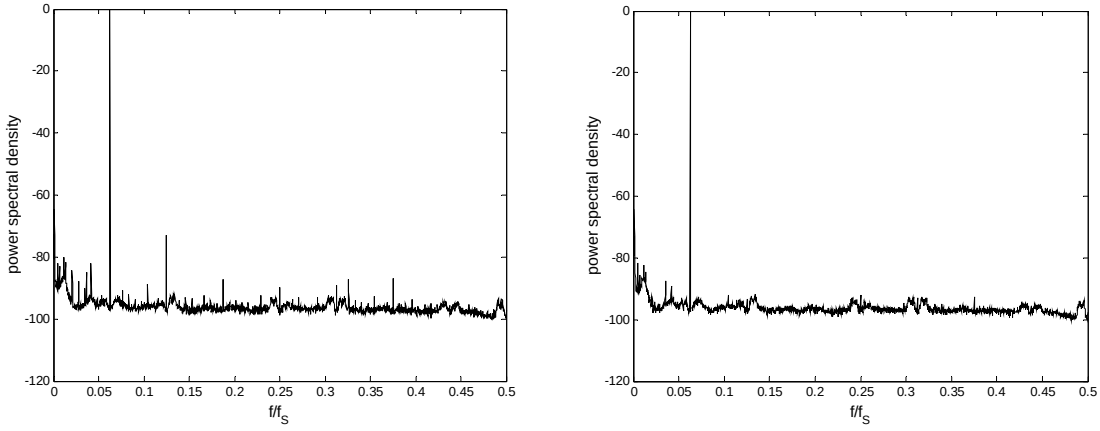
Fig. 2: Iterative cancellation of unwanted spectral components. The sinewave spectrum obtained at the output of the integrator before and after applying the correction algorithm is reported in (a) and (b) respectively, while (c) and (d) report the ADC output spectra, before and after applying the correction algorithm respectively.

interaction between the LUT output, which is mainly white, and quantization noise at the ADC output, which is shaped by the ΣΔ loop. To gain further insight, the signal spectrum has been analyzed also at the output of the ADC, that is where the harmonics are identified, and at the DAC input. For instance Fig. 2(c) and 2(d) report the ADC output spectra corresponding to the DAC input spectra of Fig. 2a-b. It can be observed that in this case the ADC noise is spectrally shaped by the loop, and that the harmonics are mostly those reported in Fig 2(a) and 2(b). Finally, it can be observed that after applying the cancellation algorithm, the remaining unwanted component are mostly high frequency ones, since those terms are not easily estimated from the ADC output due to the noise shaping. The algorithm has been tested also by reducing the ADC resolution, showing that by using a 7 bit resolution ADC the algorithm is still capable of improving the SFDR.

IV. Experimental Verification

In order to validate the results of sections II and III, experimental data have been collected, using a Texas Instruments DSK TMS320C6713 development board. This system features a 220MHz C6713 DSP, 16 MB SDRAM, a 16 bit ADC and a 16 bit DAC both with a Full Scale range of about ±1.4V, operating at a sampling rate of 96 kSa/s. In order to correct DAC non-linearities, using the proposed methodology, a continuous-time ΣΔ architecture as that shown in Fig. 1 has been implemented, by using an op-amp based, first order, low pass filter as integrator, having a 2^{12} sample sized look-up table in the board memory, and programming the DSP to carry out the loop related processing. The DFT analysis and generation of cancellation terms needed to update the LUT was performed offline on a PC, downloading each record acquired by the ADC from the DSP board to the PC, evaluating the harmonic removal terms using MATLAB, and finally uploading evaluated LUT values to the board.

The system was programmed to generate a 3 kHz sinusoidal carrier, with zero DC component and a



(a) (b)

Fig 3: Iterative cancellation of unwanted spectral components. The sinewave obtained before applying the correction algorithm is reported in (a), while (b) is obtained after applying the harmonic removal algorithm to the C6713 DAC.

peak amplitude of about 50 mV. In particular, the transfer function between the DAC input and the integrator output was measured at the given frequencies by using the ADC data, and the correction algorithm was used without iterating the cancellation of each single unwanted harmonic. Fig. 3 reports the results of the compensation algorithm on the ADC output spectrum. In particular, the abscissa reports the frequency, normalized to the sampling frequency. Conversely, the vertical axis reports the carrier power in dB, normalized to the fundamental component. It can be observed, even using a simplified algorithm, that the unwanted harmonic content of the sinewave generator is effectively removed, improving the SFDR of about 15 dB.

V. Conclusions

An all-digital technique based on a ΣΔ architecture has been described, which allows to generate highly pure sinewaves by pre-distorting the digital DAC input. A fast converging iterative algorithm has been presented, which effectively estimates and removes the unwanted spectral components introduced by the DAC. Both simulation and experimental activity were carried out to validate the proposed algorithm, showing that the feedback architecture allows a very accurate all digital estimation and correction, considerably improving the output SFDR and desensitizing the system performance with respect to the ADC resolution and non-linearity. As a future development, the phase estimation and canceling terms generation will be delegated to the board DSP, thus implementing a fully stand alone self calibrating generator.

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