

# NEW TRENDS IN ANALOG TO DIGITAL CONVERTERS TESTING

António Cruz Serra

IT/ DEEC, IST, Universidade Técnica de Lisboa, Av. de Rovisco Pais, 1049-001 Lisboa,  
Portugal.

Ph: +351-218418490 Fax: +351-218417672, E-mail: acserra@ist.utl.pt

## ABSTRACT

In this paper, new state of the art analog-to-digital converters (ADCs) testing techniques both static and dynamic are revised and discussed.

Regarding the static test it is shown that a new technique based on the use of small triangular waves superimposed with a variable offset value as input signal, reduces dramatically the test duration. This histogram based technique can be implemented by using low cost generators even for high resolution ADC testing.

In relation to the dynamic test, a variant of the traditional histogram test using Gaussian noise as stimulus signal is discussed. It allows the test of high frequency, or high resolution ADCs in those cases where the traditional sinusoidal stimuli are not available with the required spectral purity. New techniques to grant convergence of the traditional four-parameter sine fitting algorithms traditionally used in time domain tests are also revised.

Keywords: ADC Testing, Histogram test, Sine Fitting.

## I. INTRODUCTION

Traditional analogue instruments have been nowadays almost completely substituted by digital instruments. The physical and the digital worlds are interfaced by analog-to-digital-converters that transform the quantities to be measured in digital data. Consequently, ADCs performance has a determinant impact on the performance of digital instruments, and on the quality of the measurement systems.

ADCs are traditionally tested as described in IEEE 1057 [1] and 1241 [2] standards. The development of new faster, cheaper and/or more accurate ADC testing procedures, able to characterize high resolution and high frequency converters is nowadays one of the main tasks in Instrumentation and Measurement.

The performance of the same converter under different conditions tends to vary, in some cases very strongly, fig.1. Consequently tests should be performed in conditions (input signal frequency and amplitude and sampling frequency) similar to those where they are expected to be used. Fig.1 results show that ADCs performance limit not only the accuracy but also the bandwidth of the instruments where they are included.

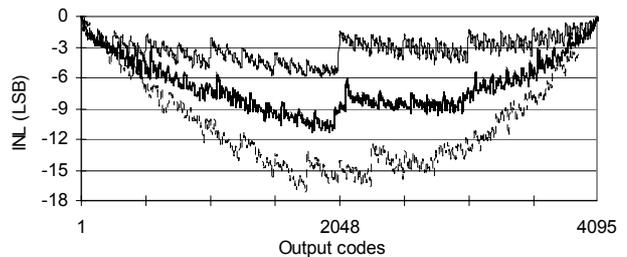


Fig. 1. *INL* of a 12 bit ADC, measured by using the traditional histogram test as described in [1] with a sampling frequency of 10 MHz and input sinewaves of 1 kHz, 20 kHz and 60 kHz.  $|INL|$  increasing for increasing input frequency.

When the converters are to be used to acquire very low frequency signals, the static test is mandatory. In all other cases a dynamic test must be performed. Dynamic tests generally used can be divided in time domain, frequency domain and statistical domain tests. All test procedures present advantages and drawbacks.

The main problem with the traditional static test procedure [1] is the unacceptable time duration of the tests for medium and high-resolution converters. The equipment required to test these converters with accuracy better than a small fraction of an LSB is also very expensive and consequently not available in many circumstances. Another problem is the inexistence of input stimulus sources to characterize state of the art very high resolution ADCs.

Regarding the traditional dynamic testing techniques, all of them are based on the use of “ideal” sinusoidal input stimulus (except in what concerns some time base tests). These ideal sources obviously do not exist and the validity of the approximation of considering them ideal will be lost when very high frequency or very high-resolution converters are under test. Other severe problem on these tests is the difficulty to assure coherent sampling in many cases.

The group Instrumentation and Measurement of the Institute of Telecommunications and of the Department of Electrical Engineering and Computers of IST, Technical University of Lisbon have devoted an important research effort on these subjects during the last decade. In this paper, some of the contributions of our group and the trends we foresee to solve some of the open problems on ADC testing will be presented.

## II. STATIC TEST

Given the large number of low frequency application of ADCs (low frequency data acquisition boards represent more than 90% of the total market share), this is a very important test, both for the industry and the consumers. However, researchers have devoted a small effort in the improvement of static test procedures in comparison with the work in dynamic tests.

Traditionally the test is performed as described in [1]. The transition levels are determined one at a time by applying a constant signal to the ADC input. The value of this stimulus signal is increased until it crosses each transition level,  $T[i]$ . After each stimulus signal change a set of samples is acquired. The number of acquired samples depends on the standard deviation of noise in the experimental setup ( $\sigma_n$ ) and on the required confidence and tolerance levels for the measurement. The value of each transition level is computed from the samples values and from the known values of the applied stimulus signal before and after transition level detection. This procedure is very time consuming because a high number of samples have to be acquired and processed. Furthermore it is necessary to wait for the output of the calibrator that generates the stimulus signal to settle each time it changes. This depends on the calibrator used but can go from a few milliseconds to more than one second. The duration of the test of a 12-bit converter can take several hours. If the sampling frequency is low, or the number of bits of the converter increases, the duration of the test becomes prohibitive. The calibrator used must have an output resolution lower than  $\frac{1}{4}$  of the ideal quantization width, which implies the use of medium to high cost calibrators. The higher the resolution of the converter, the costlier is the equipment necessary.

The need for an improvement in the static test was recognized during the development of the new IEEE 1241 standard [2]. A completely different procedure, in relation to IEEE 1057 std., was introduced [3,4]. It is based on the use of a feedback loop, where a DAC generates the feedback signal, applied to the ADC under test. The digital word input of the DAC, is incremented or decremented, depending on the result of the last ADC conversion. First the DAC generates a voltage slightly lower than the expected value for  $T[1]$ . After ADC conversion, the digital output code is compared with code 1. The DAC is incremented until the output code is greater or equal to code 1. The first time the comparator generates a decrement command a measurement time delay of 8 or 16 conversion times follows. The time delay is 8 if it is acceptable that the standard deviation of the measurement of the code transition to be greater than 15% of the converter noise, being 16 in the opposite case [2]. In fact, this time delay is the settling time for the ADC input. If the step size is smaller and/or

the rms value of noise increases the time delay should increase. After the time delay, IEEE 1241 procedure follows, by recording  $M$  measurements of the input signal of the ADC.  $M$  should be greater or equal to

$2 \times (\sigma_n / \varepsilon)^2$ , where  $\varepsilon$  is the allowable code edge uncertainty. The  $M$  data samples are averaged and the result reported as the code transition level  $T[1]$ . After finding this first transition level, the desired code is incremented and the procedure repeated until all code transition levels are measured.

The number of samples to be acquired for each transition level depends on the step size, but it will be always greater than  $9+M$ . All these samples are acquired at a rate that will be the smaller of the values of the settling time of the DAC and of the desired sampling period. Let us consider a 12 bit ADC. If  $\sigma_n$  is 2LSB and  $\varepsilon = 1/4$ LSB the number of samples to be acquired will be approximately  $(9+2 \times 8^2) \times 4095 = 561015$ . If the settling time is 1ms and the sampling frequency 1kHz, the duration of the test is more than 9 minutes. If the settling time changes to 100ms, the duration of the test will be 15h35m. It can be shown that this procedure is much faster than the static test described in [1] if the settling time of the DAC is low [5]. It is a very good solution if dedicated hardware, containing a fast DAC, is to be used. However it should be avoided if a general-purpose calibrator with a large settling time is considered for ADC input signal generation. The procedure is particularly interesting for high-resolution, low sampling rate ADCs, since in this case the duration of the test is limited by the sampling rate, and the number of acquired samples in this procedure is very low.

Given the importance of this test, we have been working for a long time on the reduction of the test duration and on the possibility of the use of low cost equipment to perform the static test [5-12].

Our first direction of work was the use of a variable step size to reduce the time consumption of the test both by reduction the number of changes of the calibrator output and the number of acquired samples [6]. Later the use of an extrapolated convergence factor method [5,8] based on the idea of calculate the increment to apply to the programmable source in the next iteration, from the results of the two last obtained records of data, in order to guess the position of the next code transition level was explored. It resulted in a reduction of the duration of the test by a factor between 2 and 4, depending on the ADC resolution, the required confidence and the noise present in the experimental setup. A very important behavior of this new method was that it performed worst in the absence of noise. The reason was obvious; the extrapolation of the next transition level,  $T[i]$ , was based on the stimulation of

different codes when a given DC value lower than  $T[i]$  was applied at the ADC input.

The idea of adding a small quantity of noise to the DC input, together with the use of all samples acquired in the previous records of data and built a histogram was growing up. A suggestion [9] to use small amplitude waves to test ADCs speed up the research. In fact, instead of adding uniformly distributed noise hard to generate, or Gaussian noise which would require a very accurate calibrator to generate de applied DC value, we begun to use small amplitude triangular waves with variable DC levels as stimulus signal for the static test [10-12], see fig. 2. This procedure is based in the traditional Histogram Method [13] but uses a uniformly distributed input signal that scans the ADC input range by increasing the DC level by steps.

The procedure requires several steps ( $N_s$ ). In each step, a small number of ADC codes are stimulated repetitively via small triangular waves. The shape of the stimulus signal is always the same in every step, but the DC level is changed from step to step.

Defining  $-V_r$  and  $V_r$  as the values of the first and the last transition levels, respectively, the DC offset ( $C_i$ ) of the stimulus signal used in the  $i$ -th step is:

$$C_i = -V_r + \frac{V_r}{N_s} + 2 \cdot i \cdot \frac{V_r}{N_s}, \quad i = 0, \dots, N_s - 1 \quad (1)$$

and the amplitude  $A$  of the stimulus signal is:

$$A = \frac{V_r}{N_s} \cdot (1 + \alpha), \quad (2)$$

where  $\alpha$  is the percentage of overdrive. Analogously as in the traditional histogram test, the ADC is overdriven in order to stimulate all the codes and to exclude the samples corrupted by noise in the extremities of the stimulus signal [10]. In the case of a triangular stimulus signal, the samples in the extremity have to be excluded also to avoid distortions due to the discontinuity in the signal derivative.

For all the codes stimulated by each of the small triangular waves, the DNL is calculated according to the histogram test procedure. The transition levels are estimated from the DNL values. Gain and the offset errors are corrected, and the final DNL and the INL vectors are computed.

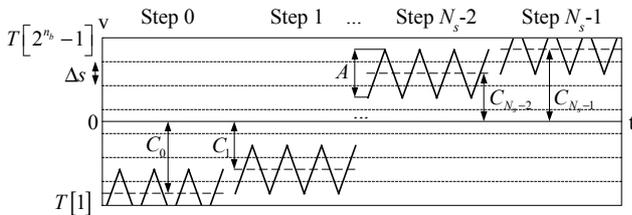


Fig. 2. Stimulus signal applied to the ADC.

This new procedure for the static test of ADCs reduces dramatically the duration of the test and allows the use of low cost equipment. The time duration of the test is reduced because the number of changes in the DC level generator is dramatically reduced, 80 to 100 changes are the maximum number of changes needed in any ADC. In many cases, good results are achieved with a much lower number of steps. This means that for instance for a 12-bit ADC the waiting time for the calibrator to settle is reduced from  $4 \times 4096$  to 80 to 100, i.e. a reduction of about 200 to 1! Another reason for the reduction of the test duration comes from the use of all acquired samples to compute all transition levels, it must be noted that in the traditional static tests [1,2] only a very small number of all acquired samples are actually used to determine the value of each transition level, and that after the computation of each level, all the previously acquired samples are discharged.

The histogram method requires the repetitive acquisition of a stimulus signal with a known amplitude probability function (*pdf*), a uniform *pdf* is preferred because it stimulates uniformly the ADC range as a whole. However, the practical difficulty of achieving economically highly linear full-scale generators leads to the extensive use of sinusoidal stimulus in the traditional dynamic test of ADCs [1, 13]. In this new procedure, since small amplitude and low frequency (to grant quasi static test conditions) triangular waves are used, very low cost generators can be used. Apart from that, the DC level generator for each step has very low accuracy requirements [10-12], leading to the use of very inexpensive equipment. The traditional test of a N-bit ADC requires a ramp input signal with a linearity better than  $1/(2^N - 1)$  of the full-scale for a 1LSB maximum error. For the presented test with  $N_s$  steps, the required linearity is  $N_s/(2^N - 1)$ . The more steps are used, the less severe are the requirements of linearity.

Figure 3 presents the results of the traditional static test, performed as described in [1] for a 12 bit data acquisition board. The rms noise level of the experimental setup was estimated to be 0.2LSB. The acquisition of records with 4096 samples assures an accuracy of 0.012LSB for the INL.

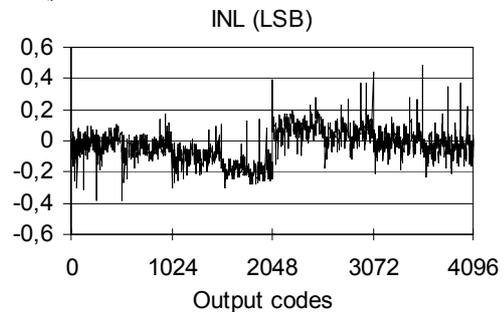


Figure 3. Results of the IEEE 1057-94 standard static test of a 12-bit data acquisition board.

In [12] the results of the new procedure performed by using small but increasing number of steps in order to highlight the relaxation of the linearity constraints for the triangular waveform generator were presented. It was shown that a triangular generator with a poor nonlinearity was capable of performing the test if the input range is divided into a convenient number of intervals. A test was performed by acquiring a total of 20 million samples leading to an uncertainty in the INL results lower than 0.01LSB with 99.5% confidence level. The difference between the results of the INL obtained with the histogram test and those obtained with the static test ( $\Delta\text{INL}$ ) is highlighted in fig. 4. It shows the results obtained with 200 triangular waves, each one with amplitude of 60mV.

$$\Delta\text{INL} = \text{INL}_{\text{histogram test}} - \text{INL}_{\text{static test}} \quad (3)$$

The error introduced in the INL by the poor nonlinearity of the generator in the case of a full-scale triangular wave had a maximum value of 3.5LSB. It was reduced to 0.0175LSB as can be seen in the central part of the INLs difference ( $\Delta\text{INL}$ ) in figure 4. The higher values of  $\Delta\text{INL}$ , in fig. 4, for lower and higher codes are due to the decrease of accuracy of the traditional static test, due to the increase of the rms value of noise generated in the calibrator used as DC input stimulus, due to the change of its output circuitry for different output ranges. A significant reduction of the testing time in relation to the static test was achieved. The traditional static test in fig. 3 took approximately 6 hours and the test with the new method took only about 5 minutes.

Experimental tests were also performed in other converters, with different architectures. The validity of the procedure was verified also in these cases. Work on the required number of samples for a given tolerance and confidence pair is now being refined. In our opinion this is a very efficient and simple procedure and it should be included in the new standards. For that it is necessary to prove the validity and robustness of the procedure by using it in different Laboratories.

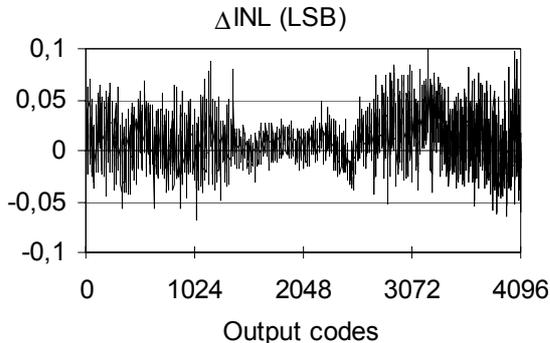


Figure 4 - INL difference of the small amplitude waves test results with 200 triangular waves and the traditional the static test results of figure 3.

The main drawback of this test arises from the acquisition of a small number of samples per period when the input signal frequency approaches the sampling frequency. This procedure is not, in its present form, suited for the dynamic test of ADCs since the small amplitude of the stimulus signal to use makes difficult the generation of a stimulus signal with sufficiently high slope to approach dynamic conditions.

### III. DYNAMIC TEST – HISTOGRAM METHOD WITH GAUSSIAN NOISE AS STIMULUS SIGNAL

The histogram method is the test procedure usually used to extract the stationary dynamic transfer function of ADCs by comparing the probability density function (*pdf*) of a known stimulus signal with the number of occurrences of each digital code. The most commonly employed stimulus signal is the sinusoid. The use of a deterministic wave present however some problems: (i) the wave statistical properties rely heavily on its magnitude/time trend, being the histogram particularly sensitive to in-phase distortions [14]; (ii) noise inevitably present in any experimental setup distort the signal stimulus *pdf* influencing negatively the test results [13]; (iii) being periodic, the signal and sampling frequencies must be such as to avoid information redundancy.

On the other hand, the use of a statistically defined electrical signal, like Gaussian noise, as the stimulus signal for the histogram test, presents some advantages [15,16]: (i) only the first order statistics are relevant for the characterisation. As always, however, any nonlinearities in the generator will reflect themselves in the converter merit figures; (ii) a noise wave is as easy as or easier to generate than a sine wave, especially when high resolution or high frequency converters are under test; (iii) noise in the test ensemble will only add its variance to the noise of the generator, as long as both possess normal distribution; (iv) an error in the variance of the noise only induces a gain error; (v) noise is not periodic, thus not requiring hard to implement sampling schemes; (vi) white noise in particular presents a uniform power spectral density allowing for a wide-band performance analysis.

Apart from all the referred advantages, the use of Gaussian noise should be considered in those cases where the ADC is expected to acquire signals with *pdfs* similar to those of random noise. It is the case for instance of audio signals. Converters for use in digital radio or on modern digital communication systems should be tested with such a stimulus. It is well know that ADCs exhibits in many cases nonlinearities dependent of the input signal *pdf* as a consequence of localised heating effects in ADC integrated circuits, the use of a sinusoidal wave as input signal for the test, with *pdf* maximums in the input range limits will lead to

different results of those obtained with waves where the *pdf* maximum is localized in the central part of the range.

One of the main directions of work within our research group has been the study of the use of Gaussian noise as the stimulus signal for ADC testing. In this case the transition level  $T[i+1]$ , is given by [15]

$$T[i+1] = \sqrt{2}\sigma_R \operatorname{erf}^{-1}(2CH_i - 1) + \mu_R \quad (4)$$

where  $\sigma_R$  and  $\mu_R$  are the standard deviation and the mean of the noise stimulus,  $CH$  stands for the cumulative histogram and  $\operatorname{erf}$  is the error function.

The standard deviation of the input noise to be used as stimulus signal in this test cannot be arbitrary for two reasons: (i) it must be such as to excite all levels of the converter; (ii) as shown in [15], an optimum value exists that minimises the required number of samples for a given pair of tolerance/confidence ( $\gamma/\xi$ ) levels in the measurement of INL and DNL vectors. In [15] an expression for the number of required samples was derived

$$N \geq \frac{2T[i+1]^2 \left[1 - \operatorname{erf}^2(0.5)\right] \cdot \left[\operatorname{erf}^{-1}\left(\xi^{2^{-n}}\right)\right]^2}{4(\gamma Q)^2 \left[\operatorname{erf}(1) - \operatorname{erf}(0.5)\right]} \quad (5)$$

$Q$  being the average quantization step.

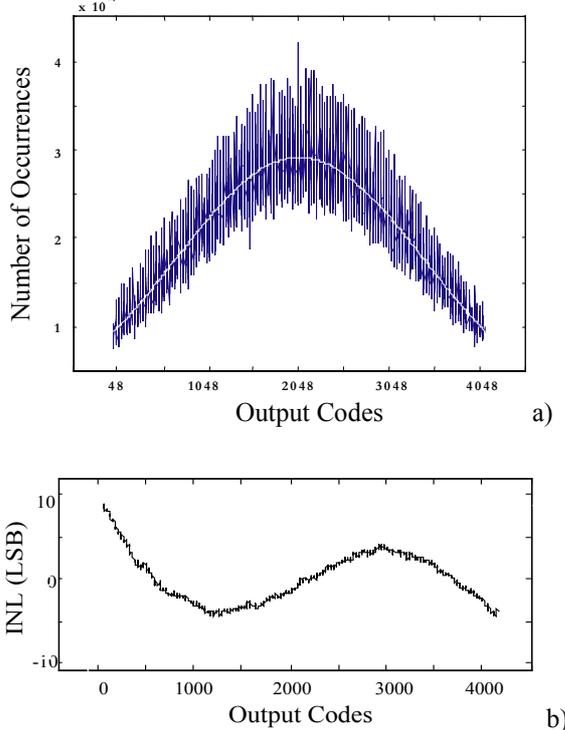


Fig. 5 a) Experimental results of a histogram test stimulated by Gaussian noise for a 12-bit ADC with  $4.16 \times 10^6$  samples. b) Corresponding independently based *INL*.

Caution must be taken in order to avoid device damage by high input signal amplitude when this stimulus signal is used. In fact, due to the nature of normal distributed noise, a high variance implies the existence of a finite probability for the occurrence of potentially damaging levels. Consequently, a limiting circuit must be included (except in the cases where noise is originated in a pseudo-random digital sequence) that does not distort the input signal normal *pdf* within all the input ADC range.

In fig. 5 a) experimental results for a 12 bit ADC, obtained by the histogram test stimulated by Gaussian noise are presented. In fig. 5 b) the corresponding independently based *INL* is shown. By comparing the *INL* values of the traditional histogram test with results of fig. 5 b), one can say that the results of both tests converge when the input signal frequency in the case of a sinusoidal stimulus increases [18]. This is not surprising since white noise is a wide band signal.

To verify the validity of the histogram test stimulate by Gaussian noise intensive numerical simulation was carried out. In [17] results both for ideal and non-ideal simulated ADCs were shown, together with experimental results of an “ideal” actual ADC board.

Figure 6 shows histogram test results of a simulated 8-bit ideal converter and of the most significant 8 bits from a 12-bit board (whose static *INL* was shown in fig. 3) so as to have a real converter with a transfer function as close to the ideal as possible. This allows the comparison of the results of the physical experiment with its simulation. In both tests the same pseudo-random sequence of  $10^6$  samples with Gaussian distribution, was used. In the case of the experimental test, the pseudo-random white Gaussian noise sequence was electrically generated by a Digital to Analog 16-bit board.

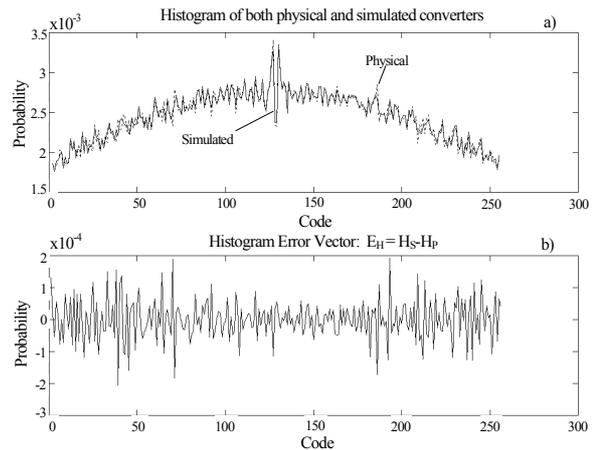


Fig. 6. a) Histograms of both the physical and simulated ideal converters. b) Histogram Error – difference between the two histograms in a).

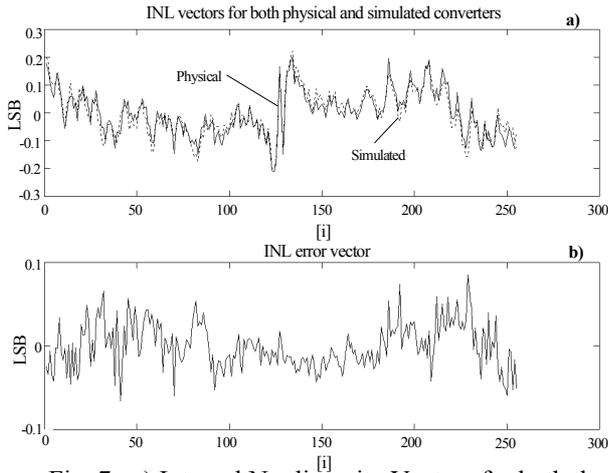


Fig. 7. a) Integral Nonlinearity Vectors for both the physical and simulated converters. b) INL Error Vector – difference between the two.

Experimental results in figures 6 and 7 are actually slightly better than the numerical simulation ones. This should come to no surprise since part of the fluctuations in the simulated histogram originate at the not exactly Gaussian distribution of the pseudo-random sequence and from its finite length where smoothed due to the presence of real Gaussian *pdf* electrical noise in the test ensemble.

#### IV. DYNAMIC TEST – SINE FITTING

Sine fitting algorithms are commonly used in fast dynamic tests of ADCs. Traditionally they are used to measure noise, signal to noise and distortion ratio and ENOB [1,2]. More recently they were proposed to obtain INL, DNL and the transfer function of ADCs, namely when they present a hysteric behavior [19]. These algorithms estimate the parameters of a sine wave,  $A_0\cos(2\pi f_0 t_n) + B_0\sin(2\pi f_0 t_n) + C_0$ , that may fit a set of  $M$  samples,  $y_1, \dots, y_M$ , acquired at a frequency  $f_s = 1/T_s$ .

If the signal frequency is unknown, the four parameter sine fitting algorithm should be used. It seeks solutions of a nonlinear system of equations, which must be solved in an iterative way. From initial estimated values for the frequency and the other three parameters,  $A_0$ ,  $B_0$  and  $C_0$ , the algorithm produces a new set of values  $A_i$ ,  $B_i$ ,  $C_i$  and a correction  $\Delta f_i$  to the frequency to be used in the next iteration. The main problem with this algorithm is that its results are highly dependent on the number of samples and especially on the initial estimated values. Occasionally the algorithm generates corrections to the frequency that lead to erroneous solutions making convergence impossible and this still an open problem. The parameter estimation is exposed to errors due to different causes like small number of samples, small number of samples per period, noise and distortion.

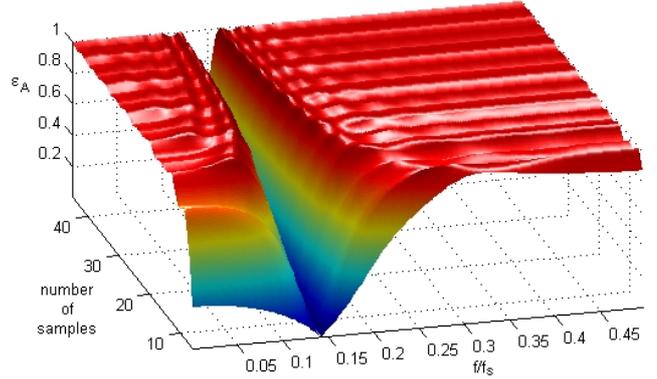


Fig. 8 – Three parameter algorithm error  $\varepsilon_A$  as a function of the number of samples and the estimated frequency, for  $f_0 = 0.14247f_s$ .

An intensive study of the algorithm behavior in different conditions was carried out in order to understand what could be done to increase its performance [20]. Fig.8 shows the results obtained with the three parameter algorithm for the relative error of the amplitude of the estimated ac component,  $\varepsilon_A$ . It can be shown that  $\varepsilon_A$  presents an absolute minimum for the correct frequency value. When the estimated frequency diverts from this value the error increases, reaching the maximum of 100% at approximately a number of samples  $N = f_s / \Delta f_0$ , where  $f_s$  is the sampling frequency and  $\Delta f_0$  is the absolute error on the estimation of the frequency  $f_0$ . From this point, local minimums of  $\varepsilon_A$  are found. Their location depends on the number of samples.

An obvious conclusion of fig.8 is that convergence to local minimums of the error function is less probable for small number of samples given the low derivative of the error function in this region. In [20] a variant of the four parameter algorithm was proposed. In it, the first iterations are computed by considering a small set of all acquired samples. After frequency convergence for the vicinity of its correct value, the number of samples can be increased leading to an accurate estimation of the input signal frequency in the region of high sensitivity (high number of samples) of the curves in fig.8.

#### V. CONCLUSIONS

New static and dynamic analog-to-digital converters testing techniques were revised and discussed.

It was shown that a new technique based on the use of small triangular waves superimposed with a variable offset value that scans all ADC input ranges to built an histogram reduces dramatically the duration of the static test, allowing also the use of lost cost equipment especially when high resolution ADC are under test.

A variant of the traditional histogram test using Gaussian noise as stimulus signal was discussed. It is

especially interesting for high frequency or high resolution ADC test.

A new technique that grants convergence of the traditional four-parameter sine fitting algorithms was revised.

## VI. ACKNOWLEDGEMENTS

This work was sponsored by the Portuguese national research project entitled "New measurement methods in Analog to Digital Converters testing", reference PCTI/ESE/32698/1999, whose support the author gratefully acknowledges.

## VII. REFERENCES

- [1] IEEE Std. 1057-1994 Standard for digitizing waveform records, The Institute of Electrical and Electronics Engineers, Inc., New York, December 1994.
- [2] IEEE 1241-2000 Standard for Analog to Digital Converters, The Institute of Electrical and Electronics Engineers, Inc., New York, 2001.
- [3] Solomon Max, "Optimum Measurement of ADC Code Transitions Using a Feedback Loop", Proceedings of the 16<sup>th</sup> IEEE Instrumentation and Measurement Technology Conference, vol. 3, pp. 1415-1420, May 1999.
- [4] Solomon Max, "Testing High Speed High Accuracy Analog to Digital Converters Embedded in Systems On a Chip", Proceeding of the International Test Conference, pp.763-771, 1999.
- [5] A. Cruz Serra, "New measurement procedure for the static test of ADCs", IEEE Instrumentation and Measurement Technology Conference Proceedings, IMTC/2000, vol. 2, pp. 866-871, Baltimore, USA, May 2000.
- [6] A. Cruz Serra and P. Silva Girão, "Static and Dynamic Testing of A/D Converters Using A VXI Based System", Proceedings of the 1994 IEEE Instrumentation and Measurement Technology Conference, vol. 2, May 1994, pp. 903-906.
- [7] A. Cruz Serra, "Uncertainties in the Estimation of the Code Transition Levels in the Static Test of ADCs", 4<sup>th</sup> Workshop on ADC modeling and Testing, September 1999, pp. 221-226.
- [8] A. Cruz Serra, "A New Measurement Method for the static test of ADCs", Comp. Stand. & Interf., CSI-22, June 2000, pp. 149-156.
- [9] Linus Michaeli, private communication at IMEKO TC4 EUPAS meeting in Trencianske Teplice, April, 1999.
- [10] F. C. Alegria, P. Arpaia, P. Daponte and A. C. Serra, "ADC Histogram Test Using Small-Amplitude Input Waves", Proceedings of the XVI IMEKO World Congress, Austria, September 2000, vol. 10, pp. 9-14.
- [11] F. Alegria, P. Arpaia, P. Daponte, A. Cruz Serra, "An ADC Histogram Test Based on Small-Amplitude Waves", accepted for publication in Measurement, Elsevier Science B. V., in press.
- [12] F. Correa Alegria, Pasquale Arpaia, Pasquale Daponte, A. Cruz Serra, "ADC histogram test by triangular small-waves", IEEE Instrumentation and Measurement Technology Conference Proceedings, IMTC/2001, vol. 3, pp. 1690-1695, Budapest, Hungary, May 2001.
- [13] Jerome Blair, "Histogram Measurement of ADC Nonlinearities", IEEE Trans. on Instr. and Meas., vol. 43, pp. 373-383, June 1994.
- [14] J. Schoukens, "A critical note on histogram testing of data acquisition channels," *IEEE Trans. Instr. Meas.*, vol. 44, pp.860-863, Aug. 1995.
- [15] R. Martins, A. Cruz Serra, "Automated ADC characterization using the histogram test stimulated by Gaussian noise", *IEEE Trans. Instr. Meas.*, vol. 48, pp. 471-474, April, 1999.
- [16] R. Martins, A. Cruz Serra, "ADC characterization by using the histogram test stimulated by Gaussian noise Theory and experimental results ", Measurement, Elsevier Science B. V., vol. 27, pp. 291-300, June, 2000.
- [17] R. Martins, A. Cruz Serra, "The use of a noise stimulus in ADC characterization", IEEE International Conference on Electronics, Circuits and Systems, ICECS'98 Proceedings, vol. 3, pp. 457-460, Lisbon, September, 1998.
- [18] R. Martins, A. Cruz Serra, "Dynamic characterisation of analog to digital converters", Confetele 99, pp. 90-94, Sesimbra, Portugal, April, 1999.
- [19] P. Arpaia, A. Cruz Serra, P. Daponte, Conceição Libano Monteiro, "A Critical Note to IEEE 1057-94 Standard on Hysteretic ADC Dynamic Testing ", IEEE Transactions on Instrumentation and Measurement, vol. 50, n. 4, pp. 941- 948, August, 2001.
- [20] M. Fonseca da Silva, A. Cruz Serra, "Improving convergence of sine fitting algorithms", accepted for publication in Computer Standards & Interfaces, Elsevier Science B. V., in press.