

HIGH-SPEED HIGH-RESOLUTION DATA CONVERTERS FOR BASE STATIONS: TECHNOLOGIES, ARCHITECTURES AND CIRCUIT DESIGN

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ABSTRACT

This paper presents a possible evolution of base station architectures in the frame of the future global communication scenario. Moving from such a view the paper considers the technology trend and its influence on high-speed data converter design. Then, architectures of high-speed, high-resolution converters are resumed. Finally, design techniques and strategies for achieving the requirements of base-station systems are discussed.

1. Introduction

The recent progress in mobile communication mainly depends on two key elements: the DSP and the data converter. New DSP architectures allow complex algorithms to be implemented at a very high computation speed. Analog-digital converters able to match the resolution and the speed of the DSP provide the required interface functions [1]. Because of the evolution in those two sectors the boundary between the analog and the digital world is moving more and more toward the antenna, thus permitting new system architectures to be implemented.

The third generation mobile communications system, *G3*, is expected to provide worldwide access and global roaming for a wide range of services, including multimedia and high-speed data transfer. Predictions say that the *G3* will be a global system, comprising both national terrestrial and satellite components. Through multi-mode multi-band terminals *G3* will extend the coverage for basic services and will permit roaming from a private cordless or a fixed network, into a pico cellular or into a micro cellular public network, toward a wide area macro cellular network and then to a satellite link, in each case with a minimal break in communication (Fig. 1) [2].

The complexity of the communication network requires equipment and basic components which are more and more sophisticated. In particular, the evolving architectures of base stations pose demanding requests to DSP

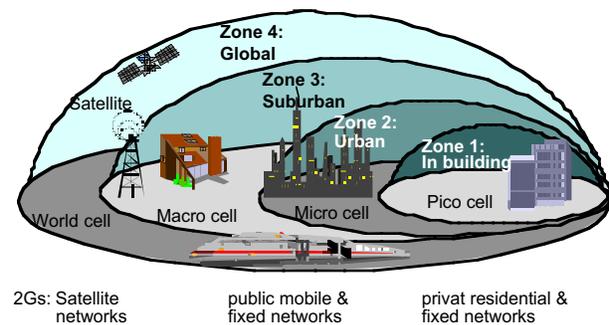


Figure 1. Global coverage of G3 communication systems.

and (relevant for this study) to data converters.

The paper considers before the architecture of a possible future base station and recalls specifications and operative conditions for the required data converters. On that basis technologies, architectures and circuit design techniques are discussed.

2. Communication systems

Existing mobile communication systems ground on the so called *G2 GSM* in Europe and part of America and Asia, *CMDA* in the *USA*. The need to protect investment for the *G2* system requires an enhancement of services through an evolutionary path. Flexible systems overlying the existing *G2* must be introduced before switching to full *G3* standards. Because of this needs future handheld and base stations must be able to perform second and third generation technologies at the same time. This is difficult to obtain with rigid architectures. Flexibility is obtained with transceiver structures software programmable: the so-called “software radio” approach [3].

The software radio concept envisages a base station platform with reconfigurable hardware and software. The architecture can be adapted to different standards or services simply by changing the software. It is evident that software radio offers many advantages: it is flexible,

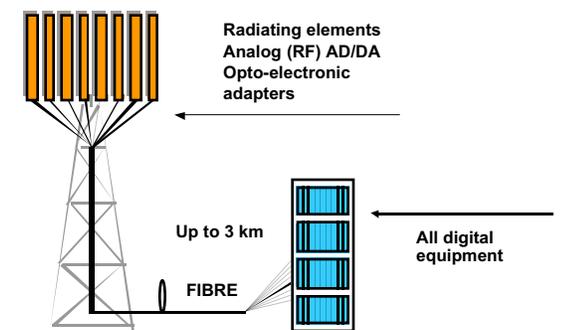


Figure 2. Hypothetical future base-station architecture.

allows new services to be added quickly thus shortening the time-to-market, offers better management of logistics, maintenance and personnel training. Moreover, software radio permits the required migration from one standard to the successive generation along an evolutionary path.

As it is obvious the cellular system implies coverage, capacity and service quality. In macro cells ensuring a proper coverage is pretty expensive; in micro or pico cells the interference from neighbor cells worsens service quality. Smart antennas are the right solutions for both the above mentioned problems. A smart antenna is a directional antenna with an adaptive array architecture used to secure a directional radiation pattern. Several antenna elements are spatially arranged with the signal driving each element suitably processed to attain the required directional feature.

Replacing an unidirectional antenna with a smart antenna not only requires to process and to generate multi-signals but also necessitates to use complex interconnection between electronics and the antenna elements. Since the frequencies involved are in the GHz range and the power to be transmitted is significant, the cost of cables can become a significant fraction of the cost of the base station, especially for micro and pico cells.

The above considerations suggest the hypothetical architecture shown in Fig. 2 [4]. The digital signal is processed into a cabinet at ground level and it is transferred to the

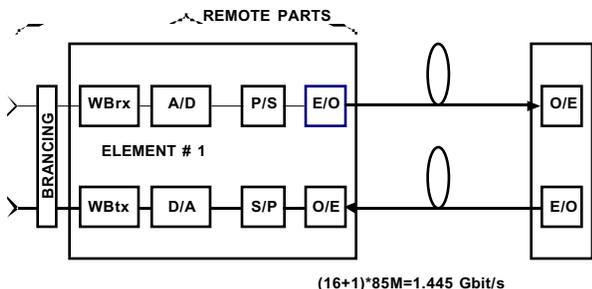


Figure 3. Details of the remote link used in Fig. 2.

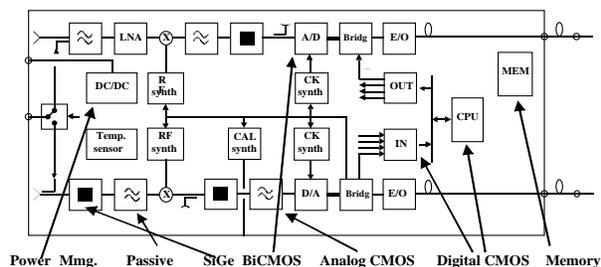


Figure 4. Remote antenna module and needed technologies.

antenna with an optical fiber connection. A serial/parallel converter transforms the high speed bit stream into the data necessary to control data converters. The conversion from digital to analog and the RF section are placed on the antenna tower next to the radiating elements (Fig. 3). Assuming that the data converters resolution is 14-bit and the conversion rate is 85 MHz the data flow (including one extra bit for signaling) is 1.275 Gbps, an affordable value for relatively short optical links. The given data flow rate enables interconnection up to few Km at a relative low cost. Therefore, in a pico-cell environment the same cabinet can accommodate the digital circuits of many smart antennas.

3. Technologies

The present technology evolution is driven by the system-on-chip (SoC) concept. Multiple IP digital cores and analog functions are combined together to implement the operations of an entire system. Therefore, SoC requires the integration of functions that are implemented today in different technologies. Consequently, analog and digital, base-band and high-frequency, low and high power with the addition of memory capabilities must be offered by a single IC technology.

The block diagram of Fig. 4 represents the various functions required by the module of the hypothetical base station of Fig. 2. Observe that the different blocks need a variety of technologies. Those technologies are almost the same that are required by the handheld. However, the driving force for the technology evolution does not come from the base station but from the necessities of the handheld. In fact, the market size of base-stations is a mere fraction of the market size of the handheld. Therefore, the single chip cell-phone objective will drive the technology merging predicted by Fig. 5 [5].

The speed of data converters to be used in base stations and in handheld requires the use of CMOS or BiCMOS sub-micron technologies. However, the accuracy needed in the handheld is more relaxed than the one required by the base-station. Because of this data converters for base

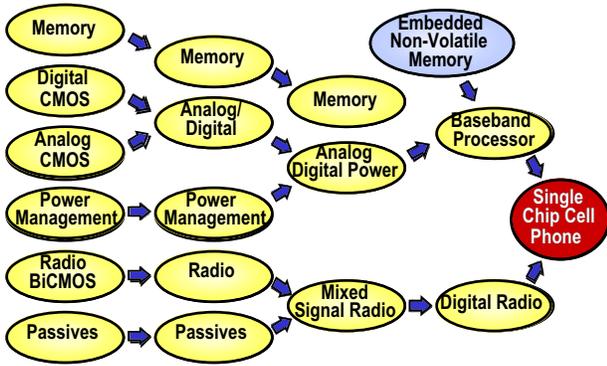


Figure 5. Merging of functions in a single chip.

stations necessitate special *CMOS* or radio *BiCMOS* technologies (with features like trimmable thin-film resistors or trench insulation). It may happen that the roadmap defined by the single chip cell phone can exclude features that are essential for base stations. It is therefore necessary to influence the technology evolution or (more likely) to identify new data converter solutions capable to achieve required performances while using a non-optimum technology.

4. Data Converter Architectures

Table 1 summarizes the critical specifications for *A/D* and *D/A* converters required by modern base station architectures [6]. The number of bits is in the *14-16 bit* range. Moreover, signal band protection imposes a multi-tone image rejections as high as *100 dB* or so.

A/D		D/A	
# of bit	14-16	# of bits	14-16
SFDR to Nyquist	95 dBFS	SFDR to Nyquist	75 dB
Multi-tone IMD Reject.	100-110 dB	Multi-tone IMD Reject.	95 dB
SNR	75-80 dB	SNR	85 dB
Analog Bandwidth	200-250 MHz	Analog Bandwidth	50-100 MHz
		Interpolation	x4 -x8
		clock	> 400 MHz

Table 1 - Critical specifications of *A/D* and *D/A*.

The choice of data-converter architectures depends on a number of design considerations. In addition to the specifications of Table 1, it is necessary to account for power consumption, available technologies and complexity of the calibration method. Nowadays the pipeline solution is the best trade-off for *A/D* requirements; the current steering technique is adequate for the *D/A* specifications.

After identifying the proper data converter architecture it is necessary to choose key parameters of the configuration and to define implementation conditions.

In a pipeline architecture it is necessary to define the bit partitioning along the pipeline stages. Up to *12-bit* the use of *1.5-bit* per stage with digital calibration is an effective solution. However, higher resolutions advise to increase the number of bit per stages (or, at least, to use more bits in the first and, if necessary, in the second stage). This strategy concentrates the need of *DAC* calibration in the very first stages of the architecture. When *4-5 bits* are already determined, the accuracy requirements relax. Therefore, the pipeline cells do not need a very accurate residual *DAC* any more. In general the use of a multi-bit per stage approach implies that:

- The inter-stage gain rises to 2^{N-1} (assuming to use 1 bit for digital calibration).
- The bandwidth requirements for the op-amp increase as the inverse of the feedback factor.

With a *BiCMOS* technology (*0.35 μm* or better) it is possible to obtain op-amp bandwidths in the *2-3 GHz* range. Since the bandwidth limits the product of sampling frequency and inter-state gain, a required conversion rate of *100 MS/s* does not permit inter-gains higher than *8-16*. As a result, three to four bit per stage is an upper limit for the nowadays technologies.

Another relevant architectural issue concerns the choice between switched capacitor [7] or current based schemes [8]. Switched capacitor architecture have shown good capabilities for medium resolution and high-speed. The charge redistribution techniques permits the designer to easily implement the functions required by the pipeline cell. However, for high accuracy and inter-state gains higher than 2, slew-rate requirements and the control needs of MOS switches are additional problems to be solved.

Current mode architectures use current steering *DACs* for the residual generation in each pipeline cell. The use of bipolar transistors procures pretty high speed. Nevertheless, the required accuracy imposes to use thin film resistors (that increases the cost of the technology) and on-chip trimming.

The *DAC* on the transmission path normally uses current steering architectures. *12-bit* have been proved with a sub-micron *CMOS* technology [9]. On the top of that the resolution may increase by one or two additional bits thanks to oversampling. Therefore, the required minimum *14-bit* can be attained. Sub-micron *CMOS* technologies are used for the *DAC*. Future technologies will permit the switching of current source to reach the *GHz* range. Therefore, an high interpolation factors (like *x32*

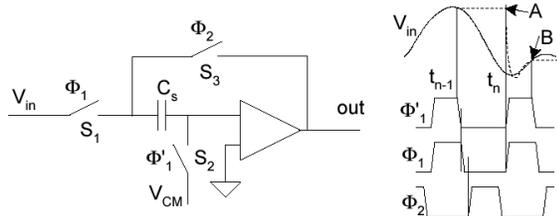


Figure 6. Switched-capacitor base S&H.

or more) will permit the designer to use noise shaping techniques and simplify the *DAC* complexity.

What is specific for base stations is the frequent request of special input processing. In addition to the interpolation communications architectures may require specific filtering features (like a band-pass response). This can be done in the *DSP* section but often it is desired to have the filtering function embedded in the *DAC*.

5. Circuit Design

We already know that the specifications for base-station data converters are very difficult. The designer must use state-of-the-art design techniques, the technology have to provide high spur rejection and the layout needs to ensure almost perfect differential configurations. In this section we recall the critical design issues specific of base-stations data converters.

Sample and Hold

Critical blocks of the pipeline architecture are the input sample-and-hold (*S&H*) and the residual generator of the first pipeline cell. A very important feature is the linearity: any distortion in the *S&H* has negative consequences on the entire converter linearity. For example, the request of *100 dB SFDR* implies third order harmonic coefficients better than *20 ppm*. Therefore, it is necessary to use extremely linear passive components (and hysteresis free) and to perform linear processing when using active components (op-amps).

Fig. 6 shows a typical *MOS S&H* configuration. During the phase 1 the switches S_1 and S_2 sample in a passive way the input voltage. During the phase 2 the switch S_3 connects the sampling capacitor at the output of the op-amp. The linearity of the capacitor does not affect the operation; however:

- Non-linear on-resistance of the switches S_1 causes harmonic distortion. The use of clock boosting techniques capable to keep V_{GS} constant alleviates the limitation. However, since the boosted voltage does not follows perfectly the input signal (especially at high frequency) a residual harmonic contribution can result.

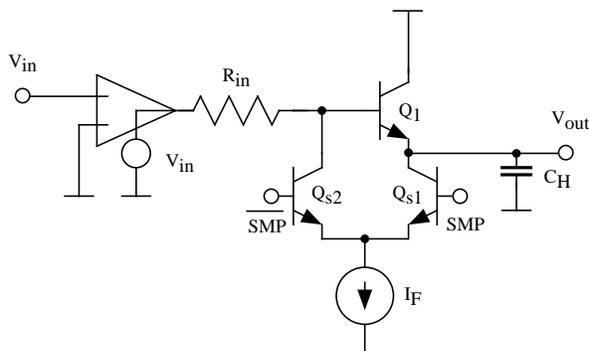


Figure 7. Switched-emitter follower.

- The non-idealities of the op-amp affect the hold phase. Namely, the combination of finite slew rate and finite bandwidth leads to a non-linear dynamic evolution of the output voltage. A limited hold-time does not permit a complete settling bringing on harmonic distortion.
- The finite gain of the op-amp is not constant on the entire output swing. A finite gain produces an error proportional to the inverse of the gain itself. A variation of the gain within the signal amplitude range leads to non-linearity. For *100 dB SFDR* a gain better than *90 dB* over the entire output swing is necessary.

Bipolar solutions don't use feedback. The *S&H* is based on the switched emitter follower concept. It is represented by the scheme of Fig. 7. The circuit achieves a follower action during phase *SMP*. During the complementary phase the switching element Q_{s1} is turned off and the bias current I_F flows trough Q_{s2} . The base voltage of Q_1 is pulled down reverse biasing the base-to-emitter voltage of Q_1 . Therefore, the output node becomes insulated and the circuit switches in the hold mode. The conceptual scheme has been used with pure bipolar [10] and silicon or *Si/Ge BiCMOS* technologies [11], [12].

The availability of complementary vertical *BJT* grants a push-pull version of the switched emitter follower [13]. Fig. 8 shows its basic schematic. Two emitter followers generate a replica of the input signal. One uses an *npn* transistor (Q_1), and the other a *pnp* transistor (Q_2). The cascaded emitter follower Q_3 and Q_4 generate the output voltage. Switching the bias currents determines the transition from the track to the hold mode. The clamp circuit controls the reverse biasing of the Q_3 and Q_4 bases in a way that the charge injected into C_H by the base-to-emitter parasitic capacitances is kept constant. The circuit can achieve more than *95 dB SFDR* with *100 MHz* sampling but the input signal frequency is relatively low.

The limit to linearity of emitter followers comes from the modulation of the base-to-emitter voltage and to the modulation of the base-to-collector voltage. The *kT/C* limit determines the minimum sampling capacitor to be

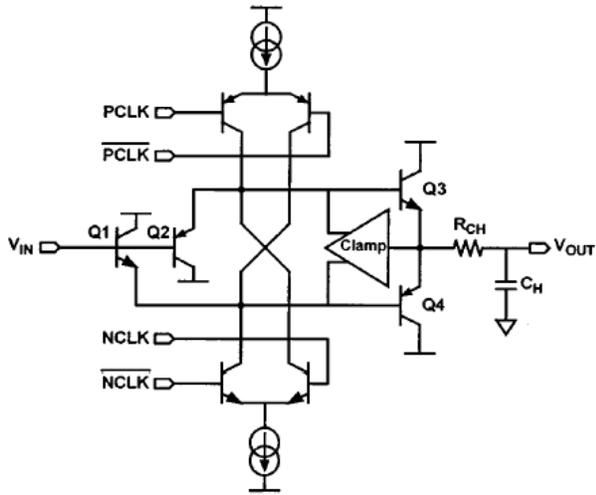


Figure 8. Push-pull switched-emitter follower.

used and, in turn, determines the current in the sampling capacitor during the sampling phase. A change in the emitter current induces a V_{BE} modulation and, consequently, non linearity. With 14-bit of resolution, 100 MS/s, bias currents in the mA range and input frequency equal to 100 MHz the total harmonic distortion cannot be better than 90 dB. Improving the linearity above such a limit is very difficult. It is necessary to compensate for the base-to-collector voltage modulations and other second-order effects [14].

The S&H must exhibit very low jitter. The uncertainties associated with the variations in the period time when the S&H switch opens, or uncertainties associated with time variations in aperture delay determine harmonic distortion if the input signal frequency is high. With a 50 MHz input sine-wave a 14-bit data converter requires an accuracy in the sampling time better than 0.2 ps.

Clock injection

The injection of charge caused by on-off transitions critically affects the linearity and the SNR. Opening a switch (either with switched emitter-followers or MOS switches) produces a charge injection that is non-linearly proportional to the input voltage. This brings about offset and harmonic distortion.

For MOS solutions a fully differential arrangement and opening the switch toward the reference voltage (S_2 in Fig. 6) before opening the switch connected to the input terminal (S_1) permits the designer to obtain more than 90 dB SFDR at low frequency. However, it is necessary to ensure that a limited noise (less than 2-5 mV) corrupts the clock voltage driving the gate of S_2 in the on-state. The sampling of that noise is rejected by the factor $(WL)C_{ox}/C_s$. High speed operation requires very wide

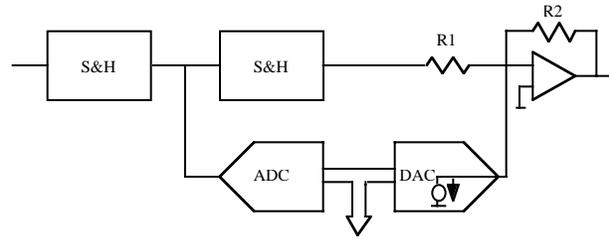


Figure 9. Basic cell of a current-based pipeline

transistors to achieve S_2 so that the attenuation factor can be as large as 0.01.

The charge injection in switched emitter follower cannot be attenuated by the use of the switching-before approach: the sampling capacitor C_H is connected directly to ground. However, as already mentioned, a controlled reverse-biasing of base-to-emitter junctions ensures a constant injection of charge. Observe that the clamp circuit must secure very precise level shifts (better than few mV) over the entire dynamic range of the output signal.

The described CMOS and BJT techniques work well up to 12-bit of resolution. When the required accuracy rises to 14-bit or more many second order effects must be accounted for. Second order effects are difficult to predict because of modeling limitations. It is therefore necessary to intensify the research activity on modelling especially for studying charge injection compensation techniques and for distortion analysis at high frequency.

Noise

An important limit to data converter resolution comes from the noise. It shows up because of the electronic noise of components used and because of the interference between analog and digital sections of the circuit.

The interference term is weakly reduced with circuit techniques: at high frequencies the parasitic coupling between supply lines and nodes of the circuit bypass any circuit protections. Therefore, separate supplies, electrical insulation (permitted by trench separations or SOI technologies) and layout are the only effective defense against the interference noise.

A careful circuit design may bring the electronic noise to its minimum level, kT/C_s (C_s is the sampling capacitance used in the considered stage). The above optimum condition requires that the spectrum of the input referred noise generator equals $4kT$ multiplied by the equivalent resistor limiting (together with the sampling capacitor) the noise band. In turn, it is required that input differential pairs dominate the op-amp noise contributions. Also, when the pipeline cell uses current steering DACs (Fig. 9) the total equivalent noise current generator of the DAC must be negligible with respect to the noise current of the resistance R_1 .

Current-Steering DAC

Current-steering D/A converters are an array of matched current sources that are switched to the output or to a dummy load [15]. The current generators can implement a unary decoded architecture by the use of equal current generators. Every unit source is addressed separately by the digital input code that is converted to a thermometer code. Another option is to use a binary arrangement: every element leads a current to the output that is twice as large as the next least significant bit. The digital input code directly controls the switching.

High-resolution converters use a mixture of the two approaches: the segmented architecture. The *LSB* controls a binary based array while the *MSB* switch single unity current sources. The unary architecture permits to select single generators in a way that compensates for symmetrical and graded errors caused by the temperature, process, and electrical gradients.

The use of a standard CMOS 0.35 μm technology permitted to achieve 10-bit of resolution and 1 GS/s conversion rate [16]. This high conversion rate is more than what is requested by the G3 specification but the resolution is lower. Therefore, the needs of base station ask for a focus on resolution and linearity enhancements.

The mismatch existing between single current sources limits the SNR and is responsible of harmonic distortion. Segment shuffling techniques and dynamic matching elements methods permit the designer to significantly improve the spectral performances. Specific algorithms control the switching of current generators and the spurious energy is redistributed as noise.

A commercial solution provided a 12-bit 400MS/s sampling rate with emitter coupled logic (ECL) compatible I/Os [9]. More recently a 14-bit 400MS/s implementation has been announced [17]. The features of the 14-bit DAC are approaching the severe transmission requirements of the G3 multi-carrier wide-band CDMA (WCDMA) standard. It is therefore expected that the above mentioned DAC will favor experimental tests of advanced G3 base-station architectures.

6. Conclusions

The G3 needs for base-station architectures reflect demanding requirements for data-converters. Presently it is possible to achieve 14-bit 100 MS/s and 90 dB SFDR in A/D converters and to obtain 14-bit 500 MHz in DACs. The third generation mobile communications system uses bandwidths much wider than the ones of G2 standards. Therefore, it is expected that higher conversion rate will be necessary. However, maintaining 14-bit of resolution at higher and higher conversion rates opens

new design problems that can possibly will find solution from a careful study of second order effects and the use of new calibration and digital correction techniques.

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