ACQUISITION SYSTEM WITH LOW JITTER

Ivo Viščor, Josef Halámek

Institute of Scientific Instruments, AS CR
Královopolská 147, 612 64 Brno, Czech Republic
Phone (+42)05 41514305, Fax (+42)05 41514404, E-mail ivovi@isibrno.cz, josef@isibrno.cz

Summary: The high dynamic range system is often limited by the jitter. The sources of the jitter are the clock generator, the clock distribution and the ADC. Two different methods of the ADC jitter measurement are presented.
Keywords: jitter, sources of jitter, measurement.

1. INTRODUCTION

The frequency and dynamic range of the acquisition systems are often limited by the jitter. The jitter originates from both the clock generation and distribution and the aperture uncertainty of the ADC itself. If the system jitter is desired as low as 1 ps, the attention should be paid to the both origins. Such a value means e.g. the analog bandwidth 160 MHz while the Nyquist SNR of 60 dB is preserved.

In our case we solved the acquisition system with the maximal dynamic range and the maximal frequency range which is intended for the NMR spectroscopy. The system is based on the ADC AD6644 (Analog Devices) with exceptional performance (fs 65 MHz, SNR 74 dB). We built two kinds of the digital receivers. In one-channel receiver 'A', the digitised signal from one ADC is processed by two digital-down-converters (DDC) AD6620. In two-channel receiver 'B', the signals from two ADCs are processed separately by two DDC's. The DDC output signals are captured by the fixed point DSP (ADSP-2181) and transferred to the PC through USB (or RS232) interface for the further processing.

In the contribution, we would like to deal with our experience from the jitter measurements. Three parameters can by explored by the measurement:

- The jitter of the generator and clock distribution;
- The jitter of the ADC;
- The overall system jitter.

With the assumption that the jitter processes in the generator and in the ADC are uncorrelated the overall jitter can be calculated: $t_{Jrms}^2 = t_{JG}^2 + t_{JADC}^2$.

The design of the sample clock generator is not covered by this contribution. The important fact is that no logic gates must be used for the clock distribution as long as the overall jitter less than 1 ps is required. The table of the jitter per gate was presented in [1], the lowest jitter per one gate (1 ps rms) is delivered by the 74ACT00 gate.

The effect of jitter is generally described for the harmonic input signal with the amplitude V and the frequency ω_{IN}:

$$v_{IN}(t) = V \sin \omega_{IN} t \qquad (1)$$

The instant slew rate of this signal is:

$$SR(t) = \frac{d\, v_{IN}}{d\, t} = V \omega_{IN} \cos \omega_{IN} t \qquad (2)$$

The effective value of the slew rate is:

$$SR_{rms} = \sqrt{\overline{SR^2}} = \frac{V}{\sqrt{2}} \omega_{IN} \qquad (3)$$

The jitter induced noise voltage is:

$$V_{Jrms} = SR_{rms} \cdot t_{Jrms} = V \sqrt{2} \pi\, f_{IN}\, t_{Jrms} \qquad (4)$$

2. SYSTEM JITTER MEASUREMENT

The theory and practical results of the overall jitter measurements are described in [1], [2]. These measurements are based on the noise detection when both the frequency and the amplitude of the signal source are changed [2]. In our case the noise contribution from jitter is too small in comparison with the noise floor of the signal source (PTS synthetizer). So one frequency was chosen and only the signal amplitude was changed, while the noise floor of the signal source is reduced with a band-pass filter. The frequency chosen is 210 MHz in order to achieve the maximum sensitivity of the measurement. This is a trade-off between the slew rate of the input signal and the slew rate reduction due to ADC frequency response $K_{ADC}(f_{IN})$. The best sensitivity of the measurement is achieved, when the $K_{ADC}(f_{IN}) \cdot f_{IN}$ product is maximized.
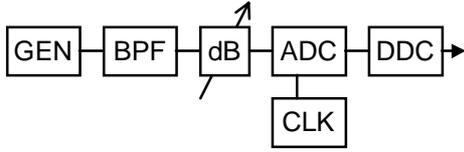
Fig.1.: Block diagram of the system jitter measurement. GEN- signal generator, BPF- band pass filter, dB- variable attenuator, CLK- clock generator.

The noise voltage $v(t)$ *is* measured at 60 frequency bands selected from the ADC Nyquist band by the DDC:

$$v(t) = v_{NADC}(t) + v_{JADC}(t) + v_{JG}(t) \qquad (5)$$

This simple model is based on the the ADC intrinsic noise $v_{NADC}(t)$, the noise induced by the jitter of the ADC $v_{JADC}(t)$ and the noise induced by the jitter of the clock generator $v_{JG}(t)$. Assuming that these noise voltages are uncorrelated, the standard deviation of $v(t)$ is:

$$\overline{v^2} = \overline{v_{NADC}}^2 + \overline{v_{JADC}}^2 + \overline{v_{JG}}^2 \qquad (6)$$

The standard deviation of the noise is measured as a function of the input signal amplitude V square regulated by an attenuator (see Fig.1):

$$\overline{v^2} = F(V^2) \qquad (7)$$

There are two jitter calculations possible: the two-point and the multi-point approach.
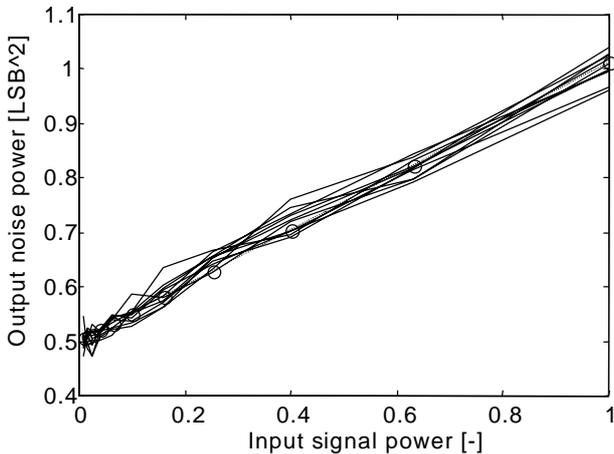

Fig.2.: The noise measured at 10 frequency bands.

The first uses the noise power under two conditions: the full-scale signal and sufficiently low signal. The second is based on a polynomial approximation of the noise power, where the independent variable is the input signal power (7). The first-order coefficient is related to the jitter while the

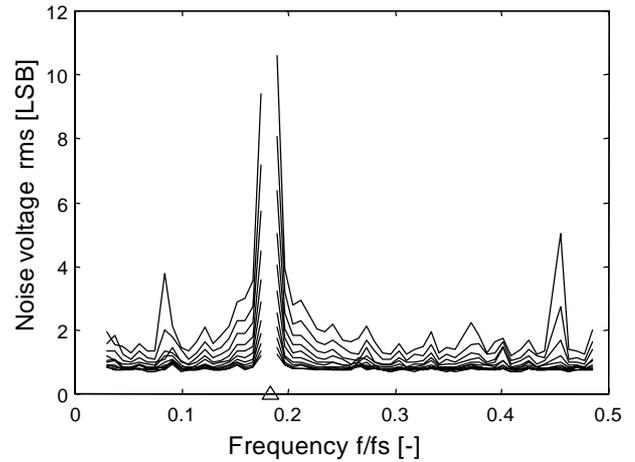zero-order coefficient represents the ADC intrinsic noise v_{NADC}^2.

Fig.3.: The noise voltage measured as a function of the frequency band and input signal amplitude. ∆- the frequency of the undersampled input signal (210 MHz).
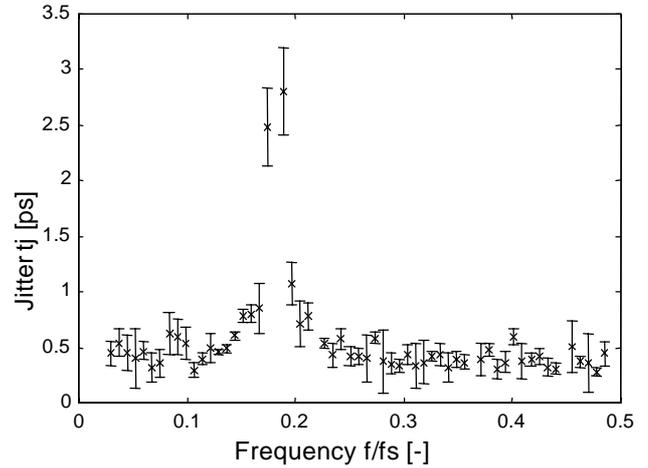

Fig.4.: The measured system jitter as a function of tuned frequency and the standard deviation of the results for different amplitudes of the input signal.
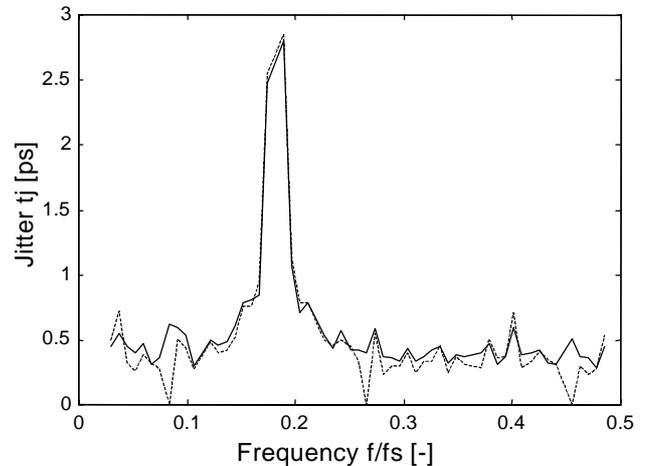

Fig.5.: The comparison of different computation; dotted line- the two-point approach, solid line- the approximation approach.

Both approaches result in our case in the same value 0.21 (0.33) ps for the receiver A (B) (Tab.1, Fig.5). The presented value is the mean value of the results from 10 selected bands with the lowest noise. This results to the elimination of the irregularities due to the harmonics and spurious distortion and the insufficient carrier suppression by the DDC in the adjacent bands (Fig.3). Note that the noise measured in DDC output bandwidth (in our case 0.5 MHz) should be recalculated for the whole Nyquist bandwidth.

3. ADC JITTER MEASUREMENT

Once we want to measure just the jitter of ADC, the influence of the clock signal jitter must be eliminated. The test method is described in the draft of IEEE standard [3], nevertheless, the method is still dependent on the quality of clock signal and digital-to-analog coupling. The accuracy of the measurement is limited by the maximal sampling frequency, which is the same as of the input signal. In our case the frequency is 66 MHz. The optimal frequency of the analog input signal would be 210 MHz for the best sensitivity as mentioned above. A generation of the input signal by a multiplier or divider is mentioned in the clause 4.10.3.1 [2]. Unfortunately such an active component would introduce the jitter grater than 1 ps and this cannot be eliminated at all.
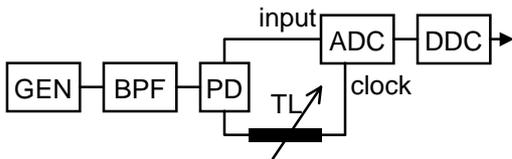

Fig.6.: Block diagram of the ADC jitter measurement. GEN- signal generator, BPF- band pass filter, PD- power divider, TL- variable transmission line.

We measured the ADC jitter in the receiver A for two different clock sources: the low jitter clock unit (the same unit was used for the system jitter) and the PTS synthetizer (jitter about 20 ps). Our measurement follows the test method described in [3]. In addition, three cables of different length are inserted at the analog input in order to phase the signal. Each active edge of the clock is sampling itself at the phase between 0° and 90° depending on the cable, so the instant slew rate (2) from a maximum down to zero is achieved.

The noise is measured as a function of the input signal phase under the full-scale condition. The noise due to jitter contribution is maximal when the phase is 0°. When the phase is 90° the jitter influence is eliminated and the intrinsic noise of the ADC is measured. This differs from the approach described in the draft of IEEE standard [2], which is based on the intrinsic noise measurement under zero input signal conditions. In our case the ADC jitter measured is 0.11 and 0.46 ps respectively, depending on the clock source. When the zero input approach is used the jitter is 0.29 and 0.53 ps respectively. So the jitter of the clock source is not eliminated entirely.

4. 2-ADC METHOD

Another method for the clock generator jitter elimination takes advantage of our receiver B with two synchronous ADC's. The idea is that if the both ADC's receive the same input and clock signals, than the both ADC outputs contain the same noise contribution induced by the jitter of the clock generator. The stringent assumption of the same clock signal is fulfilled in our case, because the clock distribution is passive and balanced.
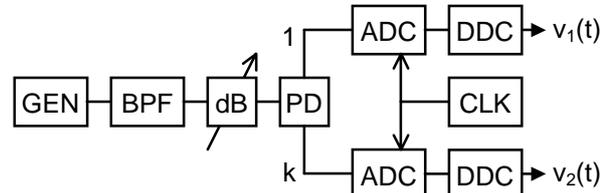

Fig.7.: Block diagram of 2-ADC method. GEN- signal generator, BPF- band pass filter, dB- variable attenuator, PD- power divider, CLK- clock generator.

Let's the complex constant $k = A \cdot e^{i\varphi}$ represents the input signal unbalance of the power divider and the ADC. The measured mean power of the noise in channel 1,2 is:

$$\overline{v_1^2} = \overline{v_{NADC1}^2} + \overline{v_{JADC1}^2} + \overline{v_{JG}^2}$$
$$\overline{v_2^2} = \overline{v_{NADC2}^2} + A^2\left(\overline{v_{JADC2}^2} + \overline{v_{JG}^2}\right) \quad (8)$$

In addition, the sum and the difference of the channels is explored:

$$v_P(t) = v_1(t) + v_2(t)$$
$$v_M(t) = v_1(t) - v_2(t) \quad (9)$$

And the mean power of the sum and the difference is measured:

$$\overline{v_P^2} = \overline{v_{NADC1}^2} + \overline{v_{NADC2}^2} + \overline{v_{JADC1}^2} + A^2 \cdot \overline{v_{JADC2}^2} +$$
$$+ 2 \cdot \left| 1 + A\cos\varphi \right| \cdot \overline{v_{JG}^2}$$

$$\overline{v_M^2} = \overline{v_{NADC1}^2} + \overline{v_{NADC2}^2} + \overline{v_{JADC1}^2} + A^2 \cdot \overline{v_{JADC2}^2} +$$
$$+ 2 \cdot \left| 1 - A\cos\varphi \right| \cdot \overline{v_{JG}^2}$$

$$(10)$$

The noise induced by the jitter of the clock generator can be simply evaluated from the equation (10). Further, the noise in both channels (8) can be corrected for the clock jitter contribution. Finally, the jitter of the clock generator and jitters of the both ADC's can be evaluated by the method for the system jitter measurement described in the section 2.

If the clock generator jitter is sufficiently low in comparison to the ADC jitter $t_{JG} << t_{JADC} / \sqrt{|1 - A\cos\varphi|}$, the evaluations can be further simplified ($A\cos\varphi = 1$). In our case, the measured channel balance is $A = 1.02$; $\cos\varphi = 0,994$. The values measured by this method are shown in Table 1. The dynamic range in the table is directly computed from the measured intrinsic noise of the ADC - v_{NADC}.

	Jitter [ps]				DR [dBFS/√Hz]	
method	2-point		Approx.		2-point	approx
receiver	avg	std	avg	std		
A, ch#1, total	0.21	0.01	0.21	0.04	150	150
B, ch#1, total	0.33	0.02	0.33	0.12	150	149
B, ch#2, total	0.30	0.02	0.30	0.13	150	150
B, clock generator	0.18	0.02	0.19	0.11	-	-
B, ch#1, corrected	0.28	0.02	0.27	0.10	150	150
B, ch#2, corrected	0.24	0.02	0.23	0.11	150	151

Tab.1.: The measured jitter and the dynamic range of the receiver A and B, channels 1,2. System jitter (total), generator jitter, ADC jitter (total jitter corrected for clock generator contribution), average results (avg) and standard deviation of results (std) across 10 frequency bands.

5. CONCLUSION

If the system jitter bellow 1 ps is required, the clock source should be perfect, the active components should be avoided for the clock distribution and the clock distribution should be properly impedance matched. Also the digital-to-analog coupling should be minimized.

The overall system jitter is important for users. The measurement is simple, its sensitivity is good and can be optimized (the maximum of $K_{ADC}(f_{IN}) \cdot f_{IN}$ product).

The ADC jitter is important for the system developers and for the producers. The sensitivity of the measurement [2] is limited by the maximal sampling frequency, which is the same for analog input signal. If the ADC jitter is bellow 1 ps, also the clock source should be sufficiently good despite the IEEE test method considerably eliminates the influence of clock source jitter. Anyway, the measured jitter is in good relation to the datasheet value of 0.2 ps (typical).

The 2-ADC method should be further explored with a high jitter clock generator. The ability of the method to suppress the clock generator jitter contribution will be investigated in future measurements.

REFRENCES

[1] B. Brannon, "Aperture Uncertainty and ADC System Performance", *Analog Devices, AN-501,* 1998.

[2] J. Halámek, M. Kasal, M. Villa, P. Cofrancesco, "Reproducibility of Jitter Measurement", *Proceedings of IMEKO 2000,* Wien, Austria, 2000, pp.153-157.

[3] *IEEE Std 1241 DRAFT:* Version 050699, (May 1999) "Standard for Terminology and Test Methods for Analog-to-Digital Converters".

[4] P. Cauvet, "Improving the Dynamic Measurements of ADC's using the 3-ADC Method", *Proceedings of 4th workshop on ADC Modelling and Testing,* Bordeaux, France, 1999, pp. 178-181.