A 6-b 1Gsample/s SiGe BiCMOS A/D Converter

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Summary

The paper describes the design of a 1GS/s 6-bit ADC in SiGe BiCMOS technology. Several techniques such as subranging, interpolation and averaging were implemented on the original flash architecture in order to achieve low power consumption without sacrificing linearity and dynamic performance.

Keywords: Analog to Digital (A/D) converter, Averaging, SiGe BiCMOS.

1.Introduction

Very high-speed A/D converters are widely used in hard disk read channels, high-speed Ethernet transceivers and satellite receivers. For such applications a resolution of 6-b at a sampling speed of 1GS/s or higher is usually required. In literature some CMOS implementations are reported, featuring a sampling speed between 0.8 and 1.6-GS/s and power consumption between 300 and 500mW [1,2,3,4]. Those ADCs usually exhibit limited analog bandwidth and a severe degradation of the effective resolution when the input signal approaches the Nyquist frequency. Bipolar implementations usually feature high power consumption, not suitable for battery powered applications. Flash architecture is the best suited for operation in the GHz range, but it requires high power consumption and silicon area. This paper describes the design of a 1GS/s 6-b ADC in a 0.8µm SiGe BiCMOS technology. This ADC implements subranging, interpolation and averaging for achieving high sampling speed and low power consumption at the same time. Moreover, a differential input section allows the use of low supply voltage (3.0 V) with a 0.5 V dynamic range, while a novel error correction technique limits the degradation of the resolution at high input frequencies.

2.Proposed architecture

Fig. 1 shows the block diagram of the proposed ADC which is based on the flash architecture with the addition of several techniques. A conventional N-bit flash architecture would require 2^N-1 comparators. This would lead to an excessive power and area consumption. In order to reduce the total number of comparator, a subranging technique was implemented by means of two Track-and-Holds (THA) and two ADCs operating in parallel. The coarse ADC (ADC1) is a latch comparator that features polarity detection and provides the sign of the input signal (Vin) to the 5-bit ADC and to the digital output. Indeed, the output of ADC1 controls a polarity reverser in the input section of the fine, 5-b, ADC (ADC5). This circuit provides the absolute value of the ADC input signal to the fine flash-ADC, which therefore requires only $2^{N/2}$-1 comparators, with savings in terms of power consumption and area. Even if this is a well-known A/D conversion technique, it is hard to be implemented in very fast ADCs operating in the GHz frequency range. The input THAs are fully differential and based on the open-loop switched emitter follower architecture, leading to high bandwidth, low power consumption and limited linearity degradation at high input frequency.

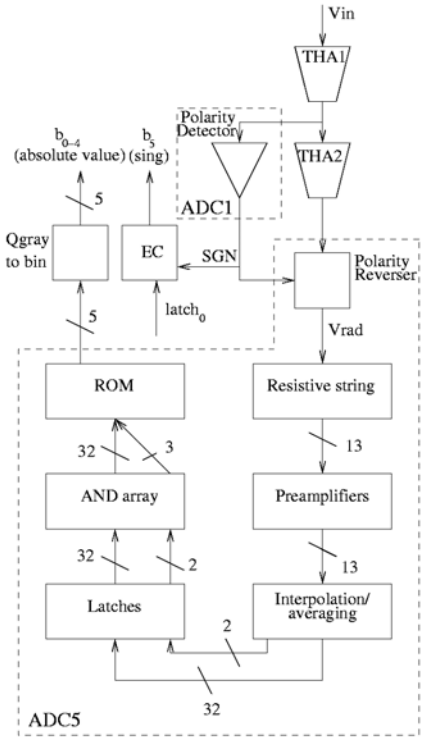

Fig. 1. ADC block diagram

Using two THAs in series relaxes the dynamic performance required to the coarse ADC and to the input section of the fine ADC, since the latter process an input signal which is held constant over a conversion half-period. In order to achieve differential conversion, the input section of the fine ADC is based on a couple of dynamic reference resistive strings [5]. The original differential input adapter implemented with npn-BJTs driving the head of the strings cannot be directly used in the proposed ADC since the THA provides a differential signal with a low common-mode voltage. Moreover, it should be noted that up-level shifter implemented with pMOS transistors are not suitable for processing high frequency signals. The problem is overcome by providing the input signal to the tail of the resistive strings through the differential pair Q1-Q2, Q2 being diode connected, Fig. 2. Two current generators are used for biasing the adapter. Since the tail generator forces a current which is two times the current of the generator in the head, the voltage at the collector of Q2, i.e. the tail of the resistive string at the left of Fig. 2, follows the positive input voltage, Vin+.

Each output of the pair of the resistive strings is equal to the ADC differential input voltage minus a threshold voltage equal to nV_t. In a conventional flash architecture V_t is equal to the LSB voltage. The differential outputs of the resistive strings are processed by an array of amplifiers in order to attenuate the impact of the offset voltage of the latched comparators on the ADC linearity.

High-speed rectification of the input signal is achieved by modifying the circuits driving the tail of each resistive string as shown in Fig. 3. Depending on the output of the 1-b ADC (SGN bit) the tail current $2I_0$ is steered to the Q1-Q2 pair or to the Q3-Q4 pair.

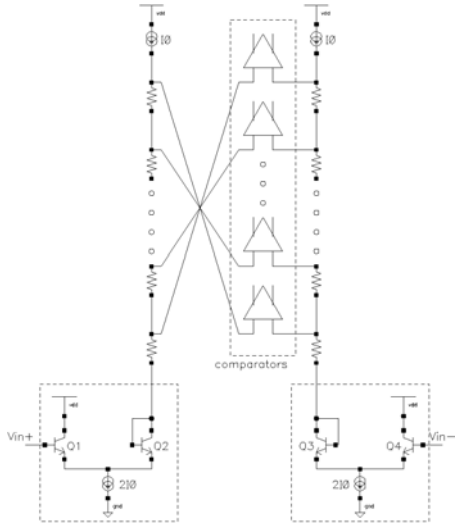

Fig. 2. Differential resistive string

Let us assume that the input signal is negative, thus the SGN bit is low and Q6 is biased while Q5 is turned off. Therefore, all the tail current flows through the Q3-Q4 pair and it is equally split between the two transistors, because of the current source at the head of the resistive string.

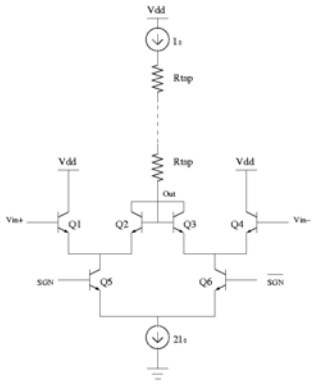

Fig. 3. Polarity reverer: single circuit

Since Q3 and Q4 are identically biased, the negative input signal, Vin-, is fed to the tail of the resistive string. At the same time, the opposite situation occurs in the other resistive string, driven by an identical circuit, but with swapped SGN inputs (Vin+ and Vin-); then the positive input signal Vin+ is provided to its tail. This obviously leads to a rectification of the sampled ADC input signal.

In order to further reduce both the power consumption and the silicon area, 4x interpolation was implemented. It consists in removing three comparators out of four and replacing them with four identical resistors connected in series, $R_a/4$, between the outputs pin of every couple of adjacent amplifiers, Fig. 4. The signals at the intermediate nodes are approximately the same that would by provided by the removed amplifiers:

$V_{i+1}=¾V_i+¼V_{i+4}$
$V_{i+2}=½(V_i+V_{i+4})$
$V_{i+3}=¼V_i+¾V_{i+4}$

This assumption holds for voltage close to the thresholds of the removed amplifiers if the LSB is relatively small whit respect to the linear range of each amplifier. This technique allows to reduce the number of comparators by a factor of 4, thus if used together with the subranging technique the amplifiers are only 1/8 with respect a conventional flash ADC.

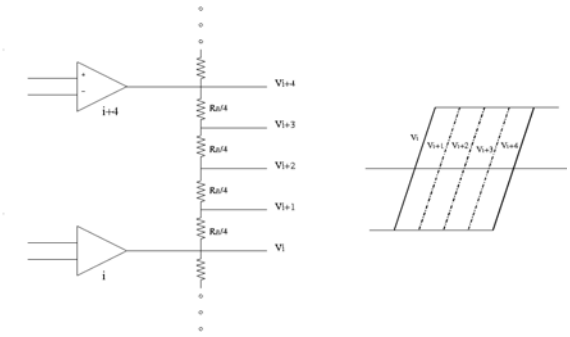

Fig. 4. Interpolation/Averaging resistors

An averaging system was also implemented. It can be proven [6] that the insertion of a resistor between the outputs pin of every couple of adjacent comparators attenuates the effect of the amplifiers offset voltage on the DNL and INL errors, because of a weighted averaging effect between the outputs of several adjacent amplifiers. In the present circuit a single resistive network is used for both averaging and interpolation in order to save chip area. Thus in Fig. 4 the averaging resistance is R_a: the sum of the values of the four resistors $R_a/4$. Two dummy amplifiers were added at each end of the amplifiers array for reducing non-linearity error at both end of the conversion characteristic. The averaging resistance makes the output of each amplifier dependent on the one of the neighbors, thus reducing the converter's non-linearity.

After the averaging-interpolation stage, the 32 resulting signal are digitized by a series of two latch-comparators. Two latches are necessary to reduce the metastability occurrence probability below 10^{-9}. The resulting thermometer code is converted to Quasi-Gray code by an array of differential AND gates and a ROM. Quasi-Gray code was chosen because of its robustness against bubble and sparkle code occurrence, comparable to that of the conventional Gray code. Whit respect to Gray code it allows easier conversion to binary code, which is realized by simple EX-OR cells.

3.Error Correction

Sampling skew and settling errors may lead to a discrepancy between the SGN bit (output of the 1-b ADC) and the polarity of the signal at the output of S/H2. To circumvent this problem, an error correction technique was implemented. The SGN bit correction is activated whenever the polarity of the signal Vrad (Fig. 1), at the output of the polarity reverser, is negative. This happens when the output of Latch0, corresponding to the threshold voltage at 0V, is low. In this case the polarity reverser has failed to rectify the input signal, and the fine ADC is not suitable to process the negative signal provided to its input. In order to properly handle this situation, the conversion range of the fine ADC is extended by adding some threshold voltages, and related comparators, below the 0V threshold. These additional thresholds are obtained by interpolation between the lowest useful comparator and the adjacent dummy one, previously introduced to lower the averaging-induced non-linearity errors.

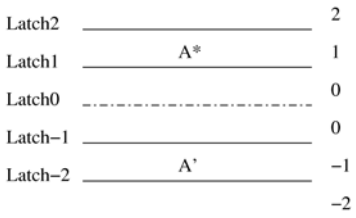

Fig. 5. Error correction example

The situation is explained in Fig. 5 where the horizontal lines represent the threshold voltage of the comparators, the numbers on the right represent the absolute value at output. If a negative signal A' whit amplitude between -2 and -1 LSB occurs at the output of the polarity reverser, the output of the $latch_0$ is low (therefore an error is detected) as for the $latch_{-1}$, while the output of the $latch_{-2}$ is high. This 1-0 transition is detected by the AND gates array and, consequently, the row of the ROM corresponding to the threshold at +1 LSB is activated (Fig. 6); this recovers the error affecting the output of the 5-b ADC (b_0-b_4) since the correct level of the signal would be A^*, between +1 LSB and +2 LSB.

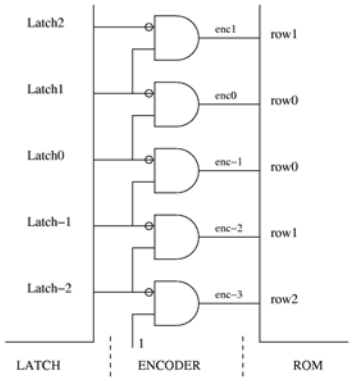

Fig. 6. Error correction circuit for absolute value

The SGN signal is corrected on the base of the truth table reported in Tab.1 where b_5 is the sign bit at the output of the complete converter.

SGN	Latch0	b_5
0	0	1
0	1	0
1	0	0
1	1	1

Tab. 1. Truth table used for correcting the sign bit (b5)

A simple negative exclusive OR implements this correction. The effect of error correction is shown in figures 7-8. The input signal is a 488.281MHz sine wave sampled at 1GS/s. Figure 7 shows the sampled values (top) without the error correction system and the corresponding residuals returned by the time-domain analysis. Note that for sample values close to zero the corresponding error is large (up to 5 LSB), as graphically highlighted in the figure. If the error correction is enabled (Figure 8) the residuals are lowered within +1 LSB.

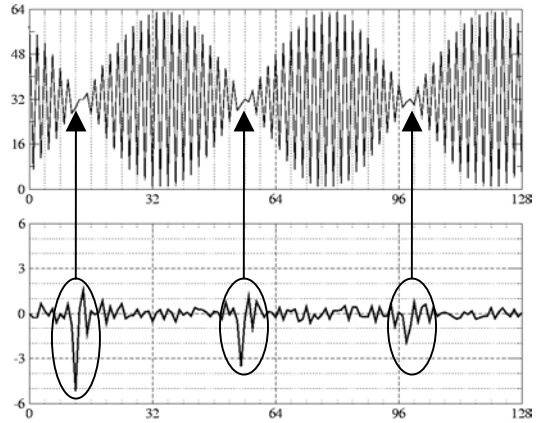

Fig. 7. ADC output (top) and residuals (bottom) (noise+distortion) without error correction

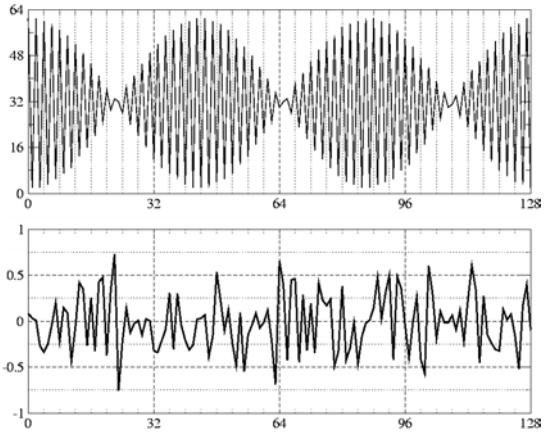

Fig. 8. ADC output (top) and residuals (bottom) (noise+distortion) with error correction

4.Specifications

The simulated static power dissipation is 450mW (close to the reported values for similar CMOS converters in literature). If redesigned in a 0.35µm SiGe BiCMOS technology, the power consumption would be reduced by about 40%, keeping the same overall dynamic performance. Extensive Montecarlo simulations were used to estimate INL and DNL, which are both below one LSB.
The converter's specifications are reported in the following Tab. 2:

Supply voltage	3V
Sampling frequency	1Gsample/s
Maximum input amplitude (peak-to-peak)	600mV
Static power dissipation	450mW
Total harmonic distortion (THD)	-38dB
Effective number of bits (ENOB)	5.55
Maximum integral non-linearity (INL)	0.79 LSB
Maximum differential non-linearity (DNL)	0.30 LSB

Tab. 2. Specifications of the converter

5.Acknowledgment

The authors would like to thanks Prof. C.Morandi of University of Parma for the fruitful discussions.

6.References

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