CANCELLATION OF CHARGE INJECTION ERROR ON SWITCHED CURRENT DIVIDER CIRCUITS FOR ACCURATE D/A CONVERTERS.

E.GARNIER, A. TETELIN and Ph.MARCHEGAY.

Laboratoire IXL – C.N.R.S. UMR 5818 – E.N.S.E.I.R.B
Université Bordeaux I
351, cours de la libération – 33405 Talence – France
Tél : 33 (0)5 56 84 26 32 – Fax : 33 (0)5 56 37 15 45
E mail : mailto:garnier@enseirb.fr

Abstract

This paper proposes compensated methods to cancel the effects of charge injection error on switched-current Divider Circuits. Algorithmic structures of current dividers are presented and the final charge injection error is evaluated for each Algorithm. So, compensated methods to cancel this error are proposed.

I.- INTRODUCTION

As more progress of very large scale integration (VLSI) technology has been made, many mixed-signal integrated circuits have been implemented on a single chip. “Low-voltage/low power circuit” design like Digital to Analog Converters (DAC’s) is strongly needed for both analog to digital circuits to increase operation time and to decrease occupied die area and consumption [1].

With SI (switched-current) technique the same low-cost digital CMOS process for the digital portion of mixed signal circuits can also be used for the analog part [2].

When current is used as the active parameter, the need of matched signals implies a need for matched currents. Typically though, matched currents are generated using current mirrors which depend on good device matching [3], [4]. To avoid this device parameter dependence, alternative copying sequence to resolve the matching problem of the basic divider are used which are algorithmic structures [5], [6], [7].

Many authors proposed different structures as Robert and al. divider [5], Wey and Krishman structure [6] and Wang and Wey circuit [7]. But the accuracy of these dividers is limited by clock feedthrough error effects.

So this paper presents the evolution of charge injection error on switched-current divider circuits and proposes, for each structure, adapted compensated methods to minimize this error and to obtain a greater accuracy.

At first, in the second section, the different structures of algorithmic S.I divider circuits are analyzed. In the next section, the clock feedthrough error (CFT) effects and the evolution of CFT error, for each Algorithmic structure, is analyzed. Section 4, compensated methods are proposed. Finally, a conclusion is given in section 5.

II.- CURRENT DIVIDER CIRCUITS.

The principle of current division is often used in SI D/A conversion. Such conversion generally requires many successive divisions by two which must be very accurate.

So the use of Algorithmic dividers by two allows to achieve a very high accuracy [8], [9]. Robert and al [5] proposed the first algorithmic current divider which is shown in figure 1.

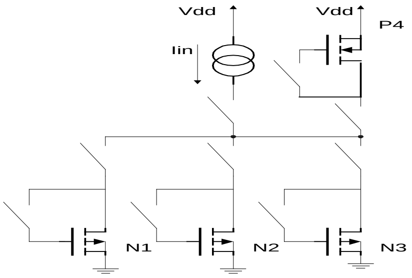

Fig-1: basic Algorithmic current divider.

The number of iterations necessary to obtain half the current with certain accuracy depends on the mismatch of transistors N_2 and N_3. Each iteration takes three clock cycles, as illustrated below.

First iteration: a- $I_{in} \rightarrow N_2$ and N_3
b- $N_2 \rightarrow P_4$
c- P_4 and $N_3 \rightarrow N_1$

Other iterations: a- I_{in} and $N_1 \rightarrow N_2$ and N_3
b- $N_2 \rightarrow P_4$
c- P_4 and $N_3 \rightarrow N_1$

If α_2 and α_3 are the mismatch factors of the transistors N_2 and N_3, respectively, the mismatch ratio γ is equal to $((\alpha_3/\alpha_2)-1)$, $I_2 = \alpha_2 I_{in}$ and $I_3 = \alpha_3 I_{in}$.

According to the current copying sequence, the current held in N_3 at the end of the first cycle of the k-th iteration, I_{3k}, is expressed as [6].

$$I_{3k} = \frac{Iin}{2}\left[1+(-1)^{k-1}\left(\frac{\gamma}{2+\gamma}\right)^{k}\right] \quad (1)$$

The error due to mismatch decreases rapidly as k increases and authors [5] show that an accuracy of 0.1% can be achieved by taking only three iterations for γ = 20%.

But the NMOS copier proposed stores only a positive current, hence the divider functions properly only when $I_2 > I_3$.

Because the transistor mismatch is generally unknown in advance, this structure could be used, only with biased S.I cells. An alternative structure with the same algorithm was proposed by Wey and al.[6] where the NMOS copier has been replaced by a CMOS stage as illustrated in figure 2

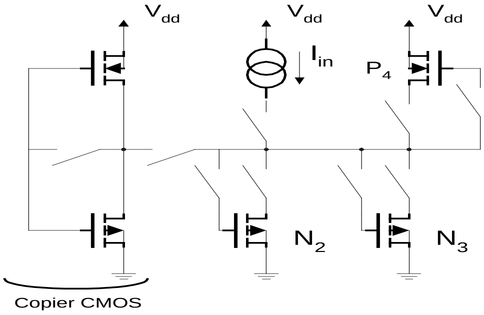

Fig-2: CMOS Algorithmic current divider.

So, N_2, N_3 and P_4 stages can be unbiased cells.To eliminate the CMOS stage Wang and al. [7] proposed a new structure realized entirely with unbiased cells (figure 3).

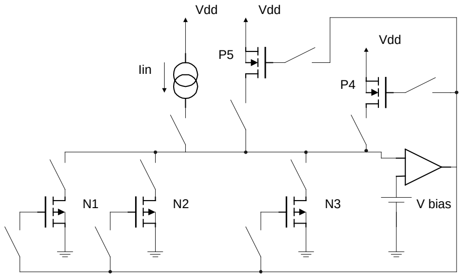

Fig-3: Wang and al. divider.

The copying sequences between N_2 and N_3 are then illustrated below:

First iteration: a- $I_{in} \rightarrow N_1$
b- $N_1 \rightarrow P_4$
c- $N_1 \rightarrow P_5$

Others iterations: a- $P_4 \rightarrow N_2$ and N_3
b- P_5 and $N_3 \rightarrow N_1$
c- N_1 and $N_2 \rightarrow P_4$

The current is held in N_1 during the first cycle from the third iteration.
This structure presents a lower occupied area than the other structures and a very low power consumption, to the detriment of a more complex digital part.

So with a lower occupied die area and a more complex copying sequence, it is possible to obtain a very accurate current divider by two almost insensitive to the mismatch.

III.– CFT ERROR ON SWITCHED-CURRENT DIVIDERS.

In current matching circuits there are two primary sources of systematic errors, the transistor's finite output resistance r_0 and charge injection from switches [10].

To increase r_0, cascoded devices or a single long-channel device can be used.
The second source of systematic error is associated with the charge injection from the MOS switches [11], [12], [9], [10].

It is interesting to know the evolution of the CFT error during each iteration of the various structures in order to propose the most adapted method to compensate it. To validate the study of the effects of CFT error, simulations under cadence environment with CMOS 0.6 µm AMS technology were done.
The cells (biased or unbiased) used for these simulations have a cascoded stage associated to the hold transistor to increase r_0 and no hold capacitor is added in order that CFT error is sufficient. Therefore its effects are more obvious.
In current matching circuits, charge injection produces an error voltage δ_v on the gate capacitors of memory transistors which leads to an error current δ_I in the memorizing transistors.

By neglecting the second and higher order terms, the error δ_I may be written as [15]:

$$\delta I_n = \delta I_{ndc} + \delta I_{nac} \quad (2)$$

with $\delta I_{ndc} = kn\frac{w}{L}\left(mV_{T_n}+b\right)^2+\sqrt{k_n\frac{w}{L}*I_b}*\left[2\left(mV_{T_n}+b\right)\right]$ (3)

and $\delta I_{nac} = I_{in}*2m+\sqrt{k_n\frac{w}{L}*I_b}*\left[2\left(mV_{T_n}+b\right)\right]*\frac{\frac{I_{in}}{Ib}}{2}$ (4)

Where $K_n = \frac{\mu nCox}{2}$, m and b are constant dependent on layout, processing and switching waveforms, V_{Tn} is the threshold voltage of each of the n-channel devices, $\frac{w}{L}$ is the NMOS transistor's sizes, δI_{nac} is the signal dependent error, δI_{ndc} the signal independent error, I_b and I_{in} the biased current and the input current respectively.
In a similar manner, an input current I_{in} in the p-channel device will lead to a current error of:

$$\delta I_p = \delta I_{pdc} + \delta I_{pac} \quad (5)$$

- If the basic algorithmic divider is considered, the current error at the end of the k-th iteration during the second cycle is:

$$(\delta I_{N3})_k = \left(\frac{\delta I_{pac}}{2}\right) + \left(\frac{\delta I_{pdc}}{2}\right) - \left(\frac{\delta I_{ndc}}{2}\right) - \delta I_{nac} \qquad (6)$$

To achieve a good cancellation of the signal independent charge injection error, the current matching approach relies on matching between n-channel and p-channel devices.

As $\delta I_{pdc} = \delta I_{ndc} \pm \varepsilon_1$, $\delta I_{pac} = \delta I_{nac} \pm \varepsilon_2$,

$\varepsilon_1 < \delta I_{pdc}$ and $\varepsilon 2 < \delta I_{pac}$.

Finally: $$(\delta I_{N3})_k \cong \pm\left(\frac{\varepsilon_1}{2} + \frac{\varepsilon_2}{2}\right) - \frac{\delta I_{nac}}{2} \qquad (7)$$

So a basic algorithmic current divider is quite insensitive to the signal independent error like the algorithmic multiplier [10].
Simulations show that the current error [tab 1] after the first iteration is of the order of 1% of $\frac{Iin}{2}$ if classical biased S.I cells are used.

I_{in} µA	$(I_{N3})_1$ µA	$(I_{N3})_2$ µA	$(I_{N3})_3$ µA
20	6.9	10.28	10.28
40	16.82	20.2	20.2

-Tab 1- I_{N3} during the second cycle of each iteration with basic cells

- For the algorithmic current divider with CMOS stage, the last current error is equal to:

$$(\delta I_{N3})_k = \left(\frac{\delta I_{dcCMOS}}{2}\right) \pm \left(\frac{\varepsilon_2}{2}\right) - \left(\frac{\delta I_{nac}}{2}\right) \qquad (8)$$

The greatest part of this error comes from the CMOS stage (Tab 2-a).

	I_{in} µA	$(I_{N3})_1$ µA	$(I_{N3})_2$ µA	$(I_{N3})_3$ µA	
(a)	40	19.61	21.73	21.73	Without added capacitors to the CMOS stage.
(b)	40	19.61	19.83	19.83	With added capacitors of 1pF.

-Tab 2- I_{N3} during the second cycle without added capacitors for unbiased cells

Thus, to cancel the charge injection error two compensated methods must be implemented, one for the CMOS stage as the add of capacitors (Tab 2-b) and one for unbiased cells.

- For the last structure, it is more interesting to keep the output current on the transistor N_1 during the first cycle. The current error after the second iteration is equal to: $(\delta I_{N1})_3 = \delta I_{nac} - \delta I_{pac}$ (9)

And this error becomes for the other iterations:

$(\delta I_{N1})_k = \left(\frac{\delta I_{nac}}{2}\right)$ (10) with $k > 3$

Tab 3- resumes the results obtained for this divider with the same cells that those used for the previous divider.

I_{in} µA	$(I_{N1})_3$ µA	$(I_{N1})_4$ µA
40	19.29	19.825

-Tab 3- I_{N1} during the first cycle of each iteration

IV.– ADAPTED COMPENSATED METHODS.

So, to achieve a very good accuracy, in SI technique, adapted compensated methods must be implemented for each structure of Algorithmic dividers.

- For the basic algorithmic, the use of cells which compensate the signal dependant error as multisampling techniques (S^2I Cells) will allow to obtain a very good accuracy.

  The current error , after the first iteration with these cells, is constant and independent of the input current (Tab. 4- b). It has been reduced by a factor four and it is easier to compensate it because it is constant [16].

	I_{in} µA	$(I_{N3})_1$ µA	$(I_{N3})_2$ µA	$(I_{N3})_3$ µA	
(a)	20	6.9	10.28	10.28	Classical Cells
(b)	20	12.96	10.06	10.06	S^2I Cells.
(c)	20	10.44	10.01	10.01	Class AB S^2I Cells

-Tab 4- I_{N3} during the second cycle of each iteration with basic cells(a), S^2I cells(b), class AB S^2I cells(c).

The use of class AB cells (Tab 4- c) allows to decrease the power consumption with a very high accuracy.

So, a low power and a very accurate divider by two is obtained.

- For the algorithmic current divider with CMOS stage, the add of capacitors allows to decrease the CFT error of unbiased cells.

For the CMOS stage, the use of CMOS switch (Tab. 5-b) or a dummy circuit (Tab. 5- c) allows to decrease significantly the resultant error.

	I_{in} µA	$(I_{N3})_1$ µA	$(I_{N3})_2$ µA	$(I_{N3})_3$ µA	
(a)	40	19.61	21.73	21.73	Without added capacitors to the CMOS stage.
(b)	40	19.61	19.80	19.80	With CMOS switch for the CMOS stage.
(c)	40	19.61	19.77	19.77	With a dummy circuit.

-Tab 5- I_{N3} during the second cycle without added capacitors for unbiased cells

So, it is possible to achieve quite the same accuracy that the previous divider with a lower power consumption and a lower occupied die area than the basic algorithmic divider to the detriment of maximum frequency running due to the add of capacitors.

- For the third structure, it is necessary to add capacitors to decrease the CFT final error.

  The occupied die area and the power consumption of this divider by two are very low, but the digital part is more complex and the maximum frequency running is very low.

V.- CONCLUSION

Three structures of algorithmic dividers are considered.

First, the final current error of each structure is evaluated. And it is demonstrated that this error is different for each of divider.
Then, adapted compensated methods are proposed for each structure, like:

- The use of class AB S^2I cells for the basic algorithmic divider.
- The add of capacitors for unbiased cells and the use of dummy circuit for the CMOS stage for the second algorithmic divider.
- The add of capacitors for the last structure.

These proposed methods can degrade the speed performance of these dividers by two and consequently, with more occupied die area, the basic algorithmic divider which uses S^2I class AB cells has the greatest accuracy and the best maximum frequency with still a low power consumption.

REFERENCES.

[1] A.Matsuzawa, "Low–Voltage and Low–Power Circuit Design for Mixed Analog/Digital Systems in Portable Equipment", IEEE journal of Solid–State Circuits – Vol 29, N°4, April 1994.

[2] T.S.Fiez, Member IEEE, G.Liang, Member IEEE and D.J.Allstot, Senior Member IEEE, "Switched-Current Circuit Design Issues", IEEE journal of Solid-State Circuits – Vol 26, N°3, March 1991.

[3] P.Riffaud-Desgreys, E.Garnier, Ph.Roux, Ph.Marchegay, "New Structure of Algorithmic DAC in Switched-Current technique", International IEE Conference on Advanced A/D and D/A Conversion Techniques and their Applications - Glasgow 1999.

[4] P.Riffaud-Desgreys, E.Garnier, Ph.Roux, M..Loulou and J.Tomas, "A Switched-Current Algorithmic D/A Converter", 2nd Int. Workshop on Design of Mixed-mode Integrated Circuits and Applications - 1998.

[5] J.Robert, P.Deval, G.Weymann, "Very Accurate Current Divider", Electronics Letters - Vol 25, N°14, 6th July 1989.

[6] C.L.Wey and S.Krishman, "Current Mode Divide by two Circuit", Electronics Letters - Vol 28, N°9, 23rd April 1992.

[7] J.S.Wang and C.L.Wey, "Accurate CMOS Switched-Current Divider Circuits", IEEE – 1998.

[8] J.S.Wang and C.L.Wey, « High Speed CMOS Switched-Current D/A Converters for Low Power / Low Voltage Signal Processing Applications", - 1998.

[9] S.Wang, B.B.Bhattacharya and M.O. Ahmad, "A Novel Ratio-Independent Cyclic Multiplication D/A Converter", IEEE Int. Symposium on CAS - 1992.

[10] D.G.Nairm and C.A.T. Salama, Fellow IEEE, "A Ratio-Independent Algorithmic Analog to Digital Converter Combining Current Mode and Dynamic Techniques", IEEE Transactions on Circuits and Systems - Vol 37, N°3, March 1990.

[11] W.B.Wilson, student Member IEEE, H.Z.Massoud Member IEEE, E.J.Swanson, Member IEEE, R.T.George, Jr. Member IEEE and R.B.Fair, Senior Member IEEE, "Measurement and Modeling of Charge Feedthrough in n-channel MOS Analog Switches", IEEE journal of Solid-State Circuits – Vol SC-20, N°6, December 1985.

[12] G.Wegmann, student Member IEEE, E.A.Vittoz, Senior Member IEEE and F.Rahali, "Charge Injection in Analog MOS Switches", IEEE journal of Solid-State Circuits – Vol SC-22, N°6, December 1987.

[13] W.Groeneveld, H.Schouwenaars, H.Termeer, "A Self Calibration Technique for Monolithic high-Resolution D/A Converters", IEEE Int. Solid-State Circuits Conference – ISSCC 89.

[14] G.A.S.Machado, N.C.Battersby and C.Toumazou, "On the Development of Analogue Sampled-Data Signal Processing", Analog Integrated and Signal Processing – 1997.

[15] E. Garnier, PH. Roux and PH. Marchegay, "Effects of Charge Injection Error on Switched Current Divider Circuits", ELECO 2001 – International Conference on Electrical and Electronics Engineering.- 7 – 11 November 2001 – Bursa – Turkey.

[16] C.K.Tse and M.H.L.Chow, "A New Clock-Feedthrough Cancellation Method for Second Generation Switched-Current Circuits", IEEE ISCAS – Vol 3, pp2104-2107, May 1995.