Modified Σ-Δ Voltage to Frequency Converter

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Summary: Voltage to frequency converter (VFC) is an oscillator whose frequency is linearly proportional to control voltage. There are two common VFC architectures: the current steering multivibrator and the charge-balance VFC. For higher linearity, the charge-balancing method is preferred. The charge balanced VFC may be made in asynchronous or synchronous (clocked) forms. The synchronous charge balanced VFC or "sigma delta" (Σ-Δ) VFC is used when output pulses are synchronized to a clock. The charge balance VFC is more complex, more demanding in its supply voltage and current requirements, and more accurate. It is capable of 16 to 18 bit linearity.

Σ-Δ modulator can be used for synchronous VFC (SVFC). The synchronous behaviour is good in many applications, but the output of SVFC is not a pure tone (plus harmonics) like a conventional VFC, but it contains components harmonically related to the clock frequency. The SVFC produces a change in probability density of output pulses N and $N+1$ clock cycles after the previous output pulse.

In this paper, the modified SVFC (MSVFC) is described. This MSVFC works similarly as conventional SVFC but it has a pure tone on output (for constant input voltage). Therefore, it is possible to measure the period of MSVFC output (this does not work for SVFC).

Keywords: Voltage to frequency converter, charge balanced, sigma delta modulator.

1. Introduction

In recent years, VFC have become quite popular due to their low cost and application versatility in variety of electronic control and measurement systems. With a good quality VFC, this circuit will match the performance of many commercial A/D converters. Its only disadvantage is relatively slow conversion time. Σ-Δ modulator [1] can be used for SVFC. The block diagram of the Σ-Δ VFC is shown on Figure 1.
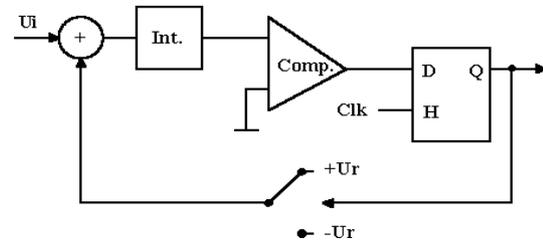

Figure 1. Σ-Δ voltage to frequency converter. Int. - integrator, Comp. - comparator, U_i - input voltage, U_R - reference voltage, D - flip flop

In SVFC charge balance pulse length is now defined by two successive edges of the external clock. If this clock has low jitter the charge will be defined very accurately. The output pulse will also be synchronous with the clock. SVFCs of this type are capable of up to 18-bit linearity and they have excellent temperature stability [2], but is not pure tone for constant input voltage. Figure 2 shows the waveforms of the Σ-Δ SVFC.
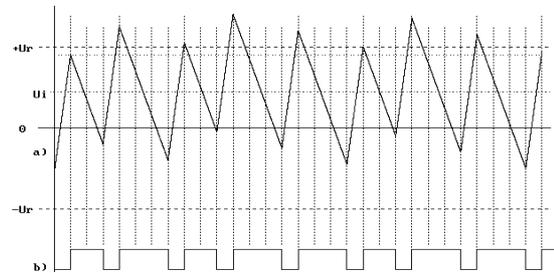

Figure 2. Waveforms of Σ-Δ SVFC. a) integrator output, b) comparator output, input voltage $U_i = 1.8$ V, reference voltage $U_R = 4$ V.

From Fig. 2 can be seen, that output periods are not the same, but they changed between 3 and 4 clock cycles. This disadvantage was taken away in MSVFC.

2. Modified synchronous VFC

In Figure 3 is modified Σ-Δ SVFC block diagram. Only one-shot is added and connected to
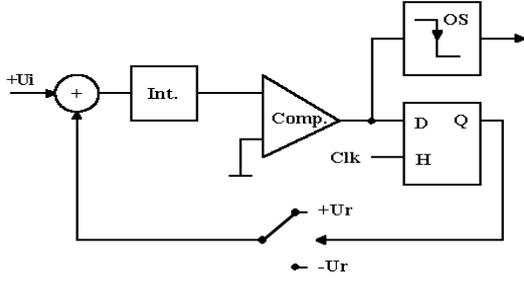
comparator output.

Figure 3. Modified Σ-Δ voltage to frequency
converter. Int. - integrator, Comp. - comparator,
U_i - input voltage, U_R - reference voltage,
D - flip flop, OS - one shot

Figure 4 shows waveforms of this modified Σ-Δ
SVFC. Number of pulses is same for Σ-Δ SVFC
and modified Σ-Δ SVFC, but for modified Σ-Δ
SVFC the frequency is linearly proportional to a
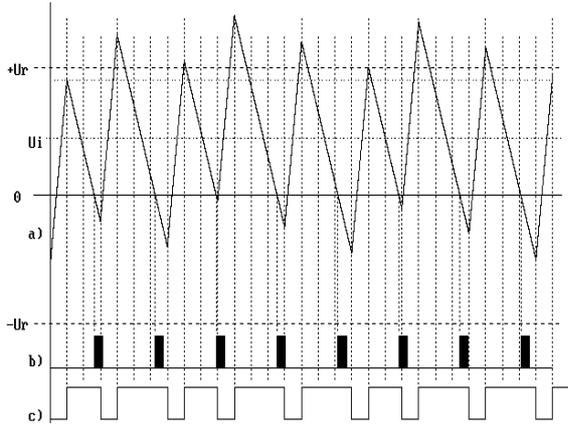control voltage (input voltage must be offset in
converter![2]).

Figure 4. Waveforms of modified Σ-Δ SVFC.
a) integrator output, b) one shot output,
c) D-flip flop output. $U_i = 1.8$ V, $U_R = 4$ V,
period of one shot is 3.636 * period of clock

The output frequency f_O (without offset of
input voltage) is given by (1):
$$f_O = f_{CLK} \left(1 - U_i / U_R \right) / 2 \qquad [\text{Hz, V}] \qquad (1)$$
where U_i is input voltage, U_R is reference voltage
and f_{CLK} is clock frequency.
If $U_i = U_R - U_{ii}$, then
$$f_O = 0.5 f_{CLK} \left(U_{ii} / U_R \right) \qquad [\text{Hz, V}] \qquad (2)$$

where U_{ii} is input voltage with offset.

3. MSVFC output frequency evaluation

The key to Σ-Δ modulator is the integrator. At
each conversion, the integrator keeps a running
total of its previous output and its current input.
The output from the integrator is feed to 1-bit
analog/digital converter (ADC). This is simply a
comparator with its reference input at a level of
half the input range, 0 V in this case. The ADC
output feeds a 1-bit digital/analog converter (DAC)
which has output levels equal $+U_R$ or $-U_R$. A
summing amplifier completes the loop by
summing the current input signal and the previous
sample DAC output. The aim of the feedback loop
is to try to maintain the average output of the
integrator at the comparator reference level, 0 V.
Therefore:

$$\sum_{k=1}^{\infty} U_{o1}(k) + \sum_{k=1}^{\infty} U_{o2}(k) = 0 \qquad (3)$$

where $k = 1, 2,....\infty$, and $U_{o1}(k)$ and $U_{o2}(k)$ are
integrator output voltage in k-th output frequency
period, see Fig. 5.
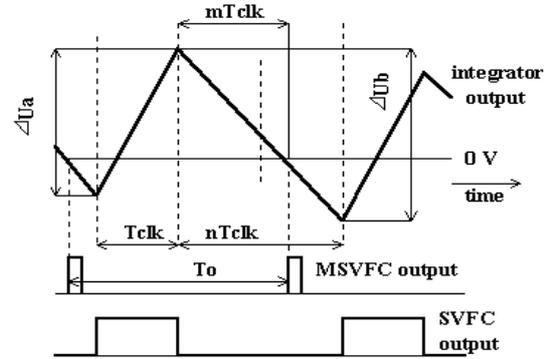

Figure 5. Detailed waveforms of the integrator,
D flip-flop SVFC and one shot MSVFC
outputs, $n=2$ in this figure $(nT_{clk}= 2T_{clk})$.

Change ΔU_a is given by (4):
$$\Delta U_a = C \int_0^{T_{clk}} (U_i(t) + U_R)dt \qquad (4)$$

and ΔU_b is given by (5):
$$\Delta U_b = C \int_0^{nT_{clk}} (U_i(t) - U_R)dt \qquad (5)$$

where C is the integrator constant. The integrator output is given by:

$$U_{o1}(k) = U_{o2}(k-1) + C \int_0^{T_{clk}} (U_i(t) + U_R)dt \qquad (6)$$

$$U_{o2}(k) = U_{o1}(k-1) + C \int_0^{nT_{clk}} (U_i(t) - U_R)dt \qquad (7)$$

and for $U_i(t) = U_i$:

$$U_{o1}(k) = U_{o2}(k-1) + C(U_i + U_R)T_{clk} \qquad (8)$$

$$U_{o2}(k) = U_{o1}(k-1) + C(U_i - U_R)nT_{clk} \qquad (9)$$

Average output of the integrator is 0 V, therefore:

$$C(U_i + U_R)T_{clk} = C(U_i - U_R)nT_{clk} \qquad (10)$$

where n must be an integer for SVFC. For MSVFC output is given by:

$$C(U_i + U_R)T_{clk} = C(U_i - U_R)mT_{clk} \qquad (11)$$

where m is real for MSVFC. From (11) $(U_R > U_i)$:

$$m = \frac{U_i + U_R}{U_R - U_i} \qquad (12)$$

for SVFC, n is given by (13):

$$n = ceil\left(\frac{U_i + U_R}{U_R - U_i}\right) = ceil(m) \qquad (13)$$

where Ceil(.) - Converts a numeric value to an integer by returning the smallest integer greater than or equal to its argument. E.g. Ceil(9/3)=3, Ceil(9.01/3) =4.

Output period for MSVFC is given by (14):

$$T_o = T_{clk} + mT_{clk} = T_{clk}(1+m) = 2T_{clk}U_R/(U_R - U_i) \qquad (14)$$

and MSVFC output frequency is:

$$f_o = 1/T_o = f_{clk}(U_R - U_i)/2U_R \qquad (15)$$

If U_i is offset $U_i = U_R - U_{ii}$, then:

$$f_o = 1/T_o = 0.5f_{clk} U_{ii}/U_R \qquad (16)$$

From (15) and (16) is shown, that MSVFC output frequency is linearly dependent on input voltage (f_{clk} and U_R are constants).

4. SVFC output frequency evaluation

For long time, number of output pulses MSVFC and SVFC are the same, but for SVFC if m (12) is not the integer, the SVFC produces a change in probability density of output pulses N and $N+1$ clock cycles after the previous output pulse. Average period (and average frequency) is the same for MSVFC and SVFC:

$$T_{oSVFC} = (rT_P + sT_Q)/(r + s) = T_{oMSVFC} = T_o \qquad (17)$$

where T_{oSVFC} is SVFC output period and T_{oMSVFC} is MSVFC output period, r is number of periods which value are T_P, s is number of periods which value are T_Q. It is important to note that T_P and T_Q difference is only one T_{clk}, therefore:

$$T_Q = T_P + T_{clk} \qquad (18)$$

From (14) and (17) r and s can be computed.
Example: Consider $U_R = 10$ V, $U_i = 1$ V and $T_{clk} = 1$. Output period from (14) is:

$$T_o = 20/(10-1) = 20/9 = 2.2222$$

Because T_o is not the integer, the output period SVFC will be $T_P = 2$ and $T_Q = 3$. From (17) r and s can be obtained as:

$$\frac{20}{9} = \frac{2r + 3s}{r + s}$$

$2r + 3s = 20$, $r + s = 9$. Numerical solution of linear equations is $r=7$, $s=2$. This solution says, that for 9 output periods, 7 periods will have value 2 and 2 periods will have value 3. This is periodically repeated. It is important to note that MSVFC will have all output period exact 2.2222!

This solution is important for variance of frequency computing etc. Worst case is, when the fractional part of $T_o=0.5$.

5. Experimental results

SVFC AD7741 and AD7742 [2] were tested and MSVFC was realized and simulated.
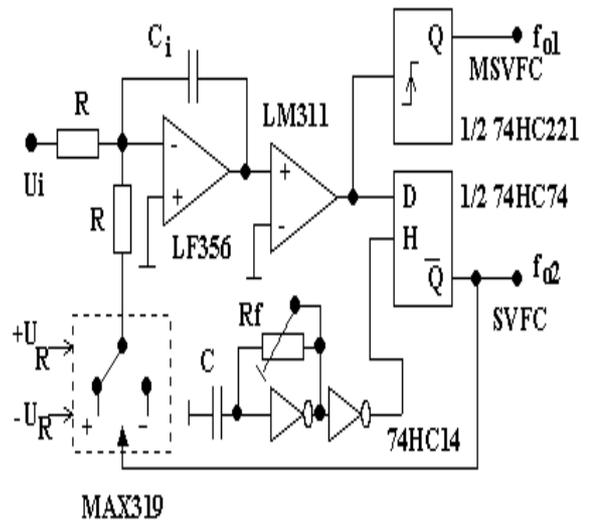

Figure 6. Experimental MSVFC simplified circuit diagram.

Simulation was performed at the block diagram level of Figure 1 and 3. The simulation program was also developed. The MSVFC was realized and simulation results and measured results were compared. In Fig. 6., experimental realized MSVFC is shown [3]. In Fig. 7, graph of measured voltage/frequency characteristic of experimental MSVFC is shown. In Tab. 1, some measured values U_i a f_o are displayed.
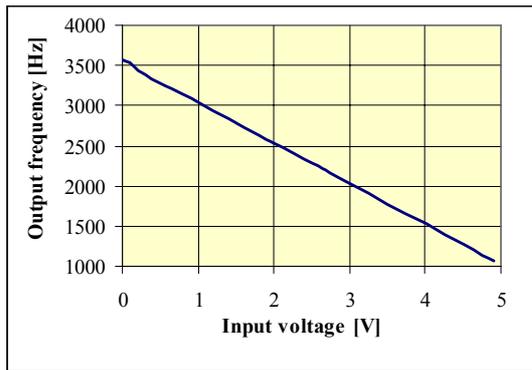

Fig. 7. Graph of voltage/frequency characteristic of realized experimental MSVFC.

U_i	0	0.1	0.4995	1.0122	1.1966
f_o	3570	3533	3288	3033	2939

U_i	1.4069	1.6046	2.014	2.507	3.01
f_o	2836	2734	2529	2279	2025

Table 1. Some measured values U_i a f_o of realized experimental MSVFC, (U_i [V], f_o [Hz]).

In Fig. 8, the oscilloscope photograph shows the integrator output and D-flip flop output of SVFC. In Fig. 9, the oscilloscope photograph shows also integrator output and one shot output of MSVFC.

6. Conclusion

Analysis, simulation and prototype of new type voltage to frequency converter were described in this paper. It was pointed out that this new converter has better properties than other synchronous types of VFC.

In common type of SVFC, since the output pulses are synchronized to a clock they are not equally spaced but have substantial jitter. This need not affect the user of a SVFC for A/D conversion, but it does prevent its use as a precision oscillator. Despite this disadvantage the improvement in performance makes the SVFC ideal for the majority of high-resolution VFC applications.

This main disadvantage of SVFC described above was removed in new type of modified SVFC.
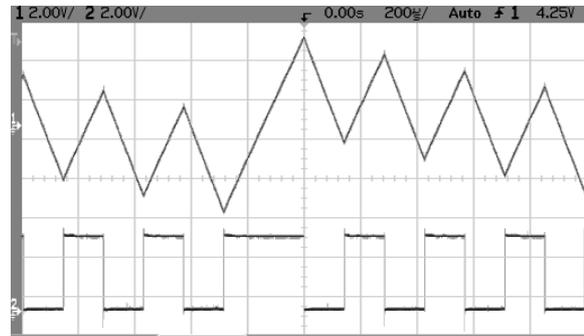

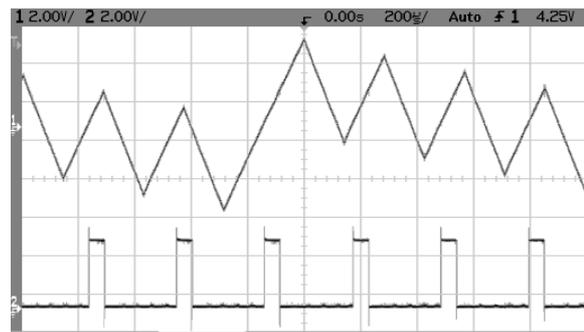Fig.8. The oscilloscope photograph of the integrator and D-flip flop output of SVFC.

Fig.9. The oscilloscope photograph of the integrator and one shot output of MSVFC.

References

[1] Sangil Park, Ph. D.: Principles of Sigma-Delta Modulation for Analog-to-Digital Converters, Motorola Application Notes APR8, 1999.
[2] Single and Multichannel, Synchronous Voltage-to-Frequency Converters, AD7741, AD7742, Analog Devices 1999.
[3] Analog Multiplexers/Switches, Maxim 1995 New Releases Data Book, Vol. IV.