ANALYSIS AND DESIGN OF A 4th ORDER BANDPASS SIGMA DELTA MODULATOR FOR GSM COMMUNICATIONS STANDARD.

J.J. Ocampo Hidalgo, A. Garcia Ortiz, L. D. Kabulepa, and M. Glesner.
Institute of Microelectronic Systems. Darmstadt University of Technology.
Karlstrasse 15 D-64283 Darmstadt. Germany.
Tel: +49 6151 16 49 39 Fax: +49 6151 16 49 36 e-mail: juano@mes.tu-darmstadt.de

ABSTRACT.

This work addresses the design of a 4th order bandpass sigma delta modulator (BPSDM) for IF AD converters suitable for second generation cellular standards such as GSM. The resonator architecture of a BPSDM can be derived from the transfer characteristic of a lowpass modulator by means of mathematical transformations. It can be observed that each transformation results in a different cascade of resonators (COR). Therefore different values of performance metrics like SNR, dynamic range, robustness against circuit non-idealities and SFDR can be expected. Behavioral simulations at the architectural level were carried out to find the COR that best meets the requirements imposed by the GSM communications standard and minimizes requirements of the sub-circuits used in the chosen architecture. A BPSDM was designed and sent to fabrication, using a 0.3μm, double polysilicon, triple metal, N-well CMOS technology. Simulation results are showing that the proposed prototype reaches a SNR of 85dB and a sampling rate of 80MHz.

Keywords: Bandpass sigma delta modulators and IF digitization.

1. INTRODUCTION

The sigma-delta modulation constitutes an interesting data conversion technique for modern communication systems because of its robustness against various analog circuit impairments, low-cost VLSI monolithic implementation and the achievable tradeoffs between resolution and bandwidth. Oversampled BPSDM converters offer particularly significant advantages in the implementation of radio receivers because of their potential ability of supporting different emerging wireless standards. Data conversion at the intermediate frequency (IF) can facilitate the realization of flexible receiver architectures by moving the analog signal processing such that I and Q separation and channel-select filtering are performed in the digital domain. Furthermore problems related to dc offsets and low frequency noise (1/f noise) can be avoided by digitizing the signal at the IF stage of a radio receiver. However, as A/D conversion is moved away from baseband, the converter must sample at higher rates and other requirements such as SFDR increases. This paper describes the design of a 4th order BPSDM for GSM receivers. The presented modulator uses a COR architecture. Particular emphasis was done in exploring the attainable performance, at the architectural level, when the COR is derived using different mathematical transformations. This paper is structured as follows: after this introduction, the architectural analysis and design is going to be presented. Third, the circuit and layout design of the modulator is shown. Finally, some conclusions are given.

2. ARCHITECTURAL DESIGN
2.1.- BPSDM's under study.
The most common way to design a BPSDM is to take a low pass modulator and to apply a low pass to band pass transformation. The simplest transformation is the $z^{-1} \rightarrow z^{-2}$ [1] transformation, whose effect is to change the integrators of the low pass prototype into resonators having poles at $\pi/2$ in a normalized discrete time frequency axis. A more general low pass to band pass transformation is the one proposed by Constantinides [2]:

$$z^{-1} \rightarrow \frac{-z^{-2} + \cos(2\pi f_C/f_S)z^{-1}}{1 - \cos(2\pi f_C/f_S)z^{-1}} \tag{1}$$

This transformation allows to put the poles of the resonators at any angle between 0 and π. Another family of resonators is derived using the continuous to discrete time bilinear transformation. Here a continuous time resonator is transformed into a discrete time IIR filter by performing the operation [3]:

$$H(z) = H(s)\big|_{s=\frac{1-z^{-1}}{1+z^{-1}}} \tag{2}$$

and the non-linear mapping:

$$\omega_D = 2\arctan(\omega_C) \tag{3}$$

After the low pass modulator proposed in [4], the three transformations were used to design the BPSDM prototypes (fig. 1). For (1), a ratio $f_c/f_s=1/6$ was taken.

(A)

(B)

(C)
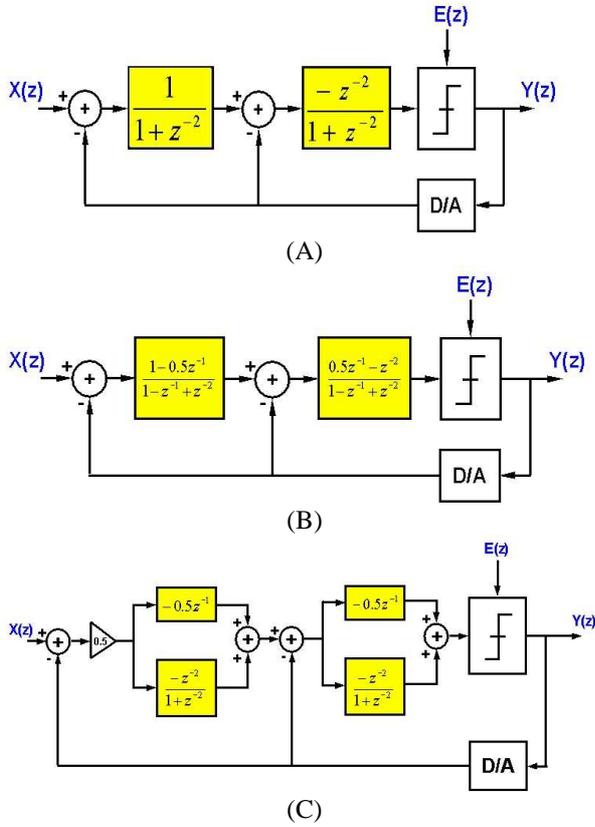
Figure 1.- The three BPSDM's under study

Resonators designed using (2) were derived from continuous time resonators having the transfer function:

$$H(s)=\frac{1}{s^2+\omega_C^2} \qquad (4)$$

Using (3) with $\omega_D = \pi/2$ it is obtained:

$$H(s)=\frac{1}{s^2+1} \qquad (5)$$

Applying (2) over (5) produces:

$$H(z)=\frac{1}{2}+\frac{z^{-1}}{1+z^{-2}} \qquad (6)$$

A delay free branch not realizable in switched capacitor is obtained. Multiplying (6) by $-z^{-1}$ adds the needed delay:

$$H(z)=-\frac{1}{2}z^1-\frac{z^{-2}}{1+z^{-2}} \qquad (7)$$

The so obtained architecture is depicted in fig. 1(C).

2.2.- Linearized analysis using ideal resonators.
Assuming that the quantization error is modeled as an additive white noise source, the quantizer included in each architecture, can be replaced by the linear model shown in fig. 2. In such a case, the BPSDM's presented in fig. 1 can be viewed as two input, $X(z)$ and $E(z)$, one output, $Y(z)$ systems, which in the z domain can be represented by:

$$Y(z) = S_{TF}(z)X(z) + N_{TF}(z)E(z) \qquad (8)$$

Where $S_{TF}(z)$ and $N_{TF}(z)$ are the signal transfer function and the noise transfer function respectively.
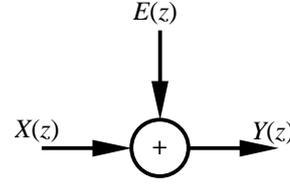
Figure 2.- Linear model of the quantizer.

For the BPSDM in fig. 1(A) it is obtained:

$$S_{TF}(z)=-z^{-2} \qquad (9)$$
$$N_{TF}(z)=(1+z^{-2})^2 \qquad (10)$$

The quantization noise power spectral density (S_Q) is shaped by the transfer function given in (10), which has zeros at $\pi/2$ and $3\pi/2$ in a normalized discrete time frequency axis, suppressing so the quantization noise power around those frequencies. For the BPSDM in fig. 1(B) it is obtained:

$$S_{TF}=\frac{1+4z+6z^2+4z^3+z^4}{1+6z^2-4z^3+9z^4-4z^5+8z^6}$$

$$N_{TF}=\frac{8z^2+16z^4+8z^6}{1+6z^2-4z^3+9z^4-4z^5+8z^6} \qquad (11)$$

The S_Q is shaped by (11) which has zeros at (0, $\pi/2$, $3\pi/2$). For the architecture depicted in fig. 1(C) it is obtained:

$$S_{TF}=\frac{0.5z-1.25z^2+0.5z^3}{0.25z^2-z^3+z^4}$$

$$N_{TF} = \frac{1 - 2z + 3z^2 - 2z^3 + z^4}{0.25z^2 - z^3 + z^4} \qquad (12)$$

Equation (11) has zeros at $(\pi/6, 5\pi/6)$ it is expected that this modulator suppresses the quantization noise around frequencies of value $f_S/6$. Figure 3 shows the FFT of the output of each modulator respectively after high level simulations performed using MIDAS [5]. For each simulation, the input signal was a sinusoid with an amplitude -10 dB with respect to the quantizer level.

(A)

(B)

(C)
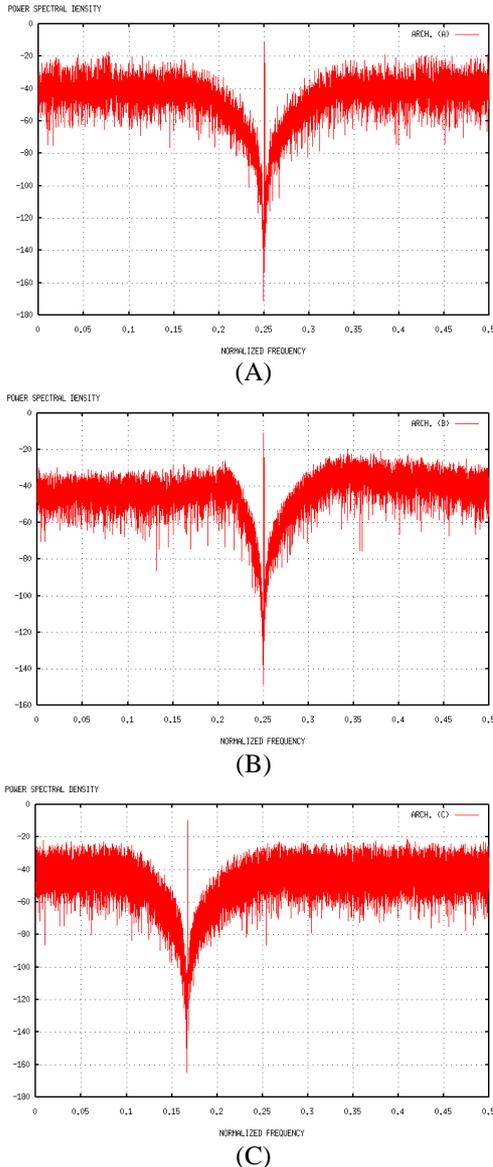
Figure 3.- FFT of the simulated output for each architecture.

For each modulator, high level simulation of the SNR and SFDR using ideal resonators were carried out.

Figure 4(A) shows a graph of the SNR versus input signal level for every architecture, while figure 4(B) depicts the SFDR.

(A)

(B)
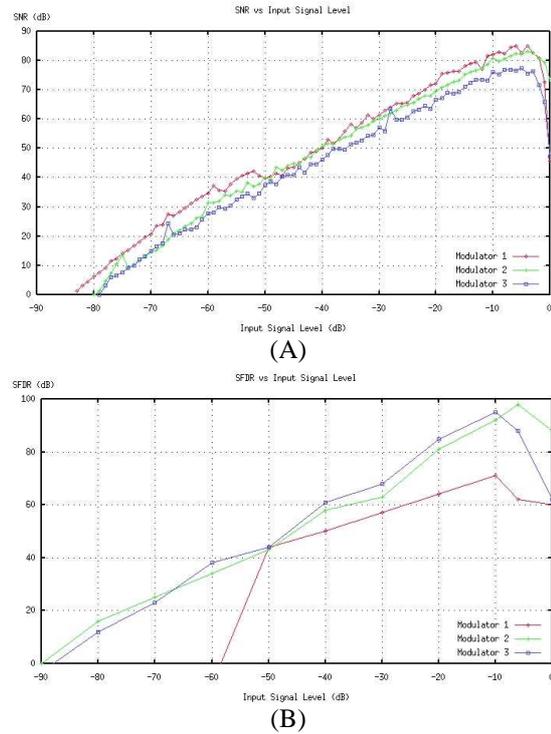
Figure 4.- Simulated SNR and SFDR estimated from simulations for each modulator.

Peak SNR values of 85, 82 and 77 dB were obtained respectively. In terms of resolution, the first architecture best meets the requirements of the GSM standard (84 dB). The other specification is the SFDR. The value required by GSM is 100 dB. Graphics of the SFDR estimated form simulation results show for each architecture a value of 71, 98 and 95 dB respectively. Although the highest SNR value is obtained with the first COR, it has the poorest SFDR. Neither of them meet GSM specifications (SNR=84 dB and SFDR=100 dB), then a compromise should be found. The SNR of the third architecture leaves it out of order. The first architecture has a very good SNR but the SFDR is very low. This problem could be solved at the digital domain using algorithms for improving SFDR [5]. Such algorithms are state variable compensation, phase plane compensation and projection filtering. The values obtained with the second architecture are closer to the needs, the SNR performance could be improved by using a higher order digital filter, since the power of the residual error is decreased by filtering and the same algorithms can be used to reach the desired SFDR, but the fact that the pass band is not situated at $fs/4$ makes the separation of the I and Q channels at the digital domain more complicated and not as simple as a

multiplication by 1, 0, -1, 0. Both solutions at the digital domain are going to be explored. At the current phase of the project the first modulator has been sent to fabricate.

3. CIRCUIT AND LAYOUT DESIGN

There are several ways to implement the transfer function of the resonators of both architectures [6], the delay based resonator structure shown in figure 5 was chosen. With this structure, the functions $1/(1+z^{-2})$ and $-z^{-2}/(1+z^{-2})$ are obtained at the points marked (a) and (b) respectively.
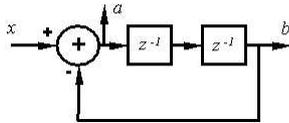

Figure 5.- Delay based resonator.

The half circuit of a fully differential SC cell that adds a delay to a signal is found in figure 6 [7]. In the z domain, the transfer function of this circuit with an ideal op. amp is given by:

$$H(z) = \frac{V_{in}(z)}{V_{out}(z)} = -\frac{C_1}{C_2} z^{-1} \qquad (13)$$
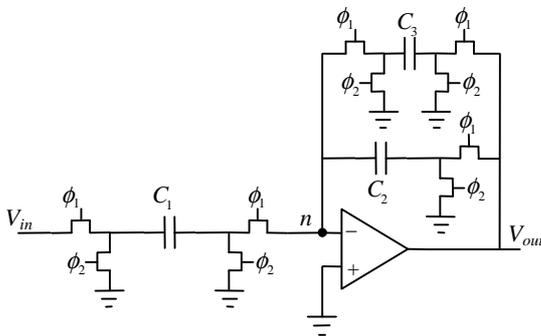

Figure 6.- SC delay circuit.

High level simulations, using models of the operational amplifiers used to construct the resonators, gave the following minimum requirements for the operational amplifiers, in order to avoid degradation of the SNR due to operational amplifier non ideal characteristics: A_V=50dB, SR=80V/µs, T_S=4ns, output signal swing=0.45V_{DD}. With these data a folded cascode op. amp. was designed, using a bias current of 1.5mA the following characteristics were reached: A_V=56dB, SR=365V/µs, T_S=4.9ns, output signal swing=0.69V_{DD}. A regenerative comparator with preamplification and

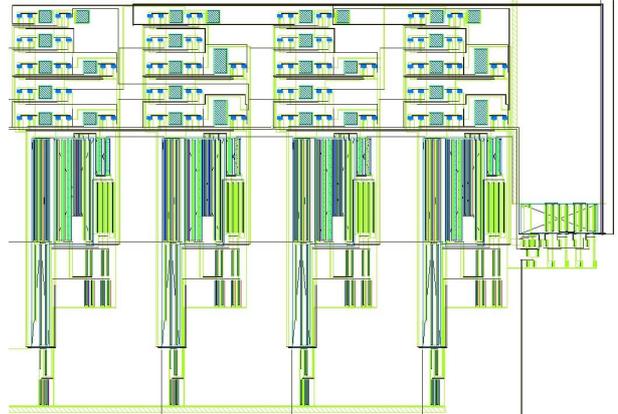output buffers was designed. The layout of the first modulator is presented in figure 7.

Figure 7.- Layout of the bandpass modulator designed with the $z^{-1} \rightarrow -z^{-2}$ transformation.

4. CONCLUSIONS.

Current and future communication standards ask for high performance ADC's. The required characteristics could be reached improving the architecture of the converters or at the digital domain. Both solutions should be compared to find out the optimal one. This paper shows the dependency of the SNR and SFDR with respect to the complexity of the resonators of a BPSDM. As future work the circuit design an fabrication of the second BPSDM is going to be done as well as the measurements of the first prototype. The implementation of the algorithms for improving SFDR is going to be carried out to compare both solutions.

5. REFERENCES.

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