Band-Pass Sigma-Delta Modulator with 5 MHz Bandwidth and 80 MHz IF

G. Bernardinis[(1)], A. Centuori[(1)], U. Gatti[(2)], P. Malcovati[(3)], F. Maloberti[(1, 4)]

[(1)] Department of Electronics, University of Pavia, Via Ferrata 1, 27100 Pavia, Italy
Tel. +39 0382 505205, Fax. +39 0382 505677, E-Mail: g.bernardinis@ele.unipv.it

[(2)] Siemens Information and Communication Networks S.p.A., 20092 Cinisello Balsamo, Milano, Italy
Tel. +39 02 27337415, Fax. +39 02 27337151, E-Mail: umberto.gatti@icn.siemens.it

[(3)] Department of Electrical Engineering, University of Pavia, Via Ferrata 1, 27100 Pavia, Italy
Tel. +39 0382 505256, Fax. +39 0382 505677, E-Mail: p.malcovati@ele.unipv.it

[(4)] Department of Electrical Engineering, PO Box 830688, EC33, Richardson, TX 75083-0688, USA
Tel. +1 972 883 2996, Fax. +1 972 883 2710, E-Mail: franco.maloberti@utdallas.edu

Abstract

In this paper we present a sigma-delta modulator for wide-band base transceiver station receivers. The modulator, based on a four-path architecture, achieves an equivalent sampling frequency of 320 MHz, although the building blocks operate at only 80 MHz. The circuit in simulation achieves 94 dB signal-to-noise ratio with a signal bandwidth of 5 MHz centered around an intermediate frequency of 80 MHz. Behavioral simulations of the complete sigma-delta modulator, including the most important non-idealities, as well as transistor-level simulations of the most critical building blocks are reported.

1. Introduction

Wide-band base transceiver station (BTS) receivers based on the software radio (SWR) technique [1] require an A/D converter with challenging specifications, particularly in terms of signal-to-noise ratio (*SNR*), sampling jitter, spurious-free dynamic range (*SFDR*) and intermediate frequency (*IF*) value, which together with the *SNR* determines the maximum clock frequency (f_s). Obviously, practical limits in the implementation of the A/D converter impose a compromise between the above features.

From system-level considerations it turns out that optimal performances are achieved with an *IF* value around 80 MHz [2, 3]. When using state-of-the-art commercially available A/D converters (with a maximum sampling frequency of 40 MHz), therefore, we are forced to consider for the conversion the third Nyquist zone. However, although commercial A/D converters with the required specifications nominally exist, their linearity performances significantly degrade for such high *IF*. Moreover, using converters with a "lowpass" transfer function extended over the third Nyquist zone for handling signals with a bandwidth of 5 MHz is definitely a waste of resources. Therefore, it could be interesting to implement an A/D converter with a "bandpass" transfer function, such as a bandpass sigma-delta (ΣΔ) modulator, centred at the desired *IF*. Such a solution allows us to convert into the digital domain only the band around the *IF*, thus reducing the in-band thermal noise requirements (the thermal noise contributions outside the signal band are eliminated in the digital domain) and to optimize the quantization noise only in the band of interest.

A rough evaluation on a 4th-order bandpass ΣΔ modulator architecture indicates that to achieve the desired *SNR* of 85 dB, an oversampling ratio (*OSR*) equal to 32 is needed. If a single-path approach is considered to implement the bandpass ΣΔ modulator [4, 5], it would lead to a prohibitive clock frequency with present technologies (f_s = 320 MHz). We have therefore to consider sigma-delta modulators based on multiple paths. In particular, in this paper we propose a 4-path bandpass ΣΔ modulator (Fig. 1), where each path features a lowpass signal transfer function (*STF*) and a highpass noise transfer function (*NTF*) operating at a clock frequency f_s = 80 MHz. In this case, the overall equivalent sampling frequency is still 320 MHz, but all of the blocks operate at only 80 MHz, thus making this solution feasible with present technologies.

2. ΣΔ Modulator Architecture

Referring to Fig.1, if $T_s = 1/f_s$ is the sampling period at the modulator output, phases Φ_1 to Φ_4 have a period equal to 4 T_s and are shifted each other by a quarter of the period. From the theory of multiple path circuits in the *z*-domain it can be demonstrated that

$$H_{TOT}(z) = V_{out}(z)/V_{in}(z) = H_P(z^4), \qquad (1)$$

where $H_P(z)$ is the transfer functions of the single path. If $H_P(z)$ has lowpass shape, its spectrum, replicated every $f_s/8$, leads to the desired bandpass *NTF*.

The main advantage of this solution is that each path operates at a frequency which is a quarter of the equivalent modulator frequency (in our case 80 MHz and 320 MHz, respectively). Moreover, the lowpass transfer function is inherently less sensitive to capacitance mismatches than the bandpass transfer function. Finally, as it will be shown later, this solution allows us to achieve the same *SNR* performance than single-path topologies with an higher order, with benefits for the stability and the complexity of the circuit.

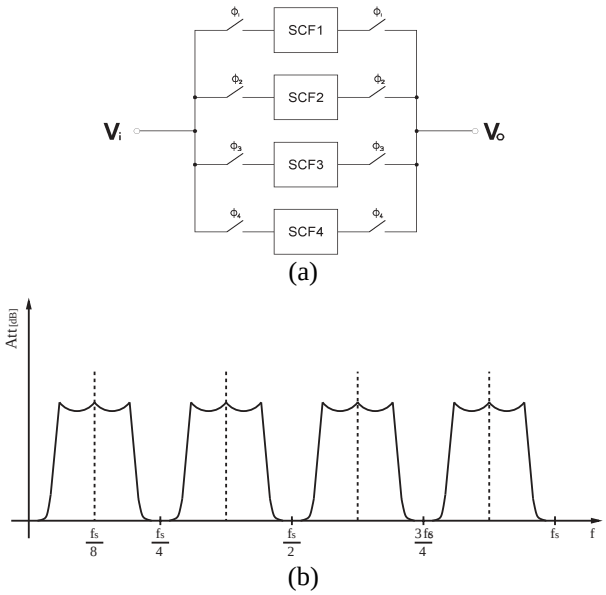

Figure 1. Block diagram (a) and output spectrum (b) of the 4-path sigma-delta modulator

The design of the modulator in the first place requires the implementation of a *NTF* which fulfils the specifications for the single path. The *STF* is then obtained automatically. From the converter *SNR* specifications we derived a highpass filter mask for the *NTF* with a stop-band limit of 2.5 MHz, an in-band attenuation of 85 dB, a ripple of 0.5 dB and a pass-band limit of 12 MHz. These requirements can be achieved with two couples of complex conjugate zeros located around 1.1 MHz and 2.5 MHz respectively. We have then to identify a circuit topology with a number of degrees of freedom (coefficients) sufficient to allow the implementation of the desired *NTF*. By using conventional architectures, such as cascade of resonator in feedback, cascade of resonator in feedforward or cascade of integrators, we obtain a system of equations which cannot be solved, thus making impossible the synthesis of the desired *NTF*.

To overcome this problem, we defined a new topology, whose block diagram is shown in Fig. 2. The internal structure of the resonators is depicted in Fig. 2 as well. We can note from the schematic diagram, that there is only one clock period of delay (z^{-1}) between the instant in which the input is sampled and the instant in which the result is fed back by the D/A converter into the input node, where it is subtracted from the next input sample. This was the main challenge in the actual switched capacitor (SC) implementation of the modulator, where we adopted some expedients to achieve the result avoiding the simultaneous concurrent settling of two cascaded integrators. Finally, we used a 9-levels quantizer to achieve the desired *SNR* and to ensure the stability of the modulator. This choice also avoids the presence of idle tones, since it reduces the power of the quantization noise.

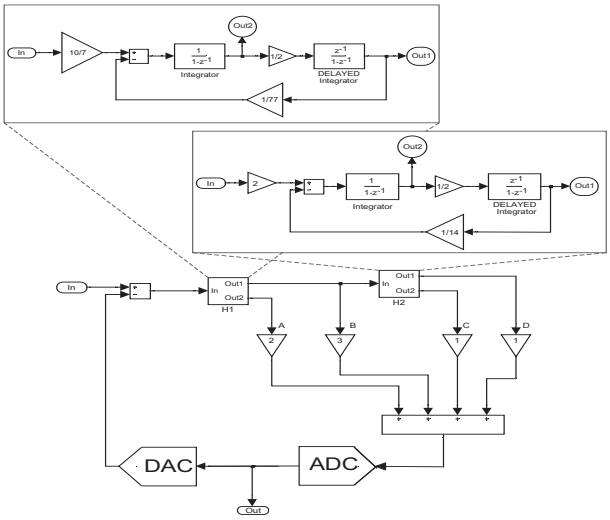

Figure 2. Block diagram of one path of the proposed sigma-delta modulator

3. Switched Capacitor Implementation

In the actual SC implementation, the resonators of Fig. 2 are realized using the circuit shown in Fig. 3. The sizing of the coefficients has been performed keeping in mind that, to maximize the precision of the position of poles and zeros in the filter, the product of the feedforward coefficient and the feedback coefficient must have a tolerance better than the 5%.

In fact, if we indicate with C_T the equivalent capacitance seen from the output *Out* to virtual ground in the T-structure used in Fig. 3, the transfer function of the resonator becomes

$$\frac{Out}{In}(z) = \frac{C_2 C_1 z^{-1/2}}{C_{f2} C_{f1} (1 - z^{-1})^2 + z^{-1} C_2 C_T}. \qquad (2)$$

This transfer function features a couples of purely imaginary poles given by

$$z_{1,2} = e^{\pm j\vartheta}, \qquad (3)$$

where ϑ is the angular position of the pole on the unit circle in the *z*-plane representation. The resonant frequency of the circuit consequently is

$$\omega_0 = f_s \cdot \vartheta \text{ with } \vartheta = \operatorname{acos}\left(1 - \frac{C_2 C_T}{2 C_{f1} C_{f2}}\right). \qquad (4)$$

From behavioral simulations of the system performed with a dedicated toolbox [6], it turns out that errors which affects any other capacitance ratios except those determining ϑ, can be as large as 10%. This is a useful feature to dimension the capacitors, because it allows us to approximate the ideal coefficients with fractional ratios. The "basic" capacitive element is the capacitor used in the T-structure. Since the equivalent capacitance of the T-structure, referring to Fig. 3, is given by

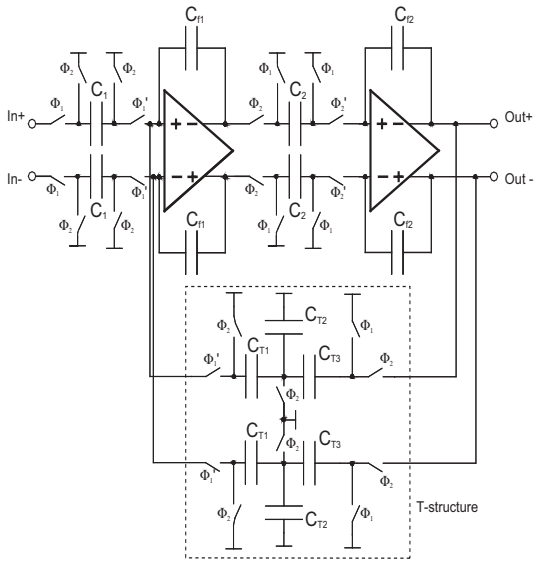

Figure 3. SC implementation of the resonator

$$C_T = \frac{C_{T1}C_{T3}}{C_{T1} + C_{T2} + C_{T3}}, \quad (5)$$

we have chosen $C_{T1} = C_{T3} = C$ to minimize C_T and use C as the brick to build the other capacitors.

Fig. 4 shows the structure of the comparator, which is also used for the sum of the four signals coming from the resonators at the input of the ADC. The charge accumulated in the capacitor C during clock phase Φ_2, is redistributed on the whole capacitance seen from the comparator input during the clock phase Φ_1. The expression of the voltage at the input of the comparator during Φ_1 is the given by

$$V_x = \frac{V_A 2C + V_B 3C + V_C C + V_D C - V_{ref} C}{8C}. \quad (6)$$

This voltage is then compared with zero. Obviously voltage V_{ref} is different in the 8 comparators used to implement the quantizer. Furthermore, if we consider also the input capacitance of the comparator, the denominator of Eqn. (6) increases, leading to a further attenuation of signal V_x.

The difference between the addition implemented with an active circuit and the proposed solution based on the charge redistribution is that in the latter the result is scaled by a coefficient (in our case 8), thus increasing the input referred comparator offset. On the other hand the use of active circuits would lead in our case to the simultaneous settling of two operational amplifiers (op-amps) in cascade. To overcome the signal attenuation and the offset problem, we introduced a simple gain stage with autozero in front of the comparator, as shown in Fig. 5.

4. Building Blocks

In this section we present two of the basic building blocks of the modulator: the op-amp (Fig. 6) and the comparator

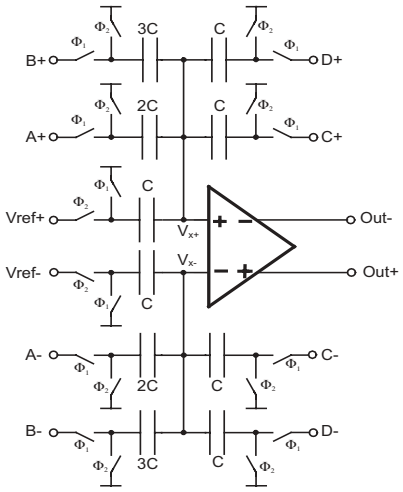

Figure 4. SC implementation of the comparator

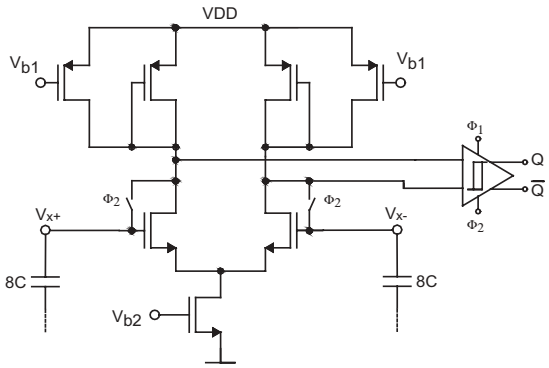

Figure 5. Comparator structure: gain stage followed by a latch

(Fig. 5). For the op-amp we have chosen a folded cascode architecture with n-channel input stage, in order to ensure a high output swing. Indeed, from the behavioral simulations of the complete sigma-delta modulator [6] it turns out that the linear range of the op-amp must be as high as ±1.4 V differential, with a 3.3 V power supply. The other circuit requirements obtained from the behavioral simulations are 80 dB of gain, 325 MHz of gain-bandwidth product and 400 V/μs of slew rate. To fulfil these requirements, we used a gain boosting technique to enhance the output resistance of the p-channel branch of the cascode [7]. The dynamic common-mode feedback circuit (CM-FB) consist of a conventional SC circuit that consumes almost no power. The complete schematic of the op-amp is shown in Fig. 6.

The comparator consist of a gain stage followed by a latched stage [8]. During clock phase Φ_2, which is the reset phase, the latch is reset and at the same time the gain stage is closed in unit gain configuration, thus storing the input referred offset error in the capacitors connected to the input terminal of the comparator (V_x). During clock phase Φ_1, then, the amplifier and offset-free signal at node V_x is compared with zero. With this structure, we

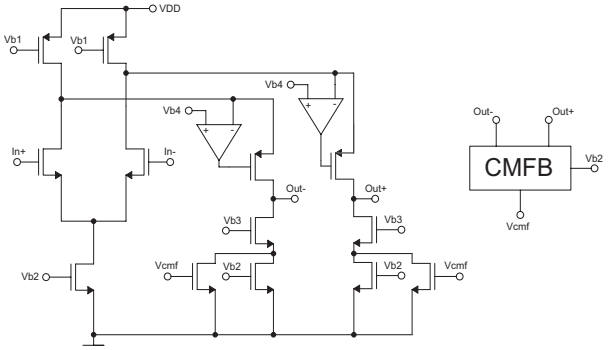

Figure 6. Folded cascode OTA with gain boost and CMFB

strongly reduce both the offset error and the attenuation problem deriving from the charge redistribution.

5. Simulation Results

In the behavioral simulations of the complete sigma-delta modulator we achieved a resolution of more than 16 bits, considering only the op-amp non idealities. Including also the noise of the first integrator (the noise contributions of the other integrators are negligible) we obtained the output spectrum shown in Fig. 7, which leads to a *SNR* of 94 dB (15.3 bits of resolution). In order to account for additional non-idealities not included in the behavioral simulations, in the design we aimed to a resolution one bit higher with respect to the specifications.

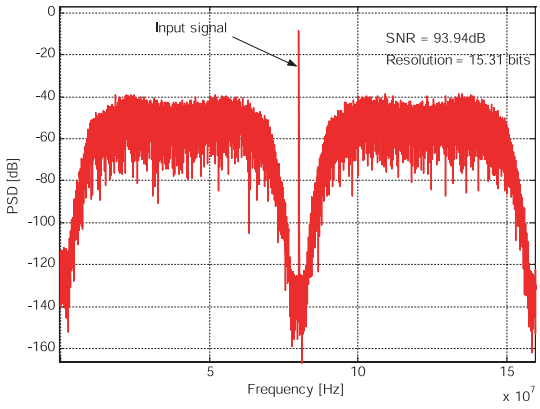

Figure 7. Simulated output spectrum of the ΣΔ modulator considering all of the non-idealities

Tab.1 summarizes the results achieved in the transistor-level simulations of the building blocks. The op-amp is considered in open loop configuration with a capacitive load C_L. With σ we indicate the standard deviation of the input referred offset of the comparator, derived from the parameters of the used technology.

6. Conclusions

In this paper we presented a four-path sigma-delta modulator for wide-band base transceiver station receivers based on the software radio architecture. The modulator features 5 MHz of bandwidth centered around an intermediate frequency of 80 MHz and achieves 94 dB of signal-to-noise ratio. The performances of the sigma-delta modulator have been verified with behavioral simulations of the complete circuit, including the most important non-idealities, as well as with transistor-level simulations of the most critical building blocks.

Parameter	***Value***
Operational Amplifier (C_L = 2 pF)	
Gain-bandwidth product	1.055 GHz
DC gain	103.7 dB
Slew-rate	740 V/μs
Power consumption	18.2 mW
Comparator	
Sensitivity	2 mV
Settling time (V_x = 10 mV)	1.5 ns
Reset time	0.2 ns
Input referred offset (σ)	6.3 mV

Table 1. Simulated performances of operational amplifier and comparator

Acknowledgements

The research was partially supported by MEDEA+ in the frame of Project ANASTASIA+ A510.

References

[1] B. Schweber, “Converters Restructure Communications Architectures”, *EDN*, pp. 51-64, Aug. 1995.

[2] CATT, “TD-SCDMA Radio Transmission Technology”, Ver. 1.0.0, Dec. 1999.

[3] A. M. Badà, M. Donati, “The Software Radio Technique Applied to the RF Front-End for Cellular Mobile Systems”, *Proc. Workshop on Software Radio: Technologies and Services*, Isola d’Elba, Italy, Sept. 2000.

[4] S. Jantzi, M. Snelgrove, P. Ferguson, “A Fourth-Order Bandpass Sigma-Delta Modulator”, *IEEE J. of Solid-State Circuits*, vol. 28, pp. 282-291, Mar. 1993.

[5] B.-S. Song, “A Fourth-Order Bandpass Delta-Sigma Modulator with Reduced Number of Op Amps”, *IEEE J. of Solid-State Circuits*, vol. 30, pp. 1309-1315, Dec. 1995.

[6] S. Brigati, F. Francesconi, P. Malcovati, D. Tonietto, A. Baschirotto, F. Maloberti, “Modeling Sigma-Delta Modulator Non-Idealities in SIMULINK”, *Proc. of IEEE ISCAS 1999*, pp. 384-387, May 1999.

[7] Y.Geerts, A. Marques, M. Steyaert, W. Sansen, ”A 3.3-V, 15-bit, Delta-Sigma ADC with a Signal Bandwidth of 1.1 MHz for ADSL Application”, *IEEE J. of Solid-State Circuits*, vol.34, pp. 927-936, Jul. 1999.

[8] G. M. Yin, F. Op’t Einde, W. Sansen, “A High-Speed Comparator with 8-b Resolution”, *IEEE J. Solid-State Circuits*, vol. 27, pp. 208–211, Feb. 1992.