A FRAMEWORK FOR EXTERNAL DYNAMIC COMPENSATION OF AD CONVERTERS

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ABSTRACT

External correction of analog-to-digital converters is considered. First, a dynamic correction scheme is proposed to comprise bit-masking. Next, a framework for analyzing the effects of bit-reduced table indexing is derived. This framework is finally applied in an optimization problem for bit allocation in the bit mask of the introduced correction scheme.

Both the dynamic correction method and the optimization problem are exemplified with experimental AD data. The results indicate that the considered correction scheme is superior to static schemes, and that the choice of bit mask is crucial, motivating the analysis framework.
Keywords: dynamic correction, optimization, bit allocation.

1 INTRODUCTION

The demand for broad-band analog-to-digital converters (ADCs) is increasing rapidly. In third-generation mobile communications, for instance, broad-band linearity of the radio receiver ADC is a crucial property. It is a well-known fact that practical AD converters suffer from various errors, e.g., gain, offset and linearity errors. These stem from numerous sources such as non-ideal spacing of transition levels and timing jitter, to mention a few, and they contribute to deterioration of the broad-band performance of the converter. Several methods have been proposed to *externally* compensate for such errors, e.g., [1, 2, 3]. External in this case implies that digital signal processing methods which operate *outside* of the actual converter are used in the correction schemes.

In this paper, a generalized form of the dynamic calibration and compensation method proposed in [4] is presented. This novel form comprises bit masks to reduce the table memory requirements by selecting fewer addressing bits. In the context of this correction method, the problem of investigating the effect of a certain bit mask arises. Therefore, a framework for analyzing the performance of reduced-bit table indexing is derived. Finally, using this framework, an optimization problem for the bit mask is posed, and exemplary solutions are presented.

2 DYNAMIC COMPENSATION

In classic look-up table correction, the error table (containing the error associated with each transition level) is addressed using the present ADC output sample. Obviously, this addressing yields the same correction for a given ADC output sample, regardless of the dynamic properties of the input signal; the correction is *static*. By addressing the error table with both the present sample and the previous sample, the correction becomes dependent on the signal dynamics. This method, sometimes referred to as the 'state-space' method, has been proposed several times [2, 5] and can be interpreted as a 2-dimensional error table. The motivation for introducing dynamics is, of course, that the errors sought to mitigate for in general show a dependence upon signal dynamics.

The dynamic calibration and compensation scheme that was presented in [4] introduced a novel indexing (or addressing) for look-up table correction. In this scheme the index was built by concatenating the present ADC output sample with (quantized versions of) previous (i.e., delayed) ADC output samples. This approach is an extension of the state-space method, involving not only the first previous sample, but an arbitrary number of delayed samples; with the present sample and K delayed samples used for addressing, the error table is made $(K+1)$-dimensional. In the present paper, the scheme is generalized to contain a bit mask, instead of the quantization of samples, as illustrated in Figure 1. The figure depicts the compensation system outline, i.e., the structure used during normal ADC operation.

The b-bit output samples $x(n)$ through $x(n-K)$,

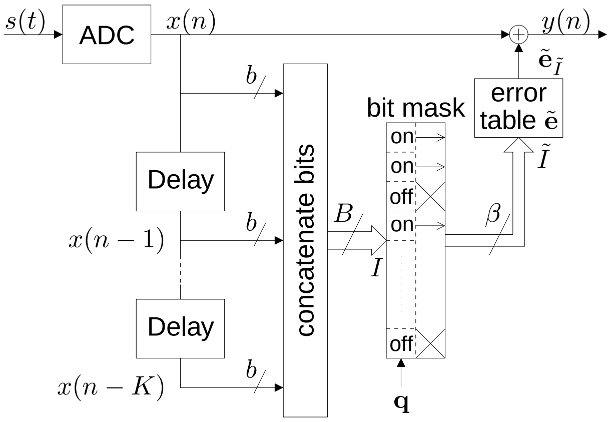

Fig. 1. Dynamic compensation system outline. Delayed samples are stacked together with the present sample to form an index I. The index is then masked to produce the reduced index $\tilde{I}$, where a subset of the bits in I have been selected. This index is finally used to address the error table.

from the ADC and the K-step delay ladder, are stacked together to form a B-bit index I, where $B = (K + 1)b$. Since B is likely to be large, resulting in huge memory requirements for the look-up table, the index I is *bit-masked*. This implies that a subset of β bits ($\beta < B$) is selected from I to form the bit-reduced β-bit index $\tilde{I}$. This index is then used to address the error table $\tilde{\mathbf{e}}$ of size $M = 2^{\beta}$. The selection is determined by the bit mask vector $\mathbf{q}$ of length B; a '1' in the i-th position indicates that the i-th bit of the index I should be propagated to the reduced index $\tilde{I}$, while a '0' indicate that is should not. Through this operation the index size, and thereby the memory requirements, can be reduced while maintaining dynamics information. Thus, for each sample time n an index (or address) $\tilde{I} \in \{0, \ldots, 2^{\beta} - 1\}$ depending on $x(n), \ldots, x(n-K)$ is used to select the correction value $e(n) = \tilde{\mathbf{e}}_{\tilde{I}}$. Finally, the corrected ADC output is obtained from $y(n) = x(n) + \tilde{\mathbf{e}}_{\tilde{I}}$.

In order to calibrate the error table $\tilde{\mathbf{e}}$, both the calibration signal $s(t)$ and the resulting ADC output $x(n)$ must be available on the 'digital side' of the ADC. Usually this is accomplished by using a reference device, i.e. an ADC with superior characteristics. Alternatively, a digitally generated reference signal could be fed to the ADC under test through a DAC (also with superior characteristics). Both these methods require extra hardware (ADC or DAC). An alternative method, introduced in [1], is used here. The calibration signal is a sinusoid which can be reconstructed using optimal filtering [6] in the digital domain, thus omitting the need for extra hardware. Figure 2 shows the calibration system outline. The block labeled 'index building' is equivalent to the delay–concatenation–bit-masking part of Figure 1.

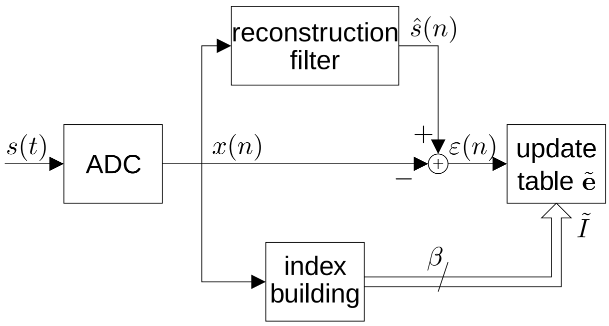

Fig. 2. Dynamic calibration system outline. The block labeled 'index building' is equivalent to the index building blocks in Figure 1. The reconstruction filter estimates the sinusoid calibration signal input to the ADC.

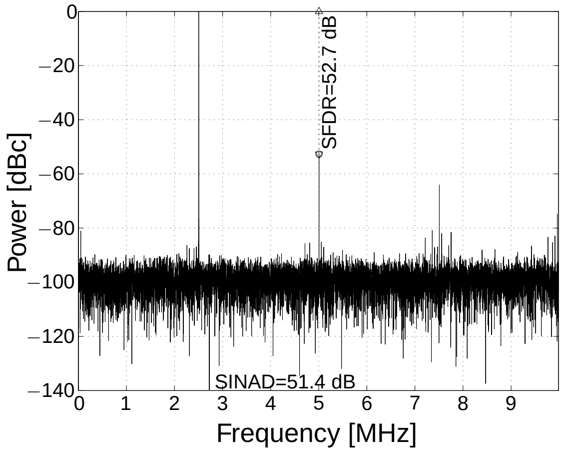

Fig. 3. Example of uncompensated spectrum of the AD876. The ADC is excited with a full-scale sinusoid at 2.50 MHz using a sampling frequency of 19.97 MHz.

Exemplary results

The dynamic error correction presented above has been evaluated using experimental ADC data from an Analog Devices AD876, 10-bit converter. Figure 3 shows a typical uncompensated spectrum of the ADC. The tests were conducted by first calibrating the error table $\tilde{\mathbf{e}}$ using a large number of sinusoid sequences with different frequencies. The ADC performance was then evaluated at several different frequencies, located over the entire Nyquist band, and compared with that of the uncompensated case. Signal-to-noise and distortion ratio (SINAD) and spurious-free dynamic range (SFDR) [7] were used as performance measures. The procedure was repeated for different numbers of delays and different bit masks.

Table 1 shows some exemplary results, presented as *mean* SFDR and SINAD improvements (relative to the uncompensated ADC) over *all test frequencies*. Results

	Configuration	Improvement	
		SFDR	SINAD
1	$K = 1$, 10-bit index	13.3 dB	4.6 dB
2	$K = 1$, 14-bit index	13.2 dB	4.7 dB
3	$K = 4$, 18-bit index	20.4 dB	5.3 dB
4	$K = 8$, 18-bit index	18.7 dB	5.1 dB
5	$K = 0$, 10-bit index	10.6 dB	4.2 dB

Table 1. Performance examples for dynamic correction with different bit masks (cases 1–4), and static correction ($K = 0$, case no. 5).

using static compensation is also presented for comparison [1]. It is interesting to note that the mean SFDR is improved by almost 3 dB from case 5 (static) to case 1; these two cases use the *same table size* ($M = 2^{10}$), but case 1 distributes 5 of the 10 address bits to the one-step delay ($x(n-1)$).

3 STRUCTURED BIT REDUCTION

It can be seen from the performance examples presented above that the configuration of the bit mask $\mathbf{q}$ has a significant impact on the results. Hence, it is interesting to analyze the effects of different choices of $\mathbf{q}$. More precisely, given a calibrated B-bit table $\mathbf{e}$ (having $M = 2^B$ entries), we want to know what errors are introduced by reducing the number of address bits from B to β.

When reducing the number of bits, the length of the table is reduced by a factor $2^{B-\beta}$, making direct comparison between the original table $\mathbf{e}$ and the reduced table $\tilde{\mathbf{e}}$ difficult. Let us therefore, for the purpose of analysis only, introduce the bit-reduced table $\mathbf{f}$. This table has the *same length* as $\mathbf{e}$, while having entries equal to those of a β-bit table $\tilde{\mathbf{e}}$. The table $\mathbf{f}$ is constructed such that if the index I is bit-masked to the reduced index $\tilde{I}$, then $\mathbf{f}_I = \tilde{\mathbf{e}}_{\tilde{I}}$. In other words, if the ADC output at a given moment corresponds to the I-th entry of the B-bit table $\mathbf{e}$, such that $y(n) = x(n) + \mathbf{e}_I$, then, a β-bit table yields $y(n) = x(n) + \tilde{\mathbf{e}}_{\tilde{I}} = x(n) + \mathbf{f}_I$ in the same situation; $\mathbf{e}$ and $\mathbf{f}$ share the same address space. Thus, $\mathbf{f}$ has a $2^{B-\beta}$-fold redundancy, i.e., each entry appears $2^{B-\beta}$ times.

It can be shown (see Appendix) that the redundant reduced-bit table $\mathbf{f}$ is a linear transform of $\mathbf{e}$

$$\mathbf{f} = \mathbf{R}(\mathbf{q}, \mathbf{a})\mathbf{e} \tag{1}$$

where the M-by-M matrix $\mathbf{R}(\mathbf{q}, \mathbf{a})$ is defined in the appendix; $\mathbf{q}$ is the bit mask and the vector $\mathbf{a}$ of length M is the probability (or 'hit-rate') for the corresponding entries in $\mathbf{e}$ during calibration. The benefit of using the redundant table $\mathbf{f}$ is that it is easy to evaluate the effects of the bit reduction. Using the *reduction matrix* $\mathbf{R}(\mathbf{q}, \mathbf{a})$, the difference between a B-bit compensation and a β-bit compensation, at a given moment, can be described by

$$\underbrace{x(n) + \mathbf{e}_I}_{B\text{-bit comp.}} - \underbrace{(x(n) + \mathbf{f}_I)}_{\beta\text{-bit comp.}} = \mathbf{e}_I - [\mathbf{R}(\mathbf{q}, \mathbf{a})\mathbf{e}]_I \tag{2}$$

In the next section we investigate how this can be used in an optimization application.

4 BIT MASK OPTIMIZATION

In this section the bit reduction tools proposed above will be used in an optimization context. Here we use the SINAD as optimization criterion, but other criteria are feasible. The definition for the SINAD is [7]

$$\text{SINAD} = \frac{\text{RMS}_{\text{sig}}}{\text{RMS}_{\text{noise}}} \tag{3}$$

$$\text{RMS}_{\text{sig}} = \frac{A}{\sqrt{2}} \tag{4}$$

$$\text{RMS}_{\text{noise}} = \left(\frac{1}{N} \sum_{n=0}^{N-1} \big(x(n) - \check{s}(n)\big)^2 \right)^{\frac{1}{2}} \tag{5}$$

with A being the amplitude of the input sinusoid. The signal $\check{s}(n)$ is a sine-wave least-squares fit [7] to the ADC output $x(n)$. When dynamic correction is used, $x(n)$ in (5) is substituted with $x(n) + \tilde{\mathbf{e}}_{\tilde{I}} = x(n) + \mathbf{f}_I$.

Assume that the sine-wave fit signal $\check{s}(n)$ can be approximated as

$$\check{s}(n) = x(n) + \varepsilon_0(n) \approx x(n) + \mathbf{e}^0_I, \tag{6}$$

where $\mathbf{e}^0$ is some error table, the same size and structure as $\mathbf{e}$, describing the difference between $\check{s}(n)$ and $x(n)$. Also let the vector $\mathbf{a}^0$ be the probability (or 'hit-rate') for the corresponding table entries during SINAD evaluation ($0 \le n \le N-1$). Then, (5) can be re-written as

$$\text{RMS}_{\text{noise}} = \left(\frac{1}{N} (\mathbf{f} - \mathbf{e}^0)^{\mathrm{T}} \underbrace{\text{Diag}\{\mathbf{a}^0\}}_{\mathbf{A}_0} (\mathbf{f} - \mathbf{e}^0) \right)^{\frac{1}{2}}. \tag{7}$$

Thus, the RMS noise is approximated with the weighted RMS difference between tables $\mathbf{f}$ and $\mathbf{e}^0$.

Since the input amplitude is independent of the bit mask $\mathbf{q}$, maximizing the SINAD (3) with respect to $\mathbf{q}$ is equivalent to *minimizing* the RMS-noise (7). Using (1), a minimization problem can be posed:

$$\begin{cases} \min\limits_{\mathbf{q}} & (\mathbf{R}(\mathbf{q}, \mathbf{a})\mathbf{e} - \mathbf{e}^0)^{\mathrm{T}} \mathbf{A}_0 (\mathbf{R}(\mathbf{q}, \mathbf{a})\mathbf{e} - \mathbf{e}^0) \\ \text{s.t.} & \sum_i \mathbf{q}_i = \beta \quad \text{and} \quad \mathbf{q}_i \in \{0, 1\}. \end{cases} \tag{8}$$

That is, *minimize the weighted noise power with respect to the bit mask* $\mathbf{q}$ *consisting of* β *'1's and the rest '0's.*

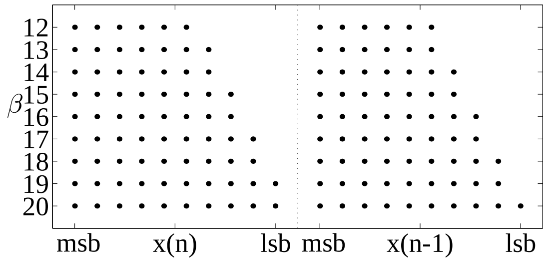

Fig. 4. Exemplary optimization results. Each row corresponds to a certain index size (β). The dots indicate which bits from the present sample (left half) and the one-step delayed sample (right half) that should be included in a β-bit index $\tilde{I}$.

The choice of reference table $\mathbf{e}^0$ impacts on the optimization results. If the objective is to achieve good performance over the same frequency range that was used while calibrating $\mathbf{e}$, then a natural strategy is to let $\mathbf{e}^0 = \mathbf{e}$ and set the 'hit-rate' equal to the distribution of the calibration signal over $\mathbf{e}$, i.e. $\mathbf{a}^0 = \mathbf{a}$.

Optimization results

The optimization problem (8) has been solved for a specific scenario. Experimental data from an Analog Devices AD876 is used. The original table $\mathbf{e}$ is calibrated using one delay block ($K = 1$), full bit mask ($B = 20$, $\mathbf{q} = \mathbf{1}$) and a large number of different calibration frequencies in sequence. The problem (8) is then solved for different β. The reference table was defined $\mathbf{e}^0 = \mathbf{e}$, and $\mathbf{a}^0 = \mathbf{a}$, as suggested above. Figure 4 shows the resulting configurations obtained for this exemplary scenario.

It is interesting to note that the least significant bits in $x(n)$ are discarded before all bits in $x(n-1)$ have been discarded. This implies that the higher bits in $x(n-1)$ carry more information about the error behaviour than the lower bits in $x(n)$, which is in some sense counterintuitive.

5 CONCLUSIONS

A generalized external dynamic correction method for AD converters has been introduced. The method proved to improve the ADC wide-band performance in terms of SINAD and SFDR. Exemplary results show that improvements can be obtained with no or minor memory increase. Second, a tool for analyzing the effects of reducing the table address space was introduced. The tool provided a matrix expression for the bit-reduction implied by selecting a more restrictive bit mask. Finally, the bit-reduction matrix was used in an optimization problem to derive the optimal bit mask in an exemplary scenario.

APPENDIX

The transform (1) from $\mathbf{e}$ to $\mathbf{f}$ is a linear operation, where the M-by-M matrix $\mathbf{R}(\mathbf{q}, \mathbf{a})$ is

$$\mathbf{R}(\mathbf{q}, \mathbf{a}) = \mathrm{Diag}\{\mathbf{\Pi}(\mathbf{q})\mathbf{a}\}^{\dagger}\mathbf{\Pi}(\mathbf{q})\,\mathrm{Diag}\{\mathbf{a}\} \tag{9}$$

and

$$\begin{aligned}\mathbf{\Pi}(\mathbf{q}) &= \frac{1}{M}\mathbf{H}_B\left(\begin{bmatrix}1 & 0\\ 0 & \mathbf{q}_B\end{bmatrix}\otimes\cdots\otimes\begin{bmatrix}1 & 0\\ 0 & \mathbf{q}_1\end{bmatrix}\right)\mathbf{H}_B\\ &\triangleq \frac{1}{M}\mathbf{H}_B\mathbf{Q}(\mathbf{q})\mathbf{H}_B,\end{aligned} \tag{10}$$

$\mathbf{q}_i$ is the i-th element of $\mathbf{q}$. The symbol $\otimes$ denotes the *Kronecker product*, $\mathbf{H}_B$ is a *Sylvester-type Hadamard matrix* [8] of size $M = 2^B$, and $\cdot^{\dagger}$ denotes the *pseudoinverse*. Thus, the result of the bit reduction depends on the new bit mask $\mathbf{q}$ (having β '1's), and on the 'hit-rate' $\mathbf{a}$, describing the distribution of the calibration signal over the entries of $\mathbf{e}$.

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