DATA PROCESSING AND DITHER ENHANCEMENT OF ADC PARAMETERS – TRENDS, APPLICATIONS, LIMITS

Jan Holub[1], Olli Aumala[2]

[1]Czech Technical University, Department of Measurement,
Technicka 2, CZ 166 27, Prague 6, Czech Republic
Tel.: +420 2 2435 2131, fax: +4202 3333 9929, e-mail: HolubJan@feld.cvut.cz

[2]Tampere University of Technology, Lab. MIT,
P.O.Box 692, FIN-33101, Tampere, Finland,
Tel: +358 3 3115 2483, fax: +358 3 3115 2171, e-mail: olli.aumala@mit.tut.fi

ABSTRACT

There is no noise-free place on Earth. Most of noisy effects are undesirable and unwelcome, especially in measuring technology. However, there are some measuring methods and algorithms using noise for quality enhancement. These processes are usually called dithering. Basic ideas of these methods were partially assumed from audio and video signal processing many years ago. The field of dithering technologies in measurement became large in recent years.

keywords: dithering, ADC

INTRODUCTION

The idea of dithering is well established in the area of printing and audio and video technology [1]. One example follows: Dither for B/W printer – greyscale printing can be achieved by changing amount of black pixels within certain area (black pixel density). When fixed pattern within one letter area is used, there is a danger of periodic resulting image (see Fig.1). Many print drivers or even printers itself can generate the pattern randomly which eliminates this risk (see Fig.2). Due to intrinsic low-pass filtering of human eye when observing the image from certain distance, the result is perfectly grey scaled as required.

There are at least the following areas of measurement technology where dither can be used [2,3,4,8,13]:

-Analogue-to-Digital Converter (ADC) dynamic range enhancement by spurious elements elimination
-ADC resolution & linearity enhancement
-Digital-to-Analogue Converter (DAC) resolution & linearity enhancement
-hysteresis suppression for ADC, DAC, sensors and actuators
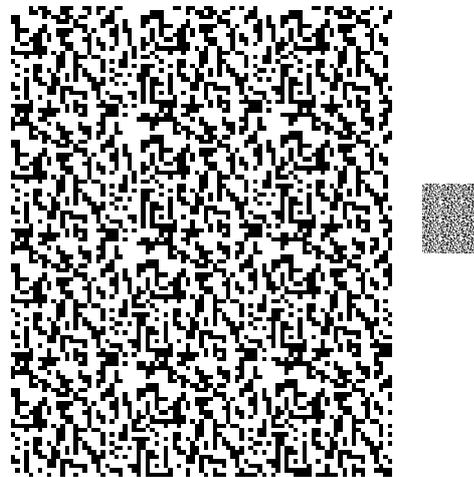-area of limited sensitivity suppression for above mentioned elements.

Fig. 1 Optically periodic print result for grey-scale printing – fixed pattern used

Fig. 2 Dithered grey-scaled print result

General approach to dither application is depicted in the Fig. 3. The input quantity is summed (or multiplied) with dither signal of proper distribution and passed through element that is to be improved. Output of this block is low pass or band pass filtered (either really or intrinsically). The output of the filter (sometimes after decimation) is the system output. Dither signal may be either stochastic (random noise) described e.g. by certain RMS value and probability density function. It can also be a deterministic one (usually periodic), determined by period/frequency and waveform or by slew rate when it is just simple linear ramp. However, it is useful to note that such deterministic signals can be described by the same apparatus as stochastic ones, it is by RMS value and probability density function.
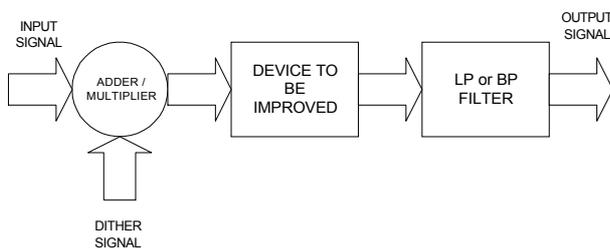

Fig. 3 General principle of dithering

There are many ways to analyse such a system mathematically. Usually, one of the following is used: suitable integral transform (Laplace or Fourier transform – to find characteristic function), statistical approach and modelling by e.g. Monte Carlo method. Alternatively, Theorem of Equivalent Non-linearity (T.E.N.) can be used [2]:

"For the purpose of calculation of conditional expectation any non-linearity $y(x)$ with an input $s+n$ is equivalent to another non-linearity $Y(x)$ with s as its only input. Equivalent non-linearity $Y(x)$ is determined by convolution of original transfer function $y(x)$ with p.d.f. of added component n (for even p.d.f. of n)".

Some examples of its application will be shown further in the text.

Another criteria, used mainly for the case when dither is used to linearize some transfer characteristic, is the Condition of Correct Convergency [3] - for infinite observation time the filtered result has to be equal to the desired (e.g. ideally linear) value.

ADC DYNAMIC PROPERTIES ENHANCEMENT BY SPURIOUS ELEMENTS ELIMINATION

This topic has been studied in detail e.g. by Halamek [4]. The basic scheme is depicted in the Fig. 4: Noise floor is raised by artificially generated noise but spurious elements are decreased by dither. As a result, Signal-to-Noise-and-Distortion (SINAD) and Spurious-free-Dynamic Range (SFDR) is increased.
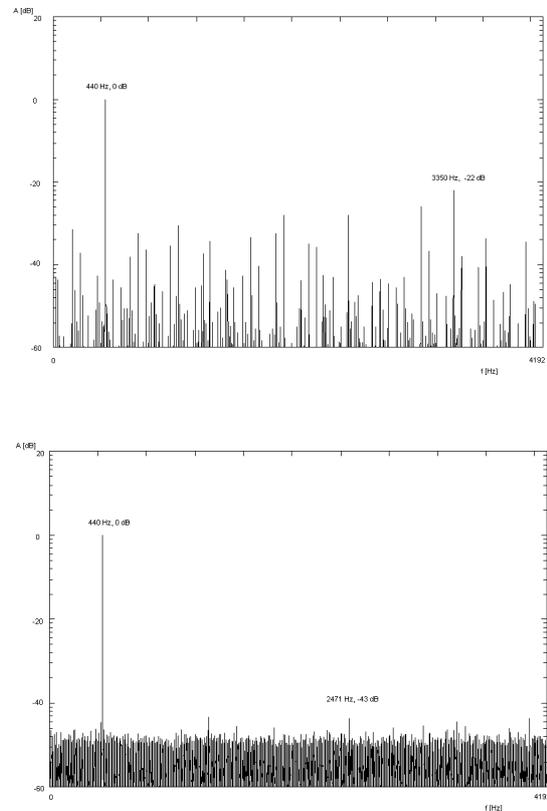

Fig. 4 Dither effect on the spectrum of sampled signal – spectrum of digitized harmonic signal, covering 5 LSB without dither (upper picture) and with random dither signal –9dB (lower picture) – noise floor is raised but spurious components are significantly decreased (-22 vs. -43 dB)

Usually, the following question is associated with this topic: Is there any LP filtering present in this case? The answer is positive. Intrinsically, the observation method (which is usually FFT or DFT) gives one integral result for the whole record. This substitutes LP filtering in other cases of dither.

There is an interesting and simple example available: Influence of noise background level to human perception of roughly quantized harmonic signal. This is a common situation in telecommunication when low level signal is quantized and then amplified by Automatic Gain Control (AGC) stage of the communication chain. The human perception provides an intrinsic LP filtering.
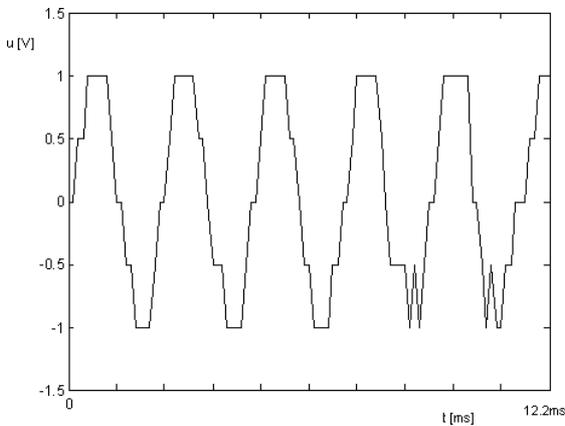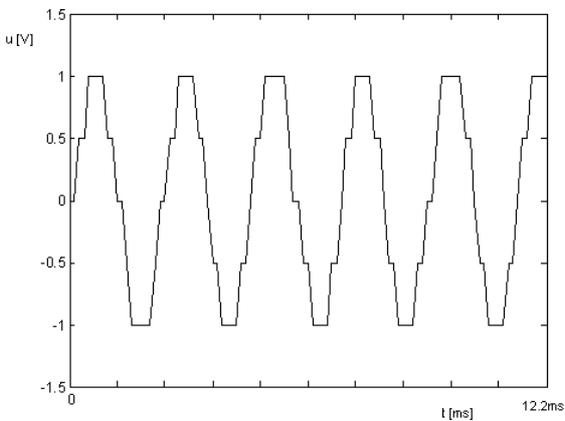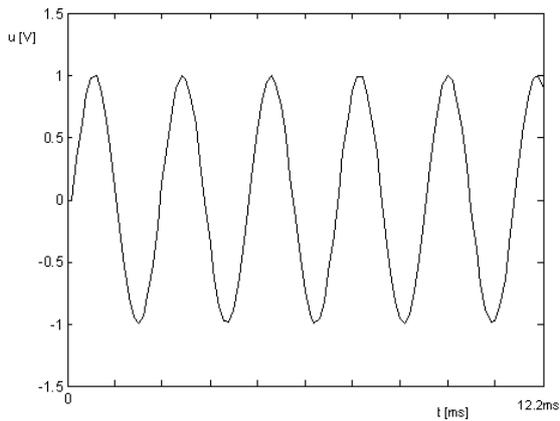
HYSTERESIS AND INSENSITIVITY AREA SUPPRESSIONS

The influence of dither to hysteresis depends on its type. A simple case is shown in the Fig. 6.
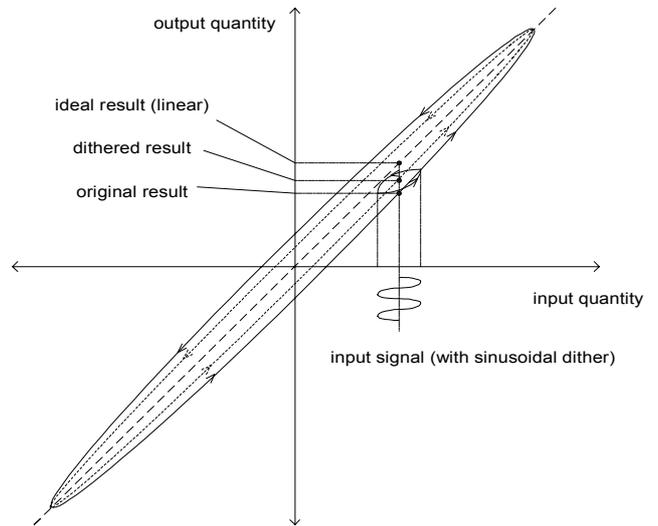

Fig. 6 Hysteresis suppression

As for the dead zone suppression, the situation is depicted in the Fig. 7. Theorem of Equivalent Non-linearity (TEN) [2] can be used in this case easily to evaluate resulting linearity. It is easy to understand that deterministic dither is an advantage in this case to speed up the convergence.
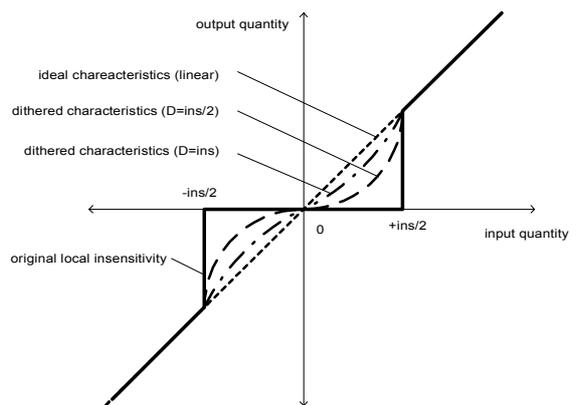

Fig. 7 Local insensitivity suppression (zoomed)

Fig. 5 Harmonic signal 440 Hz before (upper picture) and after(middle picture) quantization (5 LSB covered). Quantization with dither- white noise at −17 dB (lower picture)

Optical (laser) accelerometers and relative pressure sensors based on pressurised mechanical resonator use often dither to eliminate low sensitivity around zero.

ADC AND DAC: RESOLUTION AND LINEARITY ENHANCEMENT

Dither can be used to enhance both resolution and linearity of AD converters. This topic will be discussed now in more detail. First, ideal AD converter will be considered. Two basic arrangement are usually analysed – non-subtractive and subtractive (see Fig. 8). For subtractive arrangement both the analogue and the digital versions of the dither signal have to be available. This is easy to fulfil in case of digitally generated dither signal (by DAC).
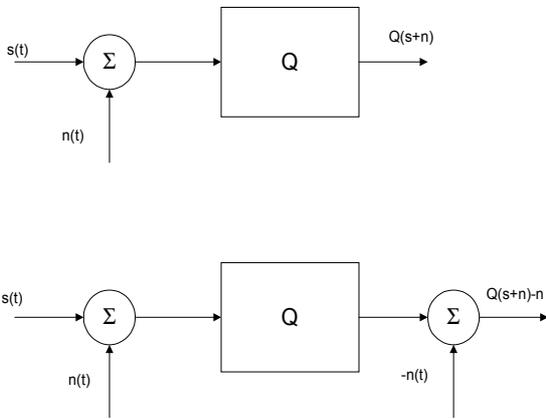

*Fig. 8 Non-subtractive (upper part) vs. Subtractive (lower) dither for ADC (*s – input signal, n – dither signal, Q – ADC and its transfer characteristics)*

Analysing e.g. TEN for different probability density functions of dither signal, it is easy to show that correct convergence is achieved for uniformly distributed dither spanning the exact multiple of quantization step q of ADC. However, normally distributed random signal with RMS value bigger than app. $0.35\ q$ can be used, too. Even harmonic signals with certain amplitude can partially contribute to a resolution/linearity enhancement. This fact leads to an idea to use originally disturbing non-desired signal (e.g. parasitically coupled signal from 50/60Hz power distribution) for dithering. This method is called self-dithering. Aumala [5] developed an interesting tool to analyse and evaluate this case, see Fig. 9.

VIEWPOINT OF MEASUREMENT INFORMATION

It was shown [6,7,8,12] that the enhancement of resolution and linearity is equal for ideal ADC and can be evaluated e.g. by means of the following approach:

Dithered quantizer and its characteristics $y(x)$ includes averaging of N samples of digital output of quantizer, which has a sum of measured signal x and generated noise d as its input. Let's have uniformly distributed noise d of range *(-D,D)*. It can be shown that for correct convergency D must fulfil

$$D = k.\frac{q}{2} \qquad k \text{ integer} >0 \qquad (1)$$

where q means quantization step. Normally distributed noise with RMS bigger than $0.35q$ is also suitable. The effective number of bits of ideal dithered quantizer can be predicted using formula

$$_0 n_{\text{eff}} = n + \log_2(N) \qquad (2)$$

for uniform dithering using deterministic signal or

$$n_{\text{eff}} = n + \frac{1}{2}\log_2\frac{N}{1+k^2} \qquad (3)$$

for stochastic dither signal, where n_{eff} is effective number of bits achieved by averaging of N samples of signal and n means nominal number of bits of used AD converter. For normally distributed noise the value of k must be calculated the following way

$$k = \frac{U_{rmsn}.2^{n+1}.\sqrt{3}}{FS} \qquad (4)$$

U_{rmsn} means RMS value of additive noise [V] and *FS* is the full scale of AD converter [V].

For DAC parameters improvement, the approach is identical but the dither signal has to be digital and the filter mechanism is of course analogue (passive or active LP or BP filter).

The (syntactic) measurement information [6] may be calculated by multiplying the number of effective bits with the frequency of generated independent results. Because independent results within the total uncertainty can be available at a pace of averaging time, the bandwidth is taken here as the inverse of the averaging time
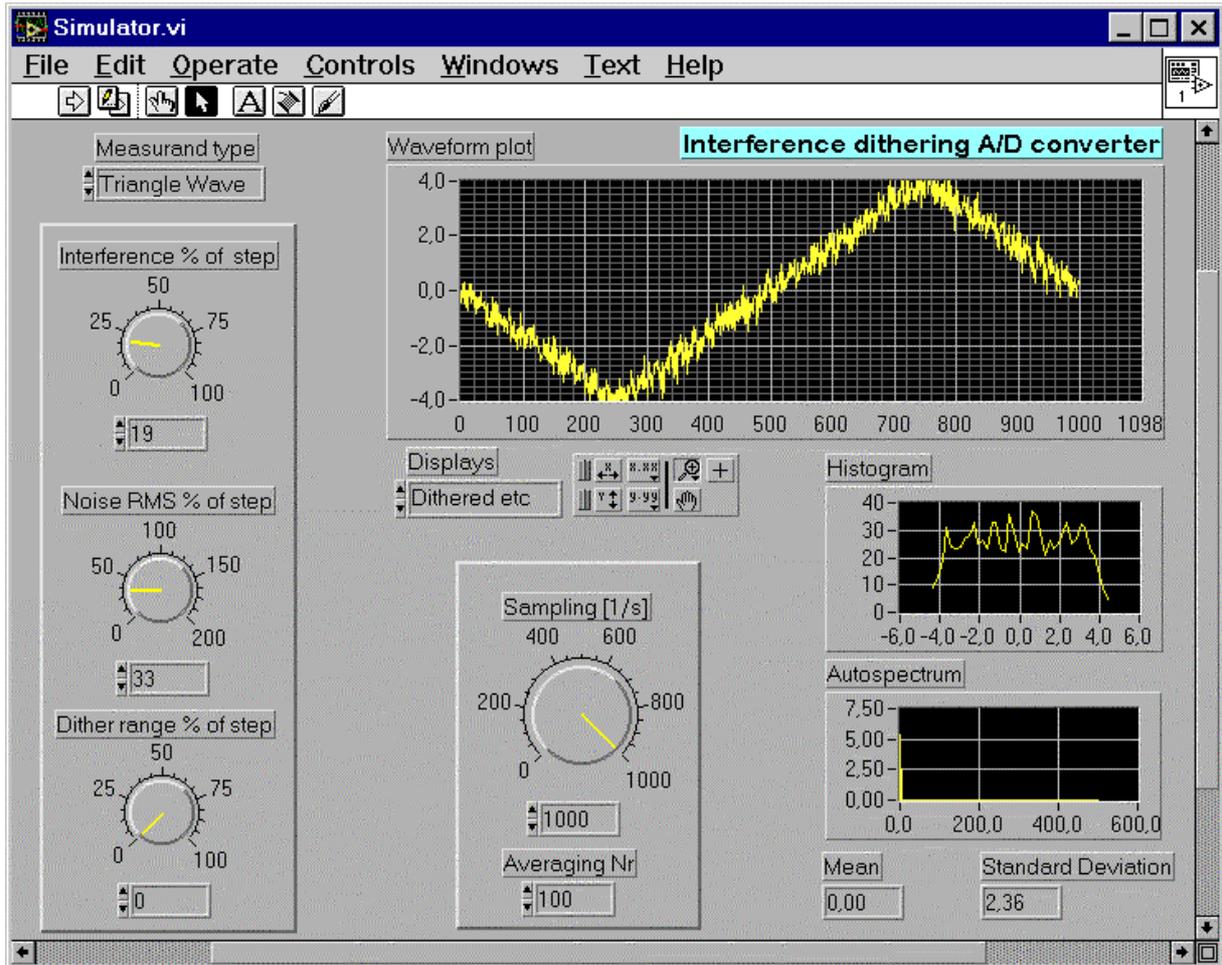
Fig. 9 – A simulator tool to analyse dithering. On the left side, setting devices for the measurand type and for the parameters of the dither signal. Down in the centre, setting of sampling and averaging. All displays present the signal and its parameters chosen by the switch under the main display window

$$B = \frac{f_c}{N} \qquad (5)$$

where f_c is the sampling frequency.

Fig. 10 presents graphically the abovementioned cases for a commercial 10 bit converter. The values n_{eff} can be read on the left hand side scale. The figure contains also data for the channel capacity.

One can see immediately that the channel capacity depends mainly on the bandwidth. If the channel capacity is important, dithering should be restricted to the minimum needed.
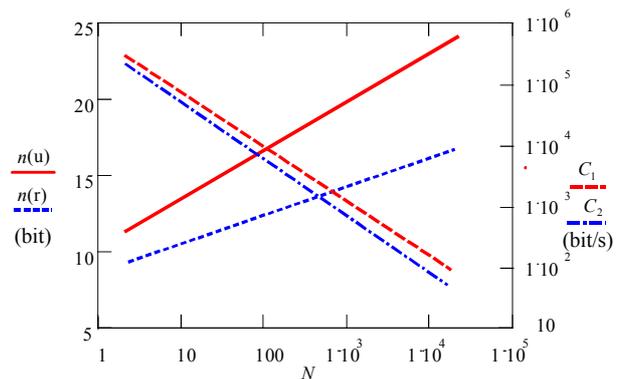

Fig. 10. Dithering increases the effective number of bits n_{eff} of an A/D converter. A/D board resolution 10 bits, conversion rate 80 kS/s. n(u) standard dithering (-q/2, q/2), n(r) dithering with normally distributed noise, $\sigma_{noise} = 0,7\ q$. N is the averaging number. C_1 channel capacity of the standard dithering case, C_2 for the normally distributed noise dithering.

DITHER APPLICATION
FOR REAL ADC

Various types of errors additionally affect the transfer characteristic of a real ADC. Besides offset and gain error, the following standard description methods [10,11], Differential Non-linearity (DNL) and Integral Non-linearity (INL) should be mentioned. Moreover, all those parameters usually vary with input signal frequency. One should have in mind that also the gain and the offset usually drifts with time, temperature changes etc.

Therefore, there are certain limits in case of a dither application to real ADCs (DACs). First, the dithering reduces only some types of errors. With certain portion of simplification it can be stated that errors at scales up to the dither span (which usually are quantizing error, DNL and part of INL) are decreased while errors at scales larger than the dither span are left (major part of INL). Also gain and offset, if they are not eliminated by other methods can not be decreased by dithering. Useful tools to analyse this problem and predict the result of dither application for certain ADC with known DNL (and consequently also INL) are multi-scale analysis

methods like Continuous Wavelet Transform (CWT). Holub and Smid [12] give an example of such approach – see Fig. 11.

Multi-scale approach can be extended by the following idea: Because for certain types of ADC (e.g. flash or successively approximating ADC) the large-scale errors are satisfactorily stable in time, they can be decreased by additional mechanism (look-up or correction table). This idea was presented by Holub and Smid [12], see Fig. 12.

The practical results depend certainly on the particular ADC type used. The theoretical resolution can be enhanced above any given limit by increasing the number of samples to be filtered/averaged. However, in practical cases the linearity (Effective Number of Bits, ENOB) could not be increased more than 1 or maximally 2 bits above the original ENOB. The result is very often still lower than the nominal number of bits of the used ADC. Additional Large Scale Error (LSE) elimination mechanism allows additional one or two bits achievement in ENOB. Nominal number of bits can be overcome. For practical example of test results of embedded ADC on chip of 80C552 micro-controller, see Table 1.
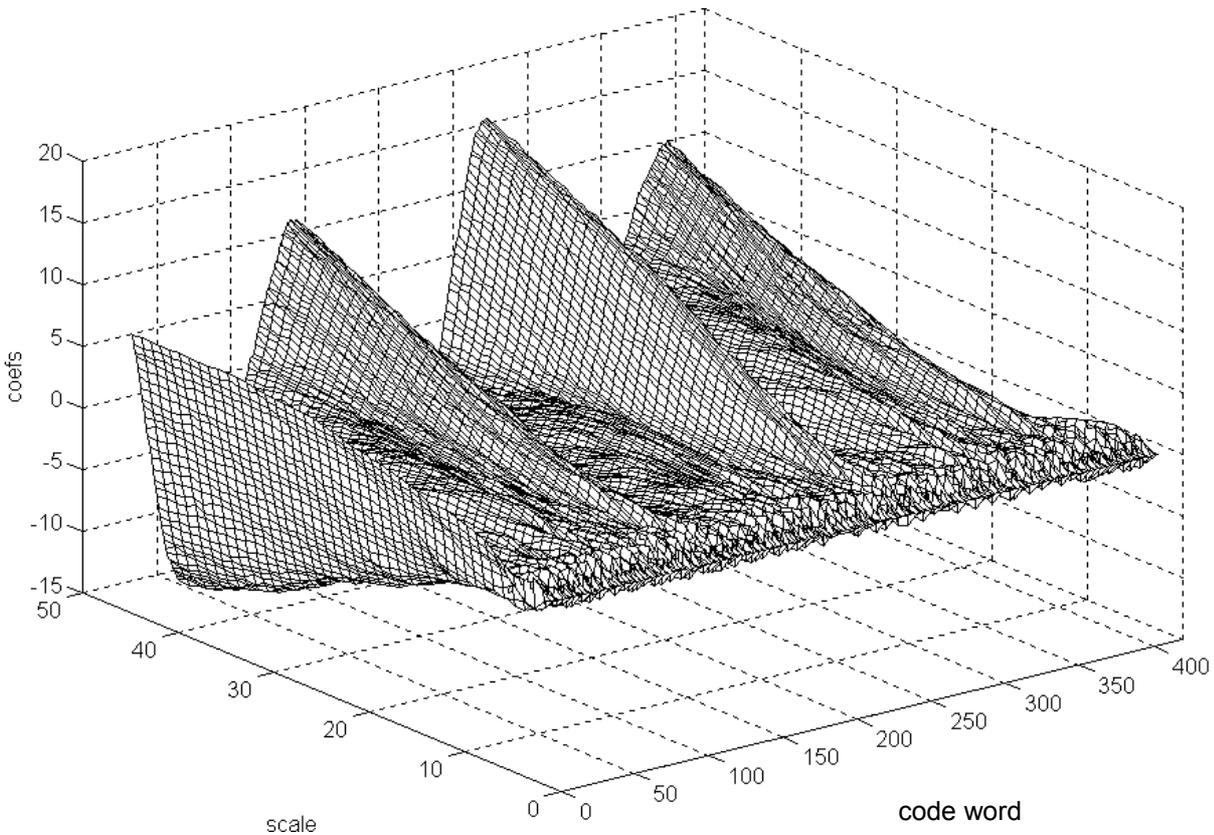

Fig. 11 CWT application for ADC transfer function error

Table 1. The comparison between original and enhanced parameters (16b-res.) of ADC (on chip 80C552)

	ORIGINAL ADC	DITHERED ADC	DITHERED ADC WITH *LSE* REDUCTION
Input Full Scale [V]	5	4.98	5
(Effective) Sampling Rate [Sa/s]	12000	8	8
Output code length [bit]	10	16	16
Effective Resolution [bit]	9.8	15.4	15.4
ENOB [bit]	9.20	11.52	13.97

Another difficulty follows from the time and temperature variations of a LSE. An analysis of these drifts has to be provided in advance and proper type and frequency of (self-) calibration has to be designed. The result can be that too frequent auto-calibrations disable the meaningful application. Also the time duration of the calibration cycle has to be considered. Histogram test methods take much more time than the FFTcalibration method that was proposed by [13].
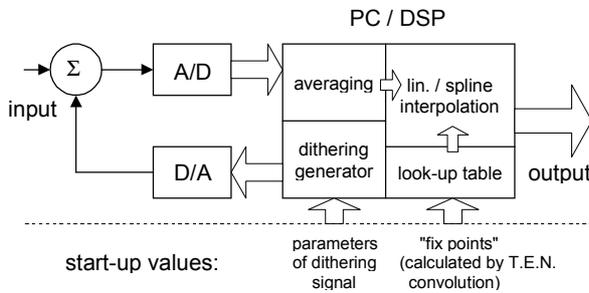

Fig. 12 Additional large scale error reduction - dither application for ADC

After certain portion of experiments in this research area, it can be easily stated that ADC models that do not reflect various errors and their drifts are useless for practical results prediction. The ideal ADC model should serve just for derivation of the basic equation and should be left during any project/device design as soon as possible.

On the contrary, there are some critical voices that seem to be surely wrong: Those are so called "deterministic scientist voices". They use to say: "All the methods that allow any smallest amount of uncertainty caused by random variables or that are based on averaging of stochastically dithered results have to be forbidden. It is obvious that dither does not reduce maximum possible error but only its mean value!"

The above mentioned caution is partially right. An example: When averaging thousand of random samples acquired from a signal that is uniformly distributed in the interval (–1, 1), there is of course a certain probability that all of them will be of higher value than 0.5 even if the signal is independent over infinite observation time. Fortunately, probability of such effect (that would cause significant error when such signal is used for dithering) is comparably small to the probability that the dithered ADC will be destroyed by asteroid during the measurement…

Some situations are really suitable for dithering application. A good example is the case when a relatively fast ADC is used to convert a steady state or slowly varying signal (e.g. temperature signal coming from sensor/system with a significant time constant). Another suitable opportunity occurs when the output signal from an ADC is used just to be shown on the screen or a LCD display of the device – the human eye does not appreciate a faster update rate than 3-5 values per second anyway. A time spare achieved by this knowledge can be easily used for dithering to convert ADC speed to resolution/linearity enhancement.

CONCLUSIONS

Dither can significantly improve quality parameters of various sensors, actuators and converters. General study approaches have been published in recent years. However, each practical application requires careful and detailed analysis to guarantee successful and reliable dither application.

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