

# A DSP BASED TEST SYSTEM FOR 'NOISE-SEPARATION' MEASUREMENTS ON ADC AND DAC SYSTEMS

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**Abstract** - This paper describes the design and application of a 'noise-separation' test system that uses in-system programmable logic devices and a digital signal processor. This offers a low cost approach to multi-tone testing of the wide-bandwidth linearity of both ADC and DAC systems. As the test signal bandwidth is software configurable and uses 1 bit D-A converters it can be applied to a much wider range of applications than more conventional multi-tone test methods. Time-domain processing is expected to provide meaningful results for routine tests in a much shorter time than with FFT analysis.

Keywords: ADC, DAC, routine tests, multi-tone testing, NPR testing.

## 1. INTRODUCTION

The linearity performance of analogue to digital conversion (ADC) and digital to analogue conversion (DAC) systems is traditionally measured using the 'harmonic separation' of a sine wave (also known as total harmonic distortion). Wideband measurements are time intensive and in broadcasting applications noise is recommended as a test signal for wide-band testing [1]. This test produces a 'noise-separation' figure. In telecommunications noise is used as a test signal for measuring cross-talk as sine-wave tests at peak level would cause power loading problems. In telecoms this test is known as a Noise Power Ratio or NPR test.

The sensitivity of NPR and noise separation measurements is limited by the stop-band performance of the analogue filters used. Pseudo random noise has been used as a test signal for NPR measurements as the results are more repeatable than when random noise is used. Conventionally a multi-level test signal is produced digitally and a multi-level DAC is required to reproduce the analogue test signal. A digital notch filter can be used to insert a spectral gap in the test signal but the performance of this DAC limits the degree of 'band separation' in the test signal. NPR measurements can be applied to testing ADCs but resolution is limited by analogue filter performance.

A novel method for noise-separation measurement testing of analogue systems was devised by the British Broadcasting Corporation (BBC) [2]. This avoided the

need for analogue band separation filters and DACs by using two interleaved pseudo random noise test signals that required only two-level signals and no DAC. This is similar in concept to oversampling as an analogue low pass filter is used to convert the two level signal to a multi-level test signal. This BBC test signal has been applied to testing the linearity of ADCs [3]. The experimental equipment devised by the BBC used discrete logic, delta modulation and delta modulation based comb-filters and was designed only for audio bandwidth.

The design and application of a noise separation test system that uses in-system programmable logic devices and a digital signal processor was undertaken at the University of Wales Swansea as collaborative project with Signal Conversion Ltd. This paper describes the aims of the work and progress. As the project is ongoing, further conclusions and results will be presented at the ADDA\_EWADC 2002 Conference.

## 2. THEORY

The British Broadcasting Corporation devised a test based on the use of two signals with interleaved spectra. Each signal consists of harmonics and the fundamental frequency of each signal is selected to ensure interleaving in the frequency domain. Standard signals that meet this specification, such as square and ramp signals have harmonic amplitudes that reduce with harmonic frequency. The amplitude probability function of the combined test signal can be selected by the choice of the two test signals.

In applications where a Normal distribution is required (e.g. audio and telecoms.) the two signals can each be generated from a pseudo random binary sequence (PRBS). A key property of a PRBS is that, provided the PRBS clock rate is more than ten times the test signal bandwidth, the one bit code from the PRBS can be low-pass filtered and this produces a multi-level signal without the need for a DAC. It is also in theory possible to use a digital low pass filter to regenerate the multi-level signal but this then requires a multi-level DAC to reproduce the signal and the test signal 'purity' and bandwidth is limited by the DAC performance.

### 3. AIMS

The primary aim was to achieve the same performance as the experimental noise-separation test apparatus provided by the BBC. This was a 19 inch rack system with the signal generator requiring one unit and the test signal analyser requiring another unit. The BBC system used discrete logic with fixed clock rates and 15 kHz test signal bandwidth. This test system was used for both research and operational tests in BBC studios but the hardware it was relatively expensive. A lower cost test system would facilitate its wider use and also make it available to the professional audio market. Its key benefit for the professional audio market is that it has been demonstrated to be able to measure audio quality with reliable results. This is not possible with any other audio test method.

In addition, it has been shown to be possible to use the noise separation test to measure wideband parameters important to ADC and DAC applications. As it is desirable to be able to test video bandwidths a further aim of this project was to provide a selectable test signal bandwidth that tracked the sampling rate of the ADC or DAC under test.

To achieve this aim it is necessary to consider three alternative approaches to the design of the signal analyser.

- discrete logic using a field programmable gate array (FPGA)
- a Digital Signal Processor could be used for the test signal analyser.
- PC based analysis.

It was clear that the best approach for the test signal generator was to use an FPGA.

The project team at UWS undertook in parallel the three tasks of PC based simulation and analysis, FPGA based design and DSP based design.

### 4. THE PROJECT

The previous section outlined the tasks and this section will describe them in more detail. Fig. 1 shows the spectrum required from the test signal generator.  $T_1$  and  $t_2$  are the repetition periods of the PRBS generators.

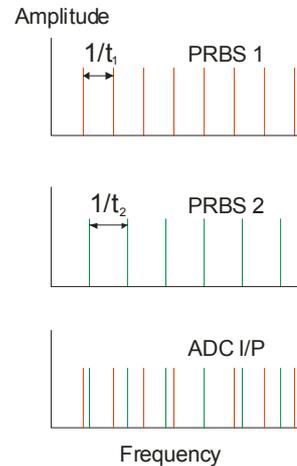


Fig. 1 Spectrum from test signal generator

When this test signal is applied, for example to an ADC, intermodulation products are generated and these fall in the spectral gaps as show in the ADC output spectrum of Fig.2.

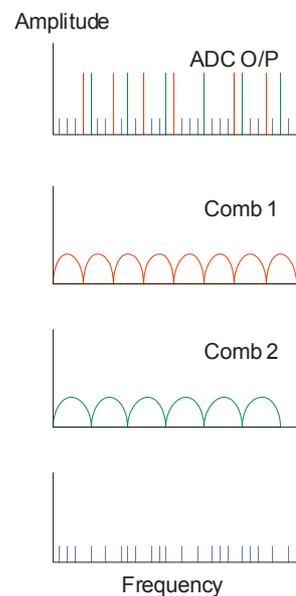


Fig. 2 Spectral processing in test signal analyser

Fortunately, the harmonic spectrum of a PRBS signal can be removed completely with a simple comb response filter. Two such filters in cascade can therefore remove the test signal completely. The remaining signal is due to the ADC quantisation, noise and non-linearity.

#### 4.1 Test signal generator

An in-system programmable (ISP) logic device was used to generate the two PRBS signals and their clocks. Initial simulations were compared with the PRBS test signals in the BBC unit using a logic analyser. This assisted in validating the design and this part of the project was relatively straight forward. A block diagram of the generator is shown in Fig. 3.

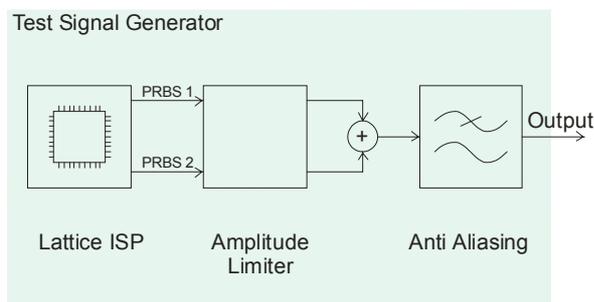


Fig. 3 Block diagram of test signal generator

From Fig. 3 it can be seen that there are three ‘analogue’ components: the amplitude limiter used to define the amplitude values of logical 1 and 0, the summing circuit, and the low pass filter and output amplifier. It is these circuits together with the tracking clock generator that provide the technical challenges. Options under study include both active and passive analogue designs as each will provide different tradeoffs between linearity, bandwidth and complexity. The tracking clock generator must produce the two clock signals for the PRBS registers and this clock signal must be locked to a multiple of the ADC or DAC data sampling clock. This presents an optimisation

provides the required PRBS clock frequencies and is a multiple of the ADC clock. This problem is under investigation and results are to be reported.

#### 4.2 Test signal analyser

The DSP platform chosen for the analyser was a TMS320 family development system or DSK. A block diagram of the analyser is depicted in Fig.4. Earlier sections of this paper have described the need for the comb filters and spectral analysis. Both these functions are conventional ones. Data from the comb filters is processed in both frequency (FFT) and time domain (quasi-peak amplitude). Software to produce quasi peak results and the interpolating filter requires experimental verification as the end result must be compared with that from the BBC test system. The challenge here is to choose an optimum oversampling ratio for the digital interpolating filter. It must be high enough to provide accurate placement of the comb filter notches. If it is too high the DSP will not be able to complete its operations and this will limit the maximum useable ADC sampling rate. Data is transferred to a host PC for display and comparison.

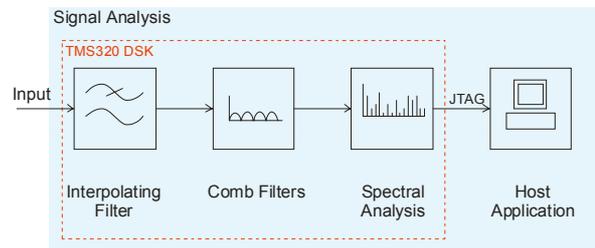


Fig. 4 Signal analyser

#### 4.3 Test system

Fig. 5 below depicts an ADC under test using the PRBS signals and DSP based analyser

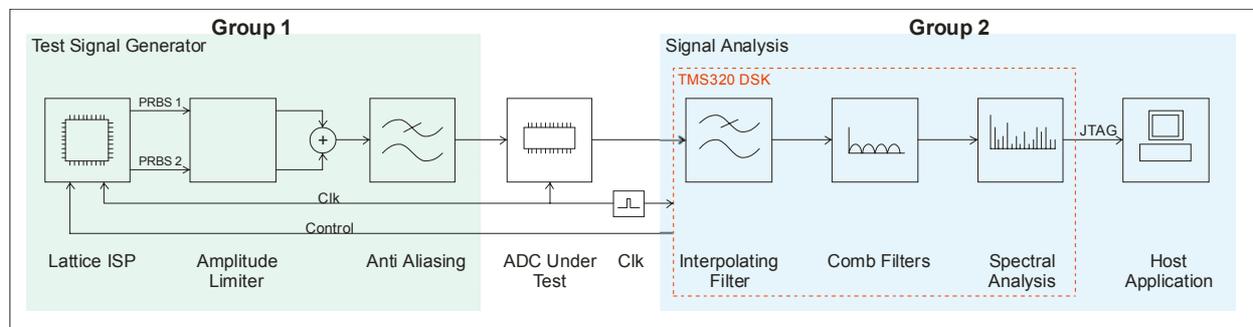


Fig. 5 ADC test system

problem. What is the lowest multiplication factor that

In this project, Matlab simulations were undertaken to investigate the optimisation of the clock generator design, interpolating filter and quasi peak measurement.

This work used Simulink and the PRBS signals were modelled using digital logic functional blocks. Data files with the combined PRBS signals were generated and frequency and time domain displays were used to check the performance of signals from the test hardware. This provided independent confirmation of the operation of the ISP program and help to resolve an ambiguity in the documentation for the BBC test system.

## 5. RESULTS

The following figures illustrate the results so far.

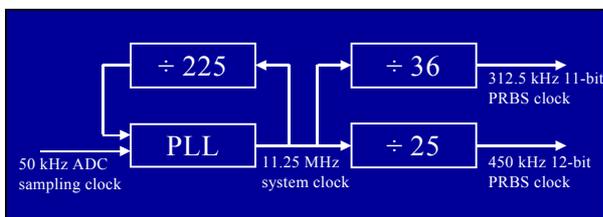


Fig. 6 clock generator

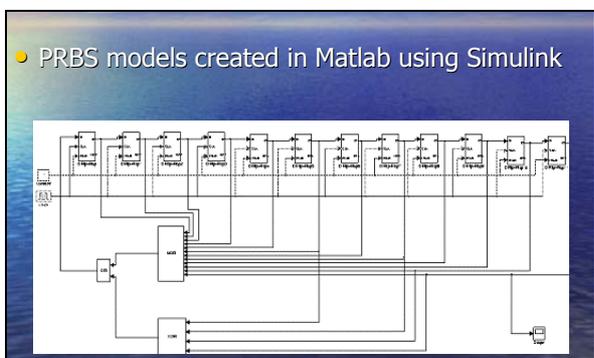


Fig. 7 Simulink

## 6. FUTURE WORK

The DSP based test system will be used to evaluate the performance of the ADC included in the TI DSK. A computer model of the ADC linearity error will be produced for the Matlab simulation and this used to estimate the minimum time needed to measure the quasi peak value of the distortion signal. Results from the simulation will be used as a cross check with results obtained from the DSP based test system and recommendations formulated to enable other researchers to make use of this test procedure.

## 7. CONCLUSIONS

This paper has outlined work aimed at providing a more flexible and readily implemented version of the noise-separation test method. It has addressed problems of synchronising the test signal with the ADC sampling clock and digital filters. An interpolating filter facilitated the increased frequency resolution required to align digital comb filters with the test signal. Experiments are in progress to determine the circuit arrangement that proves the widest bandwidth of operation.

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