QUALITY ASSURANCE AND TESTING OF THE ATLAS LIQUID ARGON CALORIMETER POWER DISTRIBUTION BOARDS

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Abstract:

During the second Large Hadron Collider Long Shutdown, the Liquid Argon calorimeter of the ATLAS experiment at CERN has been upgraded with a new trigger readout electronics which provides digital information with higher granularity to the ATLAS trigger system. In particular the new LAr Trigger Digitizer Boards will process and digitize the "Super Cells" (group of readout calorimeters cells) and send the processed data to the back-end electronics. The Power Distribution Board is a mezzanine board that provides the power distribution to the LTDB.

Keywords: Large Hadron Collider; ATLAS; Liquid Argon Calorimeter; Power Distribution Board.

1. INTRODUCTION

The ATLAS detector [1] at the CERN Large Hadron Collider (LHC) [2] is a multipurpose particle detector, optimized to exploit the full physics potential of high-energy proton–proton (pp) and heavy-ion collisions. This includes the study of the properties of the Higgs boson, precise measurements of Standard Model processes and searches for rare and new phenomena. The ATLAS detector at the LHC covers nearly the entire solid angle around the collision point, and consists of an inner tracking detector surrounded by a thin superconducting solenoid, electromagnetic and hadronic calorimeters, and a muon spectrometer incorporating three large superconducting toroidal magnets. In total, ATLAS has over 100 million electronic channels, which provide readout from these detectors. After the 2015-2018 data taking campaign (Run 2), an upgrade plan (Phase-I upgrade) started to enhance the physics reach of the experiment during the upcoming operation at increasing LHC luminosities (Run3, started in 2022). In particular, for the liquid argon calorimeter, to avoid efficiency losses and enhance the physics reach, it was decided to increase the trigger readout granularity by up to a factor of ten, summing the the transverse energy (ET) of calorimeter cells in areas smaller than the previous configuration (these smaller clusters of cells are called Super Cells). In addition, the precision and range of the ET measurement is also increased [3]. The Lar Trigger Digitizer Board (LTDB) processes and digitizes up to 320 Super Cell signals and transmits them via optical links to the Back-End. Power distribution on the LTDB is provided by the PDB mezzanine card. The choice of developing a separate board for the generation of the supply voltages for the LTDB ensures forward compatibility in the future Phase-II upgrade, for which a different power distribution scheme for the Front-End electronics is planned. The Power Distribution Board (PDB), mounted on the LTDB, uses some of the existing supply voltages as input and converts them to the needed values using LTM4619 DC/DC converters (from Analog Device, Inc.) for the digital part and LHC4913 (positive voltage) and LHC7913 (negative voltage) regulators (from STMicroelectronics) for the analog part. All the PDB produced have been tested in Milano by a custom test board, internally designed and manufactured, controlled by an Arduino. Thanks to this set up we were able to test, automatically, all outputs of the LTMs and LHCs, and in particular the output voltage and noise. The power supply, connected to the test board, powers the PDB that is placed on the board. A circuit mounted on this board allows to test the output voltage of the DC/DCs either with no load or with load, in order to simulate the load that will be connected to the PDB when it will be mounted on the LTDB.

2. THE POWER DISTRIBUTION BOARD (PDB)

The PDB is composed by digital and analog parts to power the corresponding sections of the LTDB. The block diagram of the power scheme is shown in Figure 1.

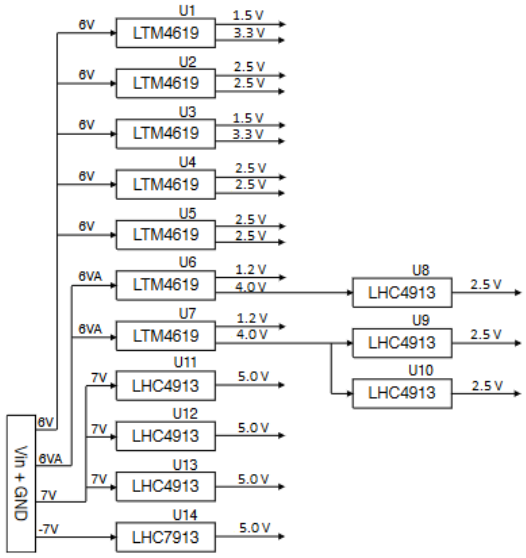

Figure 1: Power scheme of the PDB. The board integrates LTM4619 DC/DC converters (U1-U7) and LHCx913 linear voltage regulators (U8-U14) to produce the voltages needed by the LTDB (the number of devices has been established based on the budget of the output currents). From the two +6 V lines available on the input power bus, one (labelled "6 V") is used to generate the digital voltages and the other one "6 VA" is used to generate the analog voltages. Picture from [3]

From the +6 V line taken from the Front-End Crate (FEC) power bus, the following voltages are created for the digital part of the LTDB: +1.2V, +1.5V, +2.5V and +3.3V. This is achieved using LTM4619 DC-DC converters. This is a DC-DC μModule regulator operating over input voltage ranges of 4.5 V to 26.5 V and supports two outputs with voltage ranges of 0.8 V to 5 V. It delivers 4 A continuous current (5 A peak) for each output. The analog voltages are generated as follows. From the +7 V(-7 V) of the FEC power bus, the +5 V(-5 V) is generated using the LHC4913 (LHC7913) Low-DropOut (LDO) linear voltage regulator. The LHC4913 is a positive Voltage Regulator that has a fixed output voltages: 2.5 V, 3.0 V, 3.3 V, 5.0 V or 8.0 V and an input voltage ranging from 3 V to 12 V. The LHC7913, instead is a negative Voltage Regulator with an input voltage range from -3 V to -9 V. The LHC4913 is also used to generate +2.5 V, starting from the +6 V of the power bus, (with an intermediate step down at +4 V, using an LTM4916, to avoid a large voltage drop on the LDO). The PDB is radiation tolerant [4]-[6] and able to operate in presence of maximum magnetic field expected in the LTDB position (lower than 0.1 T) [7]. The radiation tolerance requirements for the PDB are less stringent than for the rest of the LTDB component since the board will have to operate only for the LHC Run 3 and will be replaced before the start of the HL-LHC. The board is manufactured as a ten-layer PCB of 1.6 mm thickness, reinforced with a fiberglass (G10) frame glued on the top side. When mounted on the LTDB motherboard, the total maximum vertical height is about 5.4 mm. One PDB is show in Figure 2. An automated set-up has been developed to test the correctness of all output voltages of the PDBs at full load before they were shipped to LTDB assembly site. The PDBs passing the tests above are then subjected to a highly accelerated stress screening (HASS) test, where the PDBs are placed in a chamber and undergo ten thermal cycles between 0 °C and 60 °C for about 12 hours. The goal of the HASS test is to find any failures due to component infant mortality, cold solder joints, etc. After HASS testing, each PDB is installed on an LTDB for re-testing, where the voltage of all outputs is measured, control and monitoring signals are tested, and the power rail ramp-up time (from 10 % to 90 % of the rising edge) for the GBTx [8] is measured as well. If the PDB passes this re-testing, it can be used on the LTDB for integration testing. A picture of the PDB mounted on the LTDB is showed in Figure 3. A first preproduction batch of 50 PDBs was produced, followed by a production batch of 150 boards, which included the 128 boards needed in the experiment and some spares.

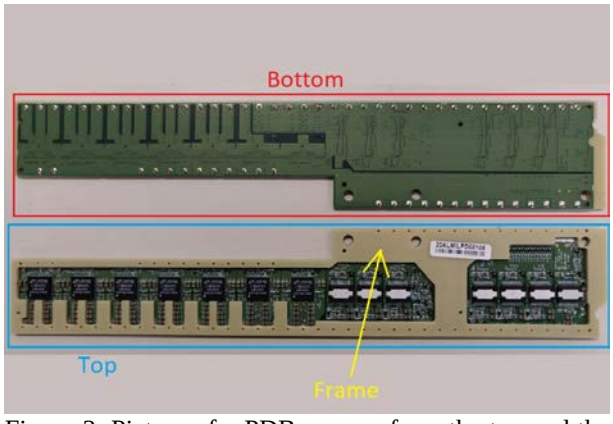

Figure 2: Picture of a PDB as seen from the top and the bottom. All components are mounted on the top side. On the same side, the G10 reinforcement frame is also visible. Picture from [3]

Figure 3: Picture of the PDB mounted on the LTDB. The PDB is located on the right side of the picture. Picture from [3]

3. QUALITY ASSURANCE, CONTROL AND TEST SETUP

The LTDB quality assurance and control (QA/QC) involves the testing of three main components: the cooling interface is tested for leaks, the PDB are tested to meet the requirements on voltage and current of the outputs, and each LTDB with a qualified PDB installed is subjected to functionality testing and - integrated with the test stand - to performance testing as detailed below. Each PDB module is tested with a standalone test stand to verify basic functionality before it is cleared to be installed on an LTDB motherboard. The input and output voltages and current are measured to obtain efficiency information. All test data and analysis results are examined and logged into a database. A PDB module is accepted if it passes the following requirements: the output voltage is within ±2.5 % of the nominal value; the output voltage ripple is within 10 mV peak-to-peak; and the efficiency is better than 70 % at nominal load. All PDBs were tested in university of Milano by an automated method before being shipped for further testing steps. All the PDBs have label with an unique code figure 4. In this way any action on the PDBs can be catalogued and we can check the action done on any PDB. The tests focused, primarily, on verifying that all controller outputs met specifications. The setup for these tests essentially consists of a board for testing a single PDB, which is powered by the power supplies described in the previous section. Each output of the PDB is connected to a resistive load that simulates the actual load after installation in the experiment. Through an additional electronic circuit and an Arduino, all output voltages are controlled both at no-load and load in a sequential way.

Figure 4: Label example on a PDB. Any PDB has a barcode that is a unique code.

4. TEST RESULT

An example of the data acquired on a PDB by automatic procedure is shown in Table 1. In the first column of the table 1 are show the name of the outputs, in the second the output voltage without load, and the third the output voltage

Table 1: Example of a data taking on a PDB of each output both with and without load

PCB number: 002-007 04-20 **Board number: 20ALMILPD00113**		
Output	**No load**	**Load**
LTM1-1V5A	1.514 V	1.508 V
LTM1-3V3	3.354 V	3.348 V
LTM2-2V5A1	2.549 V	2.545 V
LTM2-2V5A2	2.544 V	2.539 V
LTM3-1V5B	1.515 V	1.507 V
LTM3-3V3B	3.352 V	3.348 V
LTM4-2V5B1	2.545 V	2.545 V
LTM4-2V5B2	2.550 V	2.531 V
LTM5-2V5B3	2.549 V	2.539 V
LTM5-2V5B4	2.541 V	2.535 V
LTM6-1V2ADCA	1.219 V	1.218 V
LTM7-1V2ADCB	1.250 V	1.245 V
LHC1-2V5ADCA	2.578 V	2.528 V
LHC2-2V5ADCB1	2.574 V	2.550 V
LHC3-2V5ADCB2	2.524 V	2.519 V
LHC4-5VA1	2.514 V	2.520 V
LHC5-5VA2	2.534 V	2.534 V
LHC6-5VA3	2.551 V	2.554 V
LHC7-5VAN	2.353 V	2.352 V

with load. The last 4 LHCs present an output at about 5 V. To test the output of these regulators, it was necessary to insert an auxiliary circuit, a voltage divider, to decrease the output voltage so that it could be read with the Arduino. This device has a limit on the input voltage on the analog channels equal to the supply voltage of the Arduino board. Since the voltage of the last 4 LHCs is close to this value we could have some reading errors and therefore it was decided to adopt the voltage divider solution. All boards mounted within the experiment were tested with this setup and checked, one by one, to see if the voltage requirements of the outputs were met. Table1 shows an example of a PDB tested with this system and shows the output voltage values of individual components with and without resistive load. Each value was measured by taking the average of 100 values. Noise tests were also added. A sample of boards were chosen to test the RMS noise of DCDCs and regulators. Figure 5 shows a histogram that compares the RMS distribution for the 2.5 V obtained from the LTM4913s (output U2, U4, U5) and LTM 4619s (output U8, U9, U10). The signal output from the LHCs appears to be less noisy than that output from the LTMs. The measurement were done with a true RMS voltmeter (Rohde & Schwarz URE3 30MHz RMS/Peak Voltmeter) with 2 MHz bandwidth and includes the data of 9 PDBs.

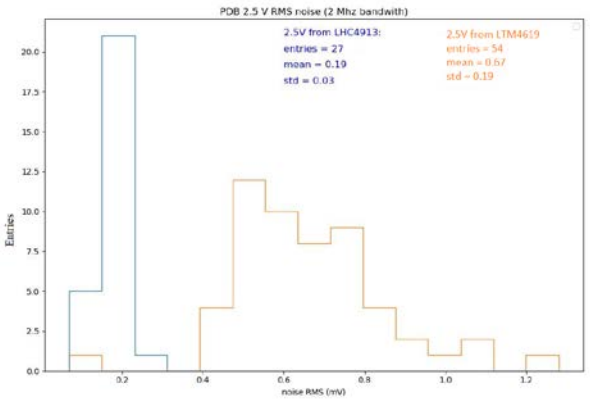

Figure 5: Histogram of noise RMS of LTMs and LHCs 2.5 V outputs

The other outputs of the LTMs and LHCs were also tested and found to have noise compatible with those shown in Figure 5. Other tests were done to verify the noise spectrum of LTMs and LHCs. Figure 6 shows the noise spectrum of an LTM that outputs 2.5 V. One can see the peak of the first harmonic around 775 kHz with an amplitude of 49.88 dBμV. This frequency corresponds to the switching frequency of the DCDC. Figure 7 show the noise spectrum of an LHC with 2.5 V outputs. The amplitude of the 775 kHz peek is reduced to 35.98 dBμV. These noise tests were not conducted as necessary for quality assurance purposes, but for further control about the quality of the components mounted on the boards. These tests were not performed on all components on the boards but on a sample. For example in Figure 5 the obtained experimental results on 27 LHCs and 54 LTMs are depicted.

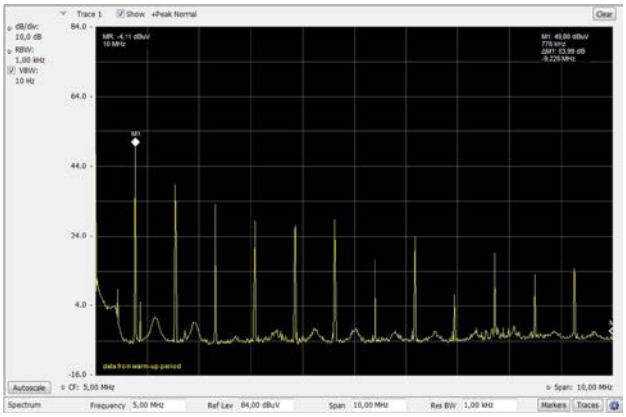

Figure 6: Noise spectrum of LTM4913 with 2.5 output voltage

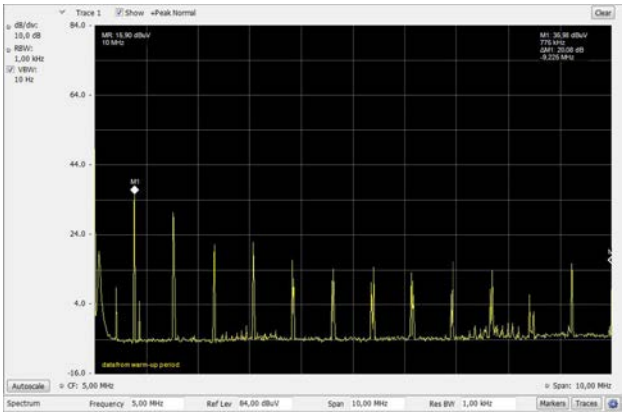

Figure 7: Noise spectrum of LHC4619 with 2.5 output voltage

5. SUMMARY

This paper gives a brief overview of the tests performed for the production of the power distribution mezzanine of the new trigger board of the ATLAS liquid argon calorimeter. The board, the test setup and the list of tests performed are presented. Results of the noise performance of the board are also presented. All the needed boards have been produced, installed on the trigger board, and successfully commissioned

6. REFERENCES

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