

Integrated model environment for digitally controlled power converter analysis and diagnostics

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Abstract – In this paper an integrated model environment is demonstrated which makes it capable to develop control, fault detection or state estimation algorithms for digitally controlled electric drives. Due to the mixed-signal platform it is possible to test and validate the developed methods. In this work a capacitor degradation phenomenon has been investigated which simulates a failure in a PI regulated Buck DC-DC converter.

I. INTRODUCTION

The electromechanical energy conversion system consists of a power converter, an electric machine fed by the converter and a digital controller which regulates the entire system. The PWM operation of the power converter generates harmonic currents and voltages which cause passive component overheating. The operation at increased temperature leads to component aging and wear-out faults.

The performance of the regulated electric drive can be improved by augmenting the digital control system with a fault detection algorithm.

II. INTEGRATED MODEL ENVIRONMENT

The microcontroller regulated electric drive system or just taking into consideration a part of these systems, the digitally controlled power converters are mixed-signal systems containing both analog and digital signals. In order to analyze these systems close to realistic behavior it is worthy to design and to model the analog and digital subsystems separately. The electric part of the system can be modeled properly in a circuit design environment, while the implementation of the digital environment and the control algorithm should be made in an environment capable to run numerical computations. In such a complex development and test environment it is possible to simulate signal conversion and signal processing processes which has a significant effect on the system behavior and generally are neglected.

The results presented in this paper are obtained using OrCAD circuit design environment and

MATLAB/Simulink environment interconnected.

A. Converter modeling

The analyzed power converter is a Buck DC-DC converter. Its specifications can be found in Table 1.

Table 1. Buck converter specifications.

U_{in}	24 VDC
U_{out}	16 VDC
f	20 kHz
i_{out}	5 A
Δi_L	0,5 A
ΔU_C	0,5 V

The power converter was designed based on the given specifications and its model is implemented in OrCAD environment. The designed circuit was extended with additional components in order to model the behavior of the converter realistically:

- resistances for wire modeling,
- capacitor ESR, inductance and parallel resistance [1],
- resistance of inductor

The switching element is an IRF140 MOSFET which is controlled with PWM pulses provided by the digital controller.

B. Digital controller modeling

The digital controller applies a PI regulator with capacitor voltage difference as an error signal at its input. The output of the regulator provides current reference which quantity can be used for duty cycle (D) calculation.

The operating frequency of the converter determines 50 μ s loop time delay, hence a Smith predictor is used for keeping the feedback controlled system stable.

The entire digital subsystem is modeled in Simulink environment in order to represent the microcontroller which supervises the power converter operation (Fig. 1).

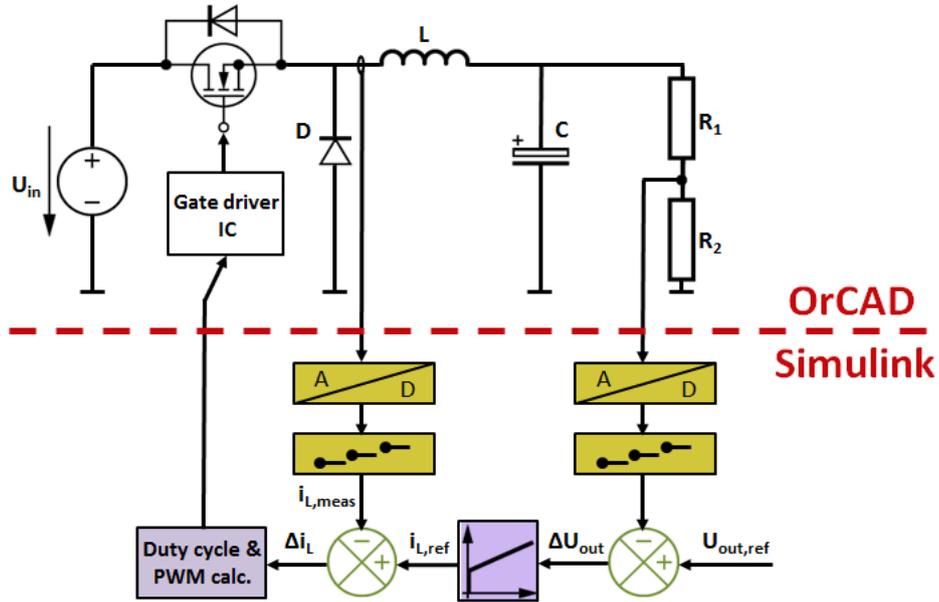


Fig. 1. Integrated model environment.

III. FAULT MODELING OF CAPACITOR

The presented model environment can handle the power converter, the connected load and even the network side phenomena together with the digital controller system. Due to these features the interconnected model environment is suitable for fault analysis, as well.

Faults can occur in several places in such a complex system. Focusing only to the power converter, faults are categorized as sensor faults, conducting part faults, passive component faults and switching element fault.

In this paper a passive component fault is introduced into the power converter, more precisely a capacitor fault has been modeled. Due to the PWM operation of converter and the occurred harmonics the ESR of the output capacitor increases, while the capacitance decreases. In five different steps the capacitor parameters were determined based on -40% change in the capacitance value (C) and 1400% change in the ESR value (Table 2). The parameters were computed applying these rates incrementally.

Table 2. Simulation of fault formation.

	$R_{ESR}[\Omega]$	$C [\mu F]$
1 (no fault)	0.02	12.5
2	0.3	7.5
3	4.5	4.5
4	67.5	2.7
5	1012.5	1.62

Even the capacitor has significant degradation, the catastrophic fault should be avoided. It is sufficient to notice the fault before it causes short-circuit through the capacitor and affects other components. In order to avoid damage it is sufficient to notice faults as early as possible.

This 5 step analysis simulates the capacitor degradation in time and the integrated model environment facilitates keeping track numerous quantities which may vary corresponding to the degradation.

IV. MODEL-BASED FAULT DETECTION

In order to notice faulty state or any kind of component degradation a model-based approach is supposed to be a suitable solution. In this type of fault detection utilizes the comparison of the output quantities of the physical system and the same quantities of the system model. When difference is noticeable between the output of the digitally implemented model and the output of the converter it may be induced by a degradation phenomenon in one of the circuit components.

The mathematical model of the Buck converter is given by (1) state-space averaged model [2], [3].

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dU_C}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ U_C \end{bmatrix} + \begin{bmatrix} \frac{D}{L} \\ 0 \end{bmatrix} [U_{in}] \quad (1)$$

This model does not consider the additional terms such as wire resistances, ESR of capacitor and inductor

resistance. The output vector is identical to the state vector.

A. Discrete-time model

The digital implementation of model based fault predictor needs the mathematical model to be discretized. The discrete-time state-space averaged model can be obtained by considering the (2)-(3) approximation of the discrete-time state and input matrices.

$$\mathbf{A}_d = \mathbf{I} + \mathbf{A}T_s + \frac{\mathbf{A}^2T_s^2}{2} + \dots \quad (2)$$

$$\mathbf{B}_d = \mathbf{B}T_s + \frac{\mathbf{A}B T_s^2}{2} + \dots \quad (3)$$

Using the approximations there is the possibility to consider only the linear parts, or also a quadratic approximation can be performed. Both the linear and the quadratic approximation based model have been implemented. In the discrete form (4) the x_{k+1} state vector can be estimated which contains two quantities: the current of the inductor (i_L) and the voltage of the capacitor (U_C).

$$\mathbf{x}_{k+1} = \mathbf{A}_d \mathbf{x}_k + \mathbf{B}_d \mathbf{u}_k \quad (4)$$

The applied duty cycle is calculated by utilizing the PI controller given inductor reference current (5) [4].

$$D[k] = \frac{L}{U_{in} T_s} (i_{ref}[k-1] - i_{L,avg}[k-1]) + \frac{U_C}{U_{in}} \quad (5)$$

At the end of each $50 \mu s$ switching period the inductor current is sampled at its minimum value, since the PWM on time is applied at the beginning of the period. In order to avoid that the minimum current value to be considered when computing current error signal, it is necessary to calculate the inductor current average value (6), [5].

$$i_{L,avg}[k-1] = i_{L,meas}[k-1] + \frac{U_{out} T_s}{2U_{in}} \frac{U_{in} - U_{out}}{L} \quad (6)$$

This method ensures that the average value of inductor current in each switching cycle follows the reference current determined in the same period.

The state estimation presented in (4) can be implemented introducing (5) and (6). Figure 2 shows that these equations are needed for the duty cycle calculation and also for the state estimation. It also can be seen in the figure that the digital control algorithm is extended by the state estimator to make model based fault detection available.

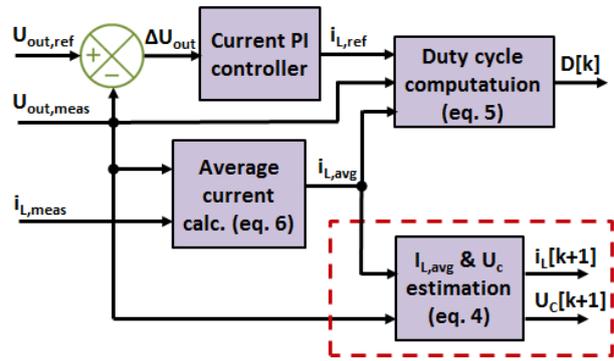


Fig.2. The current control algorithm and the state estimator.

The estimated value of the capacitor voltage and inductor current coincide in steady-state (Figs. 3-4). The second-order approximation does not advantageous, since there is no sufficient difference between the model outputs using linear and quadratic approximation.

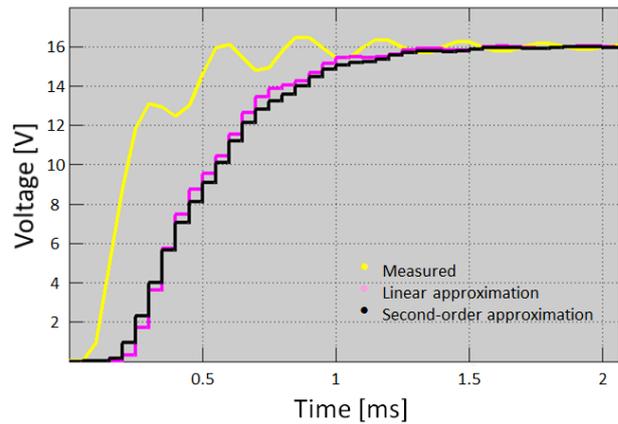


Fig. 3. Output capacitor voltage.

Fig. 4. shows the measured and estimated currents.

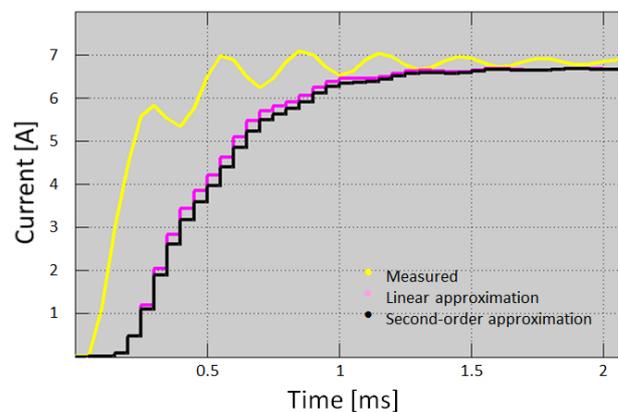


Fig. 4. Inductor current.

B. Tests introducing capacitor degradation

The digitally implemented model of the power converter makes the comparison of the measured and estimated quantities possible.

Performing simulations in 5 steps when the capacitor parameters, namely the capacitance and the ESR were changed based on Table 2; the inductor current decreased. Figure 5 shows the measured inductor current ($i_{L,avg,meas}$), and the estimated current ($i_{L,avg,est}$) with linear approximation. While inductor current has changed, the controller kept the output voltage constant, so the voltage of the capacitor is not influenced by degradation.

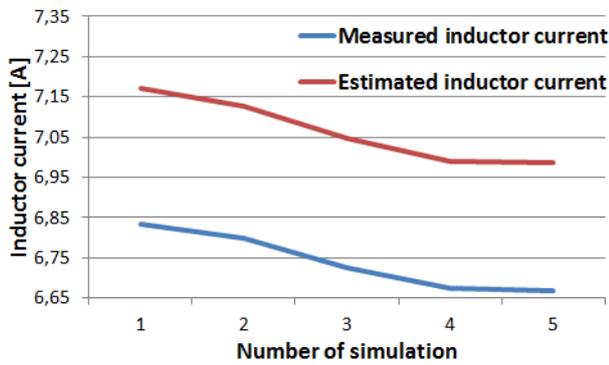


Fig.5. Measured and estimated inductor currents.

The currents presented in Fig. 5 are average currents at different degradation levels. The transient parts of the data were removed when calculating the average quantities. The estimated current in the inductor is greater than the measured, since the model does not consider additional resistances in the circuit. Both quantity decreases with same rate as the degradation level of the capacitor increases.

These results show that observing the difference evolution between measured and estimated current is not suitable to ascertain component degradation.

Furthermore, during the operation of the power converter the resistances can heat up due to the conducted current. It means that the change in the value of the current does not identify unequivocally the degradation of any component in the circuit.

V. DUTY CYCLE BASED FAULT DETECTION

In the digital platform there are two different ways to observe the duty cycle which controls the power converter.

The applied duty cycle is calculated by utilizing the PI controller given inductor reference current, as it was presented in (5).

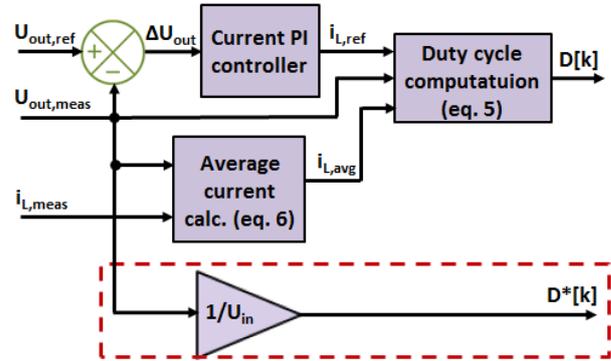


Fig.6. The current control algorithm and the duty cycle calculator.

However, the measured capacitor voltage divided by the input voltage of the converter also determines the duty cycle (7) which should be applied based on this calculation when the Buck converter is not feedback regulated. Figure 6 presents the digitally implemented control algorithm extended by the capacitor voltage based duty cycle calculator.

$$D^* [k] = \frac{U_C}{U_{in}} \quad (7)$$

The simulation of the degradation has been performed using capacitor parameters shown in Table 2, and the duty cycles were recorded at each degradation level. Difference can be noticed between the value of duty cycle determined by (5) and calculated by (7), which can be seen in Figure 7.

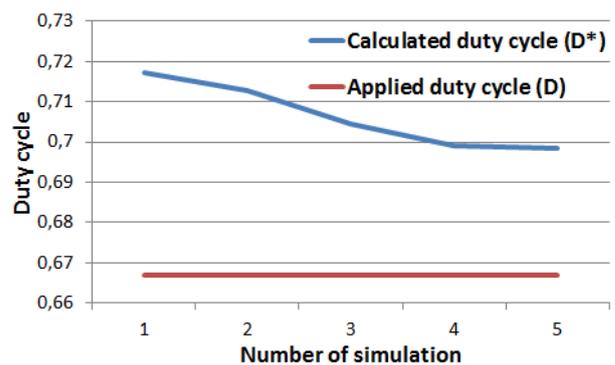


Fig. 7. Duty cycles.

The reference current based duty cycle (D) has the same value in the case of all tests while the duty cycle calculated from the measured capacitor voltage (D*) has significant reduction in its value. The cause of the difference is that the inductor average current value has no effect on the calculation based on (7), only the measured capacitor voltage is considered.

VI. CONCLUSIONS

The model based comparison of observed quantities showed that voltage across the capacitor is not changed when different degradation levels were simulated. Performing the same simulation sequence reduction can be noticed in the value of the inductor current. However, the reason of the decreasing current is not obvious, since converter operation at increased temperature also can be responsible for this.

The duty cycle is suitable to detect component degradation which leads to component fault. The duty cycle calculated from the measured capacitor voltage decreased as the component degradation level increased. The reference current based duty cycle of the switching element had the same value during the five different test simulation. The difference between the two values makes the fault detection and prevention possible, since as the capacitor aging become significant, the difference increases, as well.

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