

Method of Integral Nonlinearity Testing and Correction of Multi-Range ADC by Direct Measurement of Output Voltages of Multi-Resistors Divider

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Abstract-There is developed method of testing points generation for identification and correction of integral nonlinearity of high performance ADC. The developed method is based on averaging all voltages of multi-resistors voltage divider. It is investigated influence of resistors' error and random error of ADC on residual error of integral nonlinearity correction for method based on multi-resistor divider.

I. Introduction

Implementation of computer systems and digital signal processing algorithms in all fields of our life brings that analog-to-digital converters (ADC) becomes the necessary component of modern measurement systems. In some cases the ADC's metrology parameters determines the parameters of whole system. Particularly this is actual for electrical quantities measurement systems. Therefore improving the ADC is actual task.

The market of DC precision ADCs is covered by converters based on sigma-delta modulators SDM [1, 2]. Their high accuracy is provided by implementation the methods of null setting and calibration. These methods provide decreasing of additive and multiplicative components of conversion error. Therefore the error of conversion result is determined by errors of: calibration voltage source, multiplexer and also residual ADC's error. The main significant component of this residual ADC's error is its integral nonlinearity. For example, the maximum allowable integral nonlinearity of 24-bit ADC AD7714 [3] is 15 ppm. This nonlinearity corresponds to 16-th bit so, in the worst case the 8 least significant bits are a priori inaccurate and excessive. Therefore when we need more accurate result than 15 ppm we should correct integral nonlinearity of this ADC. In the same case the standardized noise level of this ADC does not exceed 2,5 least significant bits. Therefore we have approximately 5,5 stable bits, which we can not use because of their inaccuracy. Besides there are some advanced measurement methods like ratio measurement methods or replacement measurement method, which accuracy is defined by nonlinear error of ADC [4]. There was proposed method of ADC's integral nonlinearity identification in the set of testing points [5], which was conventionally called basic method. This method provides generation the set of testing points, which corresponds to the number sequence $1/N$ with integer N . It brings that all generated testing points are grouped in the lower half of ADC's range. The main goal of this paper is in the development and investigation method of ADC's integral nonlinearity identification and correction with uniform distribution of testing points.

II. Approach of Testing Points Generation

The basic and proposed method of testing points generation is based on analog to digital conversion of output signals of voltage divider, which consists of N serially connected resistors R_1, R_2, \dots, R_N , connected to reference power source U_{REF} . The measurement circuit is presented on fig. 1.

According to Kirchhoff's voltage law we can write

$$U_{REF} = \sum_{i=1}^N U_{R_i} \quad , \quad (1)$$

where U_{R_i} , $i = \overline{1, N}$ – voltages of appropriate resistors of the divider.

The average voltage of all resistors of the divider \bar{U} could be computed

$$\bar{U} = \frac{1}{N} \sum_{i=1}^N U_{R_i} . \quad (2)$$

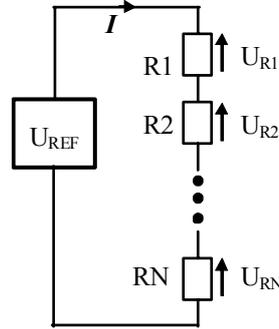


Fig. 1. Circuit of N -resistors voltage divider

Considering (1) we can present (2) as

$$\bar{U} = \frac{U_{REF}}{N} . \quad (3)$$

It means that average voltage of all resistors of the divider \bar{U} does not depend of voltages of separate resistors. Also it means that according Ohm's law the resistances of separate resistors does not influence on this average voltage. Taking into consideration that N is natural number the relative error $\delta_{\bar{U}}$ of \bar{U} is

$$\delta_{\bar{U}} = \delta_{REF} , \quad (4)$$

where δ_{REF} - relative error of power source of the divider.

In the case of ADC calibration by power source of the divider we can use average voltage \bar{U} as testing point for precision testing ADC's integral nonlinearity.

If we consider the result of analog to digital conversion of input voltage U is code C like

$$C = C_0 + \frac{C_{REF} - C_0}{U_{REF}} U + f(U) , \quad (5)$$

where C_0 - result of analog to digital conversion by null setting channel; C_{REF} - result of analog to digital conversion by calibration channel (in the case when input signal is U_{REF}); $f(U)$ - nonlinear component of conversion function.

Putting (1) and (2) into (5) and simplifying result we can compute integral nonlinearity of ADC $f(\bar{U})$ for voltage \bar{U} using conversion results C_i of voltages U_{R_i}

$$f(\bar{U}) = \frac{1}{N} \left(C_{REF} - C_0 - f(U_{REF}) - \sum_{i=1}^N (C_i - C_0) \right) = \frac{1}{N} \left(C_{REF} - C_0 - \sum_{i=1}^N (C_i - C_0) \right) . \quad (6)$$

Taking into consideration that we use the set of conversion results obtained by the same ADC with limited operating speed it puts on the limitation to time stability of reference power source during measurement experiment. The analysis of influence of tested ADC on residual error [6] show the potential of this method implementation for ADC with smooth conversion characteristic.

So the multi-resistors voltage divider provides precision identification of ADC's integral nonlinearity in one testing point without using precision resistors. It was proposed the method called basic method, which provides increasing the number of generated testing points by choosing N . Let N has the set of natural divisors $\{m_1, \dots, m_t\}$ then it is the set of natural numbers $\{k_1, \dots, k_t\}$, which satisfy a claim $N = m_i \times k_i$; $i = \overline{1, t}$. It allows converting the voltages on the cascades of k_i , $i = \overline{1, t}$ serially connected resistors, and these voltages corresponds (1). Therefore we can compute the integral nonlinearity of ADC according for the set of voltages

$$\bar{U}_i = \frac{U_{REF}}{N} k_i = \frac{U_{REF}}{m_i} ; \quad i = \overline{1, t} . \quad (7)$$

III. Approach of Testing Points Generation

The analysis of testing results of basic method of ADC's integral nonlinearity identification and correction [5, 6] emerge the linear dependence of the residual conversion error of the density of testing points concentration. It allow to separate at least two subranges – lower and higher half of ADC's range, which has different residual error after nonlinearity correction using this basic method. The residual nonlinear error of upper subrange is approximately ten times more than residual nonlinear error of lower subrange. Taking into consideration this results it is proposed to generate testing points for nonlinearity identification for multi-range ADC (in the simplest case for double range ADC) as the voltages of serially connected resistors of multi-resistors voltage divider, which are measured using lower subrange of highest range of ADC and use these voltages for calibration and nonlinearity identification/correction for all other ranges. So if we have voltage divider, which consists of N resistors: R_1, R_2, \dots, R_N we can generate testing points: first – the voltage on resistor R_1 , second – the voltage on serially connected resistors R_1 and R_2 , third – $R_1 \dots R_3$, etc. up to $N/2$ -th – $R_1 \dots R_{N/2}$. Generally this approach provides generation $N/2$ testing points with relative high precision, and which are uniformly distributed in the lower half of the highest range of ADC. Their using for calibration and nonlinearity identification for lower ranges provides high accuracy and uniform distribution (in the case when the ratio of high range to lower range not less then two) both of all generated testing points. Besides it is possible to generate arbitrary number of testing points by selecting appropriate N and increasing of generated testing points demands smaller increasing of N in comparison with basic method.

IV. Investigation Residual Nonlinear Error

Investigation of the residual nonlinear error by experimental way demands extremely precision equipment with error 3...5 times less then expected residual nonlinearity and it corresponds to 0,5 ppm. Besides it is necessary to have the opportunity to set the level and view of ADC's nonlinearity with the same error level. So it is proposed to make investigation of the proposed method by simulation and evaluate the influence of resistors' error and ADC's noise on residual nonlinear error for different nonlinearity functions. Generally the methodology of investigation is equivalent to the same methodology described in [6] and consists of the following stages:

- definition by random way the two curves, which simulates the ADC's nonlinearities on higher and lower ranges and resistance of divider's resistors R_1, R_2, \dots, R_N ;
- computing the results of analog to digital conversion for appropriate combinations of resistors for implementation the basic method for ADC's higher range nonlinearity identification;
- noising these conversion results for simulation random error of ADC;
- computing parameters of correction function for ADC's higher range nonlinearity;
- computing voltages on serially connected resistors $R_1; R_1, R_2; R_1 \dots R_3; \dots; R_1 \dots R_{N/2}$ using simulated results of analog to digital conversion for these voltages on higher range and nonlinearity correction function;
- computing the results of analog to digital conversion for these voltages using lower range of ADC;
- noising these conversion results for simulation random error of ADC;
- computing parameters of correction function for ADC's lower range nonlinearity;
- computing residual error of integral nonlinearity correction for ADC's lower range as the difference between defined curve and computed correction function for this range.

So accumulation the set of residual error curves we can implement the statistical data manipulation methods for investigation parameters of the proposed method and their sensitivity to ADC's random error and resistors' error. The nonlinearity simulations curves for higher and lower ranges are based on fourth order polynomial functions with random coefficients [5]. The validity criterion of each curve is not exceeding, by the absolute maximum value on the range of ADC the, constant 250 quanta. This constant corresponds to the maximum allowable nonlinearity of AD7714. Examples of such curves, which simulate ADC's nonlinearity, are presented on fig. 2. Y axes – nonlinearity in quantum, X axes – input voltage in percents of the range. Also there are presented two curves with maximum and minimum values for 500 curves, which where generated for investigation.

The developed software verification was done by setting "ideal" resistors and ADC (zero error of all resistors and zero ADC's random error). In this case we obtain maximum error 0,05 quantum, which we can explain by rounding error during computing. Therefore we can accept that developed models and software are adequate and we can use them for investigation the influence of components' error on the residual error after ADC's integral nonlinearity correction.

The simulation was done for 12 resistors voltage divider. This number of resistors was selected on the basis of two antinomic requirements:

- maximum number of natural dividers for implementation large amount of generated testing points (number 12 totally has six dividers: 1, 2, 3, 4, 6, 12);
- minimum number of resistors for decreasing the channels of multiplexer and simplification it (12-resistors divider demands 2 switches with 13 channels each for implementation multiplexer).

The simulated resistors' error is ± 1 and ± 2 %. It corresponds to 10 ... 20 years of exploitations of wide used wire-wound-type resistor with allowable error $\pm 0,1$ %. The wave of residual error vs input voltage for lower range in the case of resistors' error ± 1 % is presented on fig. 3. It is presented five randomly selected curves and two curves with maximum and minimum values for 500 curves. As we can see maximum value does not exceed 1,5 quantum for the worst case. This value is commensurable with ADC's resolution. Maximum residual error for resistors error ± 2 % does not exceed 3,5 quanta. This value is commensurable with ADC's noise.

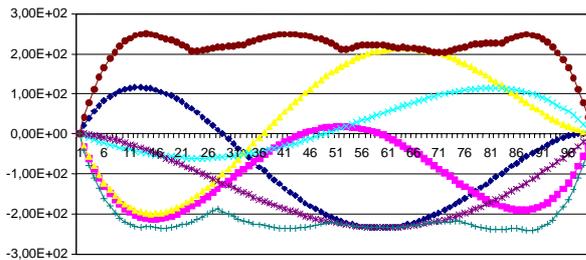


Fig. 2. Simulated nonlinearity of ADC



Fig.3. Residual error vs input voltage for resistors' error ± 1 %

The results of investigation results of influence the random error of ADC (noise) on residual error for noise level ± 6 quanta is presented on fig 4. There are five randomly selected curves and two curves with maximum and minimum values for 500 curves. As we can see the maximum value does not exceed 18 quanta for the worst case. Generally these results are close to the results of basic method investigation [5] but they corresponds to the whole lower range of ADC instead lower subrange of basic method. The view of the curves obtained for other level of ADC's noise is approximate to curves presented on fig. 4.

The dependence of maximum value of residual error for lower range of ADC vs noise level is presented on fig.5. The division of maximum value of residual error to appropriate noise level for all ptdained points does not exceed three times. Taking into consideration the linear character of function presented on fig. 5. we can extrapolate it on other noise level. It is possible to conclude that division of maximum value of residual error to appropriate noise level we can consider as noise influence coefficient and it does not exceed three for implementation the presented method using 12 resistors voltage divider.

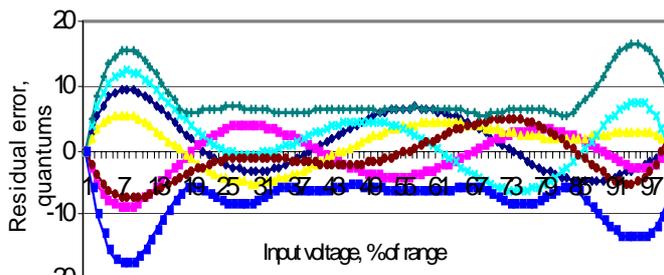


Fig.4. Residual error vs input voltage for ADC's noise ± 6 quanta

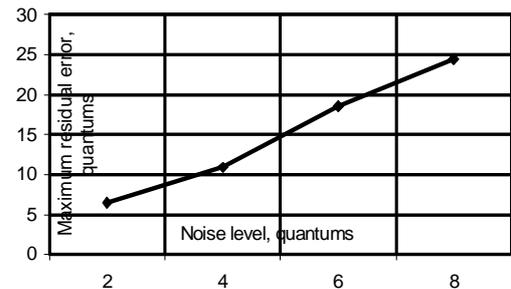


Fig.5. Maximum residual error vs ADC's noise level

V. Conclusions

Investigation of the proposed method of integral nonlinearity identification and correction for lower range of ADC gives us the following conclusions:

- The proposed method of multi-range ADC's integral nonlinearity testing and correction provides generation the set of testing points which corresponds to number sequence $\frac{1}{N}$ for highest range and provides uniform distributions for all lower ranges of ADC. It meets with the requirements of actual standards to metrology verification of ADC with smooth conversion characteristic [7, 8, 9] and provides development metrology verification systems for such ADC.
- The total number of testing points is defined by the number of resistors of multi-resistors divider and could

be predefined by selecting appropriate number of resistors of multi-resistors. It provides development metrology verification system of ADC with arbitrary ranges.

- The influence of resistors' error of multi-resistors divider on accuracy of generated testing points is negligibly small. It provides development of metrology verification system of ADC using imprecise resistors.
- The accuracy of generated testing points is defined by accuracy of reference voltage source and noise level of tested ADC. It provides development metrology verification system of ADC, which generate the set of precise testing points using precise only single channel reference voltage source.

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