A CMOS 1.5-Bit ΣΔ Digital IF to RF Transmitter for WCDMA Application

Yongping Han[1], Shahin Mehdizad Taleie[2], Tino Copani[3],
Bertan Bakkaloglu[4], and Sayfe Kiaei[4]

[1] Texas Instruments., Tucson, AZ, y-han@ti.com
[2] Qualcomm, Inc., San diego, CA, shahinm@qualcomm.com
[3] ST Microelectronics, Catania, Italy, tino.copani@asu.edu
[4] Arizona State University, Connection One NSF Center, <sayfe, bertan>@asu.edu

Abstract **-** A digital intermediate frequency (IF) to RF transmitter targeted for 2GHz wideband code division multiple access (WCDMA) is presented. The proposed transmitter integrates a 3-level digital IF current-steering cell, an up-conversion mixer with a tuned load and an RF variable gain amplifier (RF VGA) with an embedded semi-digital finite impulse response (FIR) reconstruction filter. A 4th-order 1.5-b IF bandpass sigma delta modulator (BP ΣΔM) is designed to guarantee in-band signal-to-noise ratio (SNR) and error vector magnitude (EVM) performances while the out-of-band quantization noise due to noise shaping is suppressed by the embedded FIR reconstruction filter to meet spectrum emission mask and ACPR requirements. The on-chip RF VGA provides 50dB power scaling in 10-dB steps with less than 1dB gain error. Together with the power control at the ΣΔM stage, the 74-dB dynamic range at RF frequency is achieved. The design is fabricated in a 4-metal 0.18-μm CMOS technology with a total core area of 0.8 × 1.6 mm^2. The IC delivers 0dBm output power to the 50Ω load at 2GHz and it draws approximately 120mA from a 1.8V DC supply at the maximum output power.

Index Terms— digital transmitter, sigma-delta modulator (ΣΔM), digital to analog converters (DACs), digital IF, RF variable gain amplifier (RF VGA), wideband code division multiple access (WCDMA)

I. Introduction

With the increasing demand for high linearity, power efficient and wide-bandwidth mobile devices, RF systems will benefit from moving the interface between the digital and analog domains closer to the antenna. Furthermore, in order to take advantages of the deep submicron CMOS technologies and digital signal processing (DSP), there is a strong trend towards the development of digital heterodyne architectures where the digital baseband signal is digitally up-converted to intermediate frequency (IF) [1], and RF up-conversion is part of the digital-to-analog conversion (DAC) [2], [3].

The digital to RF up-conversion methods includes current- steering DAC cells [2-4], multi-bit ΣΔ noise shaped IF [2], and the inherently linear single-bit RFDACs [3]. The digital heterodyne transmitter has the advantages of higher integration level and power efficiency, improved I/Q matching and EVM performance, and adaptive modulation of the transmitted signal bandwidth without the need of external IF SAW filter [1]. In addition, the problems associated with conventional homodyne transmitters including DC offset and LO leakage, are greatly reduced due to the elimination of the analog gain stage in the baseband. The RF DAC presented in [2] shows better signal-to-noise ratio (SNR), lower power consumption and reduced hardware complexity compared to the conventional Mixer-Following-DAC architecture. In this architecture, higher SNR is achieved by using multi-bit (8-level) ΣΔM with high sampling frequency of 514 MHz. However, the multi-bit DAC requires additional mismatch reduction techniques, such as dynamic element matching (DEM), which increases the system complexity and power consumption. The architecture of RFDAC presented in [3] offers advantages in terms of high integration due to digital-intensive design and higher linearity. The impact of flicker noise up-conversion due to the DAC's current sources is reduced by alternating the operation point of the rail device from accumulation to inversion. Also jitter masking technique is employed to minimize IF jitter impact, which ensures that the current source is off during the DAC bit switching transition. However, the design shows some limitations, which make it hard to be used in the wideband transmitter applications. One limitation is inadequate filtering of the out-of-band quantization noise. Another limitation is the use of single-ended local oscillator (LO) that drives the gate of the rail device, which leads to higher LO leakage compared to that of the conventional Gilbert-cell mixer.

In this paper, a digital IF to RF transmitter (DRFTx) is proposed for WCDMA applications utilizing a 3-level digital IF DAC and a Gilbert-cell-based up-converter, followed by a RF variable gain amplifier with an embedded linear-phase band-pass reconstruction filter. The paper is organized as follows. Section II describes the proposed architecture. Section III provides the circuit level implementation of the proposed transmitter. The measurement results for the this work are presented in Section IV. Finally, the conclusions are drawn in Section V.

II. PROPOSED DIGITAL IF-TO-RF TRANSMITTER

Fig.1 demonstrates the proposed transmitter architecture consisting of 1.5-bit band-pass ΣΔ Modulator, a wideband digital IF to RF up-conversion DAC followed by a RF VGA. The FIR reconstruction filter is embedded into the up-conversion block. The architecture performs RF up-conversion, mixing the LO signal with 3-level digital IF bit stream, while the quantization noise is suppressed by the reconstruction filter. In the proposed architecture, the digital IF signal is noise-shaped via a 4th-order 1.5-bit BP ΣΔM to improve in-band SNR, while the out-of-band quantization noise due to noise-shaping is filtered out by the semi-digital FIR filter and the analog image and spur rejection filter. In this work, the out-of-band quantization noise suppression is designed to meet WCDMA spectrum emission mask and ACPR requirements [4]. 74dB dynamic range demanded by the WCDMA standard [4] is distributed to ΣΔM stage and RF VGA to overcome CMOS substrate isolation limitation.

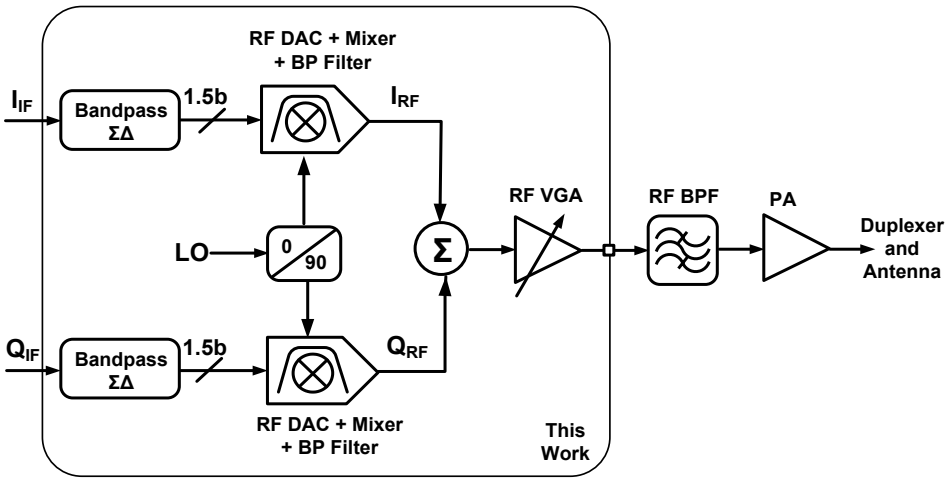


Figure 1: Proposed CMOS digital-IF transmitter architecture

At the baseband I/Q signals are first interpolated and up-sampled from 3.84MHz (WCDMA chip rate is 3.84Mcps) to f_s=253.44MHz, and then digitally up-converted to the intermediate frequency (IF) at $f_{IF}=f_s/4$= 63.36MHz. By choosing a sampling frequency f_s within the range from 250MHz to 260MHz, digital images will be out of the WCDMA transmitter and receiver bands [1], thereby relaxing the requirements on the reconstruction filter after the DAC.

The digital band-pass IF signal is 1.5-bit noise-shaped via the 4th-order band-pass (BP) ΣΔ Modulator. In order to maximize in-band SNR, the resonate-based ΣΔM is utilized. Furthermore, a 3-level quantizer is adopted in BP ΣΔ Modulator to boost the in-band SNR compared to the 2-level quantization. 3-level IF signaling reduces the transient glitch and the quantization noise level and still maintains good linearity compared to the 2-level DAC. For the given sampling frequency of f_s=253.44MHz and the signal bandwidth of about 5MHz (taking the WCDMA baseband root-raised cosine filter roll-off factor into account), the oversampling ratio is about 25[5]. From the system level simulations, 1.5-bit 4th-order BP ΣΔM is enough to provide in-band SNR with the sampling frequency of 253.44 MHz and 40-tap BP FIR filter is sufficient to reduce out-of-band quantization noise and meet the WCDMA spectrum emission mask and ACPR requirements. Fig. 2 shows the WCDMA spectrum after 40-tap FIR filtering at the IF.

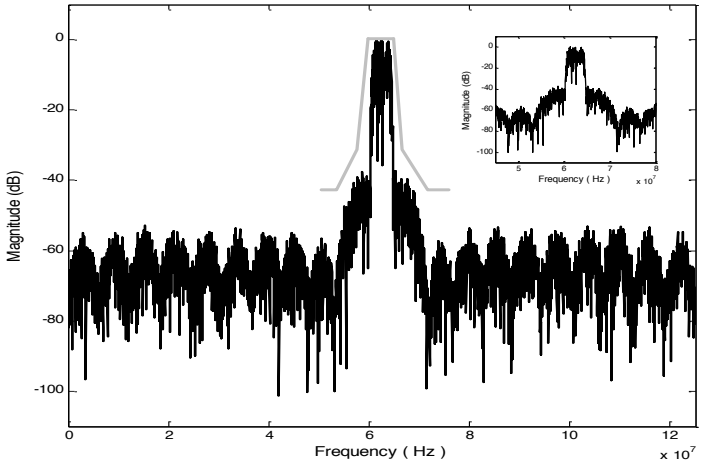


Figure 2: Simulated WCDMA IF spectrum after 40-tap FIR filtering

III Circuit Implementation of the Proposed Transmitter

A. Digital IF to RF Converter with BP Reconstruction Filter

Fig. 3 shows the schematic of digital IF to RF converter with embedded BP FIR filter. It includes a current-steering DAC, 1.5-bit digital IF switching cells, FIR filter and Gilbert-cell up-converter. Since 40-tap BP FIR filter is adopted for this design, there are 20 delay cells each of which realizes inverse of two unit delays based on $-z^{-2}$ in the digital domain, hence 20 IF switching cells each of which is driven by the delayed 3-level digital noise-shaped IF signal. The 20 non-zero FIR coefficients a_1 to a_{20} are embedded in the current sources of the IF switching stages. The output currents from all IF switching stages are summed and sent to the LO quad and then up-converted to the desired frequency of 2GHz. By absorbing FIR coefficients into the current sources of IF switching stages, the

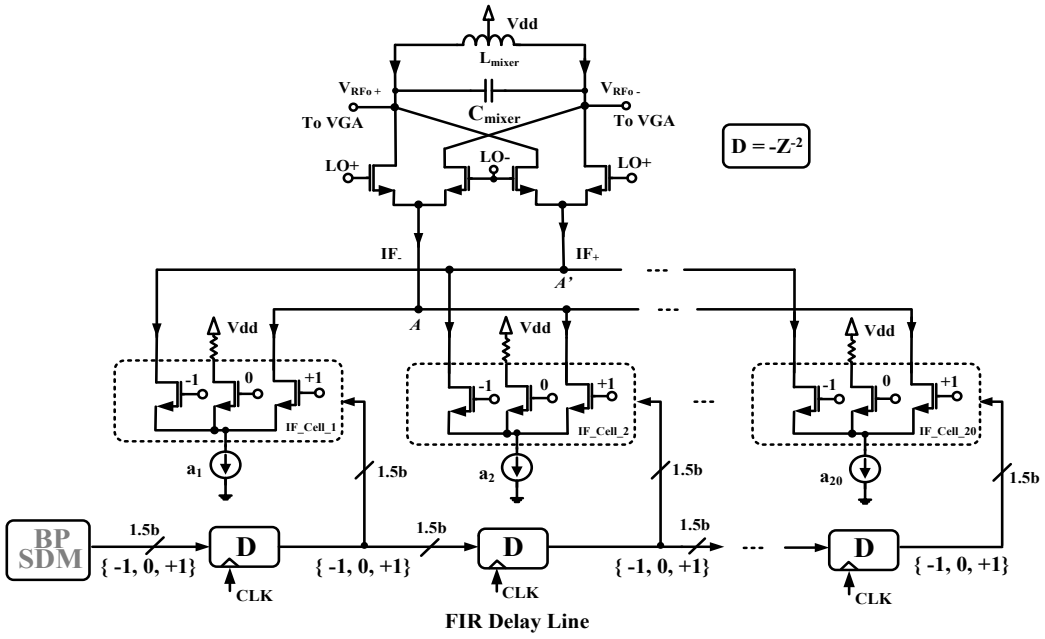


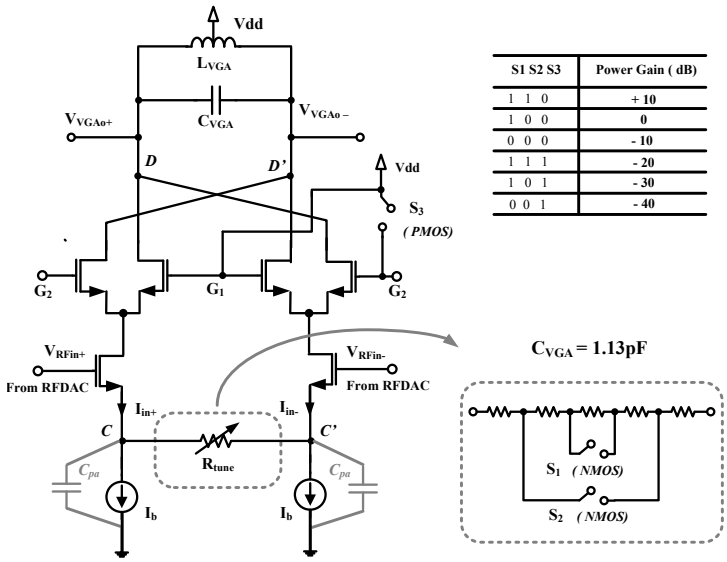
Figure 3: Simplified schematic of digital IF to RF converter with BP reconstruction filter

RFDAC, up-conversion mixer and BP FIR filter are merged into a compact block. The three-level IF signaling is achieved in the DAC path by adding a current dump path to the two-level DAC. Therefore there is a positive path corresponding to +1, a negative path corresponding to -1, and a dump path related to 0.

For the circuit level implementation of the FIR filter coefficients, DC current sources are used. The DC current sources are implemented using NMOS transistors, and sizes of the transistors are scaled by the filter coefficients. The length of the current source devices is optimized to achieve desired output impedances. The device sizes are symmetrical around the center to maximize phase linearity, so there are only 10 different filter coefficients. The gate voltage of the NMOS devices is biased through a constant-gm current bias circuit.

B. RF VGA with programmable power step

The required transmitter power control range is 74dB for WCDMA [4]. The control range can be achieved in two separate stages with 50dB from RF VGA and the rest from the sigma-delta IF stage to overcome the substrate isolation limitation. Therefore, the digital up-converter is connected to a VGA for gain-control and further out-of-band filtering purposes. A discrete-power-control RF VGA is utilized in this work as shown in Fig. 4. The VGA consists of a degenerated input transistor pair, a variable degeneration resistor bank R_{tune}, switchable cross-coupled current canceling paths, and a tunable LC load with a MIM capacitor bank C_{VGA}.



S1 S2 S3	Power Gain (dB)
1 1 0	+ 10
1 0 0	0
0 0 0	- 10
1 1 1	- 20
1 0 1	- 30
0 0 1	- 40

Figure 4: Discrete-power-step RF VGA with LC load

Due to the parasitic capacitance C_{pa} at nodes *C* and *C'*, the resistive degeneration can only provide 20dB power variation. In order to overcome this limitation, a differential cross-coupled transistor pair switched in parallel to the cascode devices, expanding the gain control variation to the target range of 50dB. By properly sizing the degeneration resistors and the cross-coupled transistors, a gain control with 10-dB steps is achieved as shown in the table in Fig. 4. Fine gain control of 1-dB step is obtained in the ΣΔ digital IF generator to minimize phase and gain discontinuity in the modulated signal.

IV. Experimental Results

The proposed digital IF to RF transmitter is fabricated on a 0.18-μm CMOS process. The die micrograph is shown in Fig. 5. The design occupies a 1.28-mm^2 die area. Multiple ground bonding wires are used to reduce parasitic inductance impact on circuit stability and performance. Fig. 6 illustrates the ideal FIR frequency response along with filtered BP sigma-delta spectrum and compared to the measured carrier at 2.06GHz. A minimum 40dB out-of-band quantization noise suppression can be achieved after FIR filtering. Fig. 7 shows the two-tone test performance. A two-tone digital IF signal is applied with 1MHz offset. The measured IMD3 is -52dBc. Fig. 8 shows the measured

WCDMA output spectrum centered at 2.0626 GHz. The chip achieves -35dBc ACPR at 5MHz offset and -50dBc at 10MHz offset, which meets the WCDMA ACPR requirements. The measured rms EVM is less than 4.8%. The total chip power consumption is measured about 120mA from 1.8V supply with 0dBm output power.

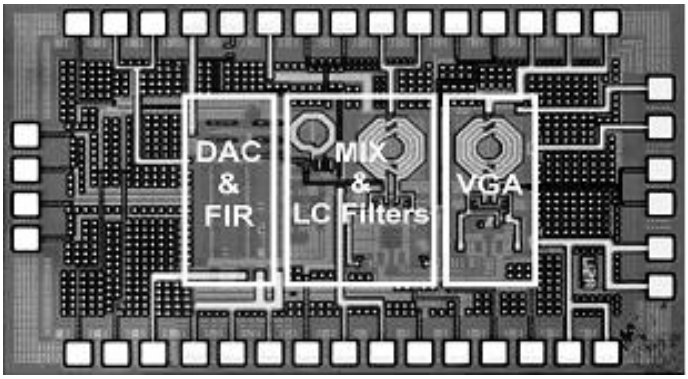


Figure 5: Die micrograph

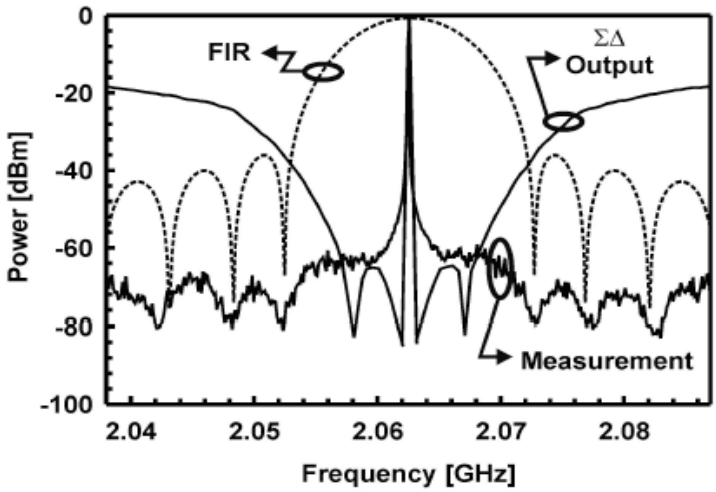


Figure 6: Ideal BP FIR filter response, BP ΣΔ modulated signal and measured single-tone spectrum

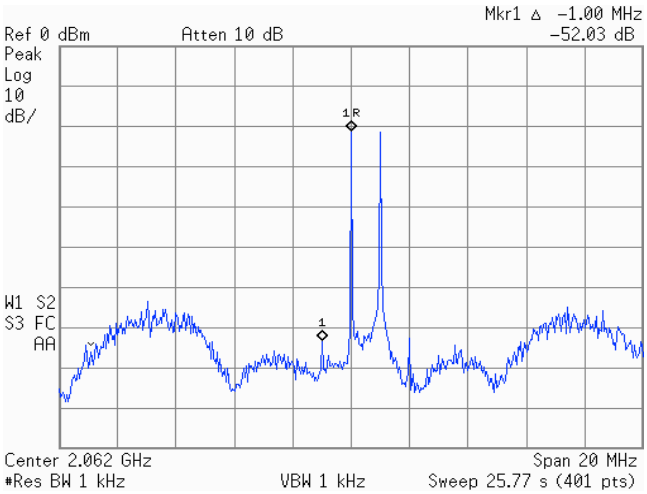


Figure 7: Measured IMD3 performance based on the two-tone test

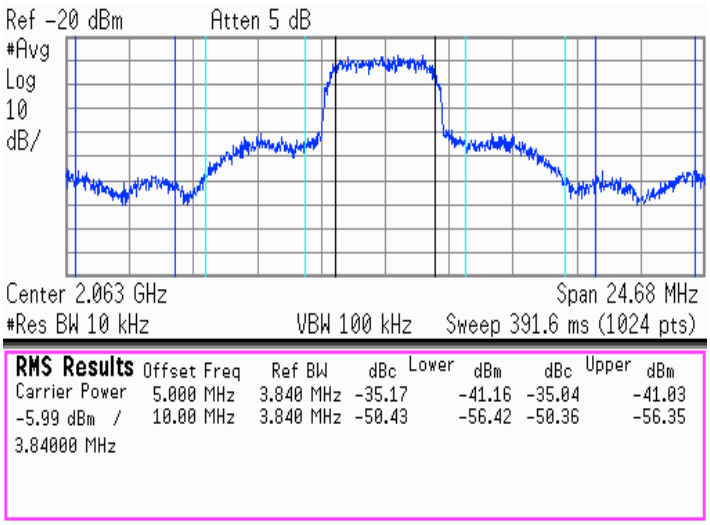


Figure 8: Measured WCDMA ACPR performances

V. Conclusions

A highly integrated digital IF to RF transmitter (DRFTx) which combines a 1.5-bit current steering DAC, a semi-digital FIR filter and a RF mixer along with a RF VGA implemented in 0.18μm CMOS technology is presented for WCDMA mobile application. The embedded reconstruction filter attenuates the out-of-band quantization noise below the spectral emission mask of WCDMA. 74dB dynamic range is achieved by scaling the power of both sigma-delta digital IF stage and RF VGA stage. The proposed DRFTx achieves good linearity utilizing 1.5b DAC. The measured results show that a digital-intensive digital IF to RF converter architecture can be successfully employed for WCDMA transmitter application.

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