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Analysis of Conversion Time of Time-to-Digital Converters with Charge Redistribution

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Abstract- The paper provides the analysis of the conversion time of a class of time-to-digital converters based on binary search principle realized by time-to-charge translation and self-timed successive charge redistribution in the binary-scaled capacitor array.

I. Introduction

In various sensing systems, time is an intermediate or an output representation of the measured quantity. Time encoding and time-to-digital converters (TDCs) are often used as components of analog-to-digital conversion (ADC) process (e.g., [1]-[3]). The well-known examples of the time-based synchronous ADCs are multislope converters commonly applied for decades (e.g., a dual-slope ADC). In particular, in the asynchronous ADCs developed in the last decade, the digital output words represent information on a sequence of time intervals that encode analog signal values [4-7]. The known approaches to asynchronous analog-to-digital conversion use the clock-based TDCs where the time discretization is based on counting periods of a high frequency reference clock during the discretized time intervals [4-7]. The time-to-digital conversion using the reference clock is simple and characterized by a non-redundant conversion time [8]. However, the clock-based TDCs with n bits of precision needs a maximum number of 2^n state transitions (clock cycles) per single conversion which is a reason of considerable amount of power consumption.

In Ref. [9] and [10], a new method of clockless time-to-digital conversion has been proposed. The concept of this method is based on applying the *binary search principle* to the conversion in the time domain. In the first phase of the proposed conversion, the discretized time interval T_{In} is translated to the corresponding charge portion Q_{In}. In the second phase, the charge portion Q_{In} is processed in the charge domain by self-timed successive charge redistribution in the binary-scaled capacitor array. Two versions of the time-to-digital converters based on the binary search algorithm have been proposed: the *Successive Charge Redistribution TDC* (SCR-TDC) where the time-to-charge translation and the charge-to-digital conversion are realized *sequentially* [9], and the *Direct Successive Charge Redistribution TDC* (DSCR-TDC) where time-to-charge translation is carried out *concurrently* to charge-to-digital conversion [10]. The important advantage of the proposed conversion method is that, the number of state transitions per a single conversion cycle equals only (n+1) in the DSCR-TDC and respectively (n+2) in the SCR-TDC.

In general, the time-to-digital converters with self-timed charge redistribution, unlike the classical time-to-digital converters with the reference clock, are characterized by a redundant conversion time that on the other hand depends non-linearly on the input time interval width T_{In}. Both the SCR-TDC and the DSCR-TDC may be implemented in the configuration with a single current source or with two current sources. In the latter, the charge redistribution is realized by the use the current source of higher effectiveness. Then, the conversion time is shorter and independent of the duration of discretized time interval T_{In}. In the configuration with a single current source used both during the charge accumulation and redistribution, the conversion time is longer and is determined by the T_{In}. A detailed comparison of the SCR-TDC and the DSCR-TDC is presented in [10].

The present study provides a careful analysis of the conversion time of both the SCR-TDC and DSRC-TDC. In particular, the maximum and minimum values of the conversion time, and the maximum time space required between beginnings of subsequent conversion cycles are evaluated. As follows from the presented analysis, the conversion time is shorter in the DSCR-TDC by the duration of the time-to-charge mapping which is equal to the quantized time interval T_{In}. Consequently, as will be shown, the conversion time of the DSCR-TDC is reduced at least twice for short time intervals, and at least four times for long time intervals. Moreover, the conversion time of the DCSR-TDC, especially for selected values of the T_{In}, is very short and may even equal zero for long time intervals. As a result, the *conversion time jitter* (i.e., the difference between the maximum and minimum conversion time) is reduced twice in the DSCR-TDC in relation to the SCR-TDC. The price for the advantages

of the DSCR-TDC stated above is a higher complexity of the algorithm of the asynchronous state machine that manages the converter operation compared to the relevant algorithm of the SCR-TDC.

I. Principles of time-to-digital conversion with self-timed charge redistribution

The block diagram of the SCR/DSCR-TDC is presented in Fig. 1. Both converters types are built of the binary-weighted capacitor array, two asynchronous comparators, one or two current sources, two voltage sources, and the asynchronous state machine that manages the conversion algorithm. In the SCR-TDC, the capacitor array contains a number of n+1 capacitors, and in the DCSR-TDC, a number of n capacitors, respectively, because the input capacitor of the highest capacitance is removed in the latter. Each conversion cycle is preceded by the relaxation phase triggered by the asynchronous state machine in order to discharge all the capacitors in the array.

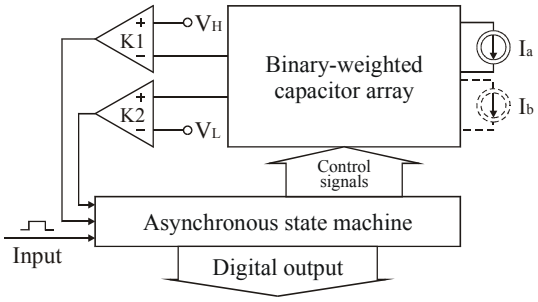

Figure 1. Block diagram of successive charge redistribution time-to-digital converter (SCR/DSCR-TDC)

A. Successive charge redistribution time-to-digital converter (SCR-TDC) operation

The circuit diagram of the SCR-TDC is shown in Fig. 2. The SCR-TDC operates as follows [9]. Assume that the time interval, whose duration T_{In} is converted to a digital number, is provided in a from of a pulse signal to the SCR-TDC input. Detecting a leading edge of the pulse on the SCR-TDC input causes the input capacitor C_n to be charged by the current source of constant intensity I_a (Fig. 2). The trailing edge of the pulse, whose duration T_{In} is discretized, stops charging the input capacitor. Thus, the charge portion Q_{In} collected in the input capacitor as an intermediate variable is proportional to the time interval T_{In} corresponding to the pulse width:

$$Q_{In} = T_{In} I_a$$

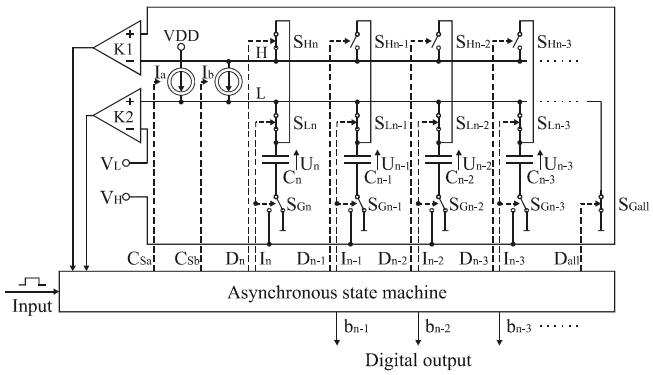

Figure 2. The SCR-TDC circuit diagram with two current sources. The controlled switch positions correspond to the relaxation phase

The trailing edge of the pulse on the SCR-TDC input starts the *conversion phase*. The conversion, carried out in the charge domain, consists of n steps where n is a number of bits in the digital output codeword. The charge portion Q_{In} collected in the input capacitor C_n and representing the discretized time interval T_{In} is divided among a set of capacitors C_{n-1},C_{n-2}, …,C_0 of binary weighted capacitances where $C_{i+1} = 2C_i$, $i = 0$, …,n-1. The division is carried out by charge transfer with the use of the current source I_a (in the version of the SCR-TDC with a single current source) or by an extra current source I_b (in the version of the SCR-TDC with two current sources) to accelerate the charge redistribution process. Thus, the effectiveness of the current source I_b should be higher than of the current source I_a (i.e., I_b=mI_a, m>1). Each capacitor C_i corresponds to the appropriate bit b_i in the output digital word. In particular, the capacitance C_{n-1} is assigned to the most-significant bit (MSB), and the capacitance C_0 corresponds to the least-significant bit (LSB). In the first conversion step, the input capacitor

plays a role of a source of charge that is successively transferred to the capacitor C_{n-1} operating as the first destination capacitor. If a voltage on the capacitor C_{n-1} reaches the prespecified threshold V_L, then the most significant bit b_{n-1} is set to one. Next, the remaining charge stored in the input capacitor C_n is transferred in the second conversion step to the capacitor C_{n-2} that takes over the role of the next destination capacitor.
However, if the capacitor C_n is discharged before the voltage on the capacitor C_{n-1} reaches the threshold V_L during the first conversion step, then the most significant bit b_{n-1} is set to zero. Furthermore, in the second conversion step, the capacitor C_{n-1} plays the role of the next source capacitor and the charge is then transferred from the C_{n-1} to the C_{n-2}. The cycle is repeated for the subsequent steps. Each conversion step produces one bit more precise discrete estimate of the input time interval. The states of bits of the output word are determined successively from the MSB to the LSB. In the kth step, the states of the bits $b_{n-k+1}, b_{n-k+2}, \ldots, b_{n-1}$ are already fixed.

B. Direct successive charge redistribution time-to-digital converter (DSCR-TDC) operation

The circuit diagram of the DSCR-TDC with two current sources is shown in Fig. 3.

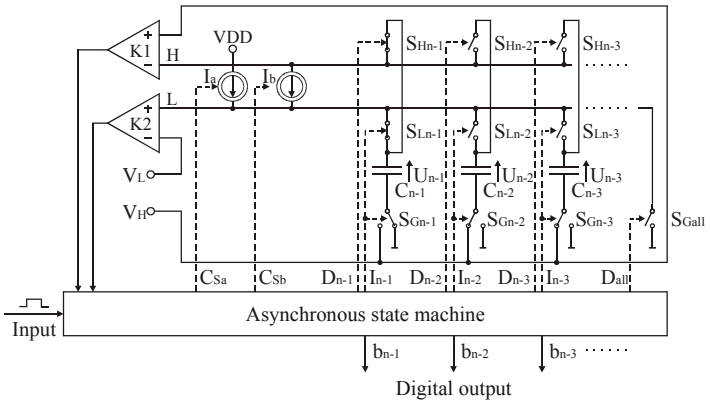

Figure 3. Circuit diagram of the DSCR-TDC with two current sources. The controlled switch states correspond to the first step of the accumulation/conversion phase when the capacitor C_{n-1} is charged

The DSCR-TDC operates as follows [10]. Detecting a leading edge of the pulse by the asynchronous state machine causes the capacitor C_{n-1} corresponding to the most significant bit (MSB) to be charged by the current source of constant intensity I_a. If a voltage on the capacitor C_{n-1} reaches the prespecified threshold V_L before the trailing edge of the pulse T_{In} is detected by the asynchronous state machine, the most significant bit b_{n-1} is set to one. Then, the consecutive capacitors $C_{n-2}, C_{n-3}, \ldots$ are charged sequentially in order to decreasing capacitances by the current source I_a. Assume that the discretized time interval T_{In} ends in the kth step of charge accumulation where $k \in \{1,\ldots,n\}$, i.e., during the time when the capacitor C_{n-k} is charged. The trailing edge of the pulse T_{In} stops to provide charge from the current source I_a, and starts to redistribute the *residual charge* stored in the latterly charged capacitor C_{n-k} into the set of binary-weighted capacitors $C_{n-k-1}, \ldots, C_0$ (Fig. 3).
The residual charge redistribution is carried out by the current source I_a (in the version of DSCR-TDC with a single current source) or by an extra current source $I_b = mI_a$, $m>1$ in the version of DSCR-TDC with two current sources). In the first step of *residual charge successive redistribution*, which is at the same time the $(k+1)$th conversion step, the capacitor C_{n-k} starts to act as the first source capacitor whereas the role of the destination capacitor plays the capacitor C_{n-k-1}. Further conversion proceeds in the same way as in the SCR-TDC as follows.

II. Analysis of the conversion time in SCR-TDC and DSCR-TDC

As stated, the time-to-digital conversion carried out by the SCR/DCSR-TDC consists of the subsequent conversion steps. Now, the duration of particular steps will be analysed in details.

A. Duration of Conversion Steps
The duration of the kth conversion step depends on the state of the output bit b_{n-k} evaluated at the end of this step. *Duration of Conversion Step with Evaluating Bit State to '1'*. The bit b_{n-k} is set to one if the charge portion stored in the source capacitor at the beginning of the kth conversion step is greater than the charge needed for charging the destination capacitor to the desired voltage V_L. The duration of the kth conversion step with evaluating the state of the bit b_{n-k} to one reaches its maximum $T_{k\max}$. The $T_{k\max}$ equals the duration of charging the capacitor C_{n-k}, that acts as the destination capacitor in the kth step, to the voltage V_L by the use of the current source $I_b = mI_a$:

$$T_k = T_{k\max} = T/2^k m \qquad \text{if } b_{n-k}=1 \tag{1}$$

where $T = 2^n V_L C_0 / I_a$ is the input range of the SCR-TDC equal to the duration of charging the input capacitor $C_n = 2^n C_0$ to the voltage V_L by the use of the current source I_a. As follows from (1), the maximum duration of the successive step $T_{k\max}$ halves with a number of the conversion step k since the capacitances of subsequent destination capacitors are reduced twice, and the rate of charge redistribution defined by I_b is constant.

Duration of Conversion Step with Evaluating Bit State to '0'. Similarly, the bit b_{n-k} is set to zero if the charge portion stored in the source capacitor at the beginning of the conversion step is smaller than the charge needed for charging the destination capacitor to the desired voltage V_L. The duration of the kth conversion step with evaluating the state of the bit b_{n-k} to zero is thus shorter than its maximum value:

$$T_k < T/2^k m \quad \text{if } b_{n-k}=0 \tag{2}$$

The exact duration of the T_k in case if $b_{n-k}=0$ can be found on the basis of the observation that the charge portion $Q_k = mI_a T_k$ transferred to the capacitor C_{n-k} during the kth conversion step equals the difference of the charge Q_{In} representing the converted time interval T_{In} and the charge portions $Q_1,\ldots,Q_{k-1}$ disposed in the destination capacitors $C_{n-1},\ldots,C_{n-k+1}$ in the previous 1,…,k-1 conversion steps as follows:

$$Q_k = Q_{In} - \sum_{i=0}^{k-1} b_{n-i} Q_i \tag{3}$$

where Q_{In} is the charge representing the converted time interval T_{In} and $\sum_{i=0}^{k-1} b_{n-i} Q_i$ is the sum of the charge portions stored in these capacitors $\{C_{n-1}, C_{n-2},\ldots,C_{n-k+1}\}$ on which the voltage value V_L has been obtained represented by evaluating the corresponding bits from the set $\{b_{n-1}, b_{n-2},\ldots, b_{n-k+1}\}$ to one. The exact duration of the kth conversion step with evaluating the state of the bit b_{n-k} to zero is defined by the following formula:

$$T_k = T_{In} - \sum_{i=0}^{k-1} b_{n-i} T_i \quad \text{if } b_{n-k}=0 \tag{4}$$

where $\sum_{i=0}^{k-1} b_{n-i} T_{i\max}$ is the sum of durations of previous conversion steps from 0 to k-1 that have been terminated with evaluating the output bits $b_{n-1},\ldots,b_{n-k+1}$ to one. The initializing conditions $T_0=0$ and $b_n=0$ have not any physical interpretation and are introduced to the formula (4) arbitrary in order to model the duration of the first conversion step (k=1) accordingly.

B. Duration of Conversion Step in General Case

Summing up, the duration T_k of the kth conversion step is defined both in the SCR-TDC and in DSCR-TDC as:

$$T_k = \begin{cases} \dfrac{T}{2^k m}; \text{if} : T_{In} \geq \dfrac{T}{2^k m} + \sum_{i=0}^{k-1} b_{n-i} T_i \\ T_{In} - \sum_{i=0}^{k-1} b_{n-i} T_i; \text{if} : T_{In} < \dfrac{T}{2^k m} + \sum_{i=0}^{k-1} b_{n-i} T_i \end{cases} \tag{5}$$

where

$$b_{n-i} = \begin{cases} 1, \text{if} : T_i = T/2^i m \\ 0, \text{if} : i = 0 \vee (i > 0 \wedge T_i < T/2^i m) \end{cases} \tag{6}$$

and $T_0 = 0$, $b_n = 0$ by the convention as stated before.

In particular, for $m = 1$ (i.e., for a converter version with a single current source), the duration of the first conversion step T_1 is: $T/2$ if b_n=1, which occurs for $T_{In} \geq T/2$; or T_{In} if b_n=0, which occurs for $T_{In} < T/2$. The 2nd conversion step for $m = 1$ lasts: $T/4$ if b_{n-1}=1, which occurs for $T_{In} \geq T/4 + b_n T/2$; or $T_{In} - T/2$ if b_{n-1}=0, which occurs for $T_{In} < T/4 + b_n T/2$. Durations of subsequent conversion cycles can be estimated accordingly.

C. Conversion Time in SCR-TDC

By taking into account the formula (5), the conversion time T_{C_SCR} versus the input time interval width T_{In} of the SCR-TDC is defined as follows:

$$T_{C\_SCR}(T_{In}) = \sum_{k=1}^{n} \left[b_{n-k} \frac{T}{2^k m} + (1 - b_{n-k}) \cdot \left(T_{In} - \sum_{i=1}^{k} b_{n-i} \frac{T}{2^i m} \right) \right] \tag{7}$$

The plot of the normalized conversion time T_{C_SCR} vs. the normalized input time interval width T_{In} for the 12-bit SCR-TDC according to (7) is shown in Fig. 4. As follows from (7) and Fig. 4, the conversion time $T_{C\_SCR}(T_{In})$ depends non-linearly on the input time interval width T_{In}.The maximum conversion time of the SCR-TDC occurs when all the bits in the output digital word are evaluated to one because the durations of all the conversion steps reach its maximum value defined by (1). This corresponds to a situation when the T_{In} approaches the SCR-TDC conversion range T divided by m:

$$T_{C\_SCR\max} = \sum_{k=1}^{n} T_{k\max} = \sum_{k=1}^{n} \frac{T}{2^k m} = T\frac{2^n - 1}{2^n m} \cong \frac{T}{m} \tag{8}$$

As follows from (8), the maximum conversion time is almost independent of the SCR-TDC resolution (n) and with an increase of a number of bits n approaches asymptotically T/m.

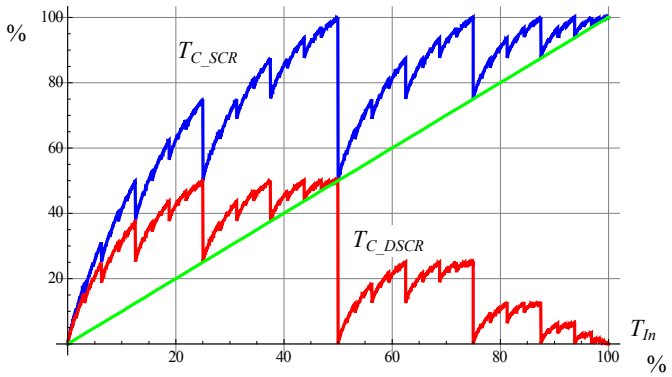

Figure 4. The normalized conversion times T_{C_SCR} (blue line) and T_{C_DSCR} (red line) vs. normalized input time interval width T_{In} according to (7), and (12) for 12-bit resolution for m=1

On the other hand, the conversion time reaches its minimum value if charge redistribution process is as effective as possible. It occurs if the binary search algorithm allows to find directly the appropriate destination capacitors without transferring the charge to the intermediate capacitors. Such situation happens if the role of the source capacitor is kept by the input capacitor through the whole conversion cycle which corresponds to the situation when the output word contains '1's only at certain number of the most significant bits. Then, the conversion time T_{C_SCR} equals T_{In}/m excepting an extra delay due to transfer of the charge portion less than charge unit Q_n where $Q_n=V_L C_0$. Thus, the most effective charge redistribution happens when T_{In} equals $T/2m$, $3T/4m$, $7T/8m$,…, $(2^n-1)/2^n m$, respectively. Finally, the conversion time T_{C_SCR} ranges from T_{In}/m to T/m depending on the T_{In} (lower bound for T_{C_SCR} is illustrated by a green line in the plot in Fig. 1)

$$T_{In}/m \le T_{C\_SCR}(T_{In}) \le T/m \tag{9}$$

The ratio T_{C_SCR}/T_{In} of the conversion time to the input time interval reaches its maximum equal to n/m if the effectiveness of charge redistriution is low (i.e., the small charge portion less than charge unit Q_n is successively transferred through all the n capacitors $C_{n-1},\ldots,C_0$, and the role of source capacitor is changed in each conversion step). On the other hand, the ratio T_{C_SCR}/T_{In} reaches its minimum equal to $1/m$ if the effectiveness of charge redistriution is high, i.e., the large charge portion is transferred directly to the destination capacitors $C_{n-1},\ldots,C_0$ while the input capacitor C_n acts as the source capacitor during the whole conversion cycle. Thus:

$$1/m \le T_{C\_SCR}/T_{In} \le n/m \tag{10}$$

Roughly speaking, the ratio T_{C_SCR}/T_{In} may approach its maximum value n/m if all the bits $b_{n-1},\ldots,b_0$ in the digital output word are evaluated to zero, and the T_{C_SCR}/T_{In} reaches $1/m$ if all bits $b_{n-1},\ldots,b_0$ are set to one. The sum of the maximum discretized time interval width T and its conversion time $T_{C\_SCR\max}$ defines the *maximum time space* $T_{SC\_SCR\max}$ between beginnings of consecutive time intervals on the converter input that may be processed in the SCR-TDC is:

$$T_{SC\_SCR\max} = T + T_{C\_SCR\max} < T(1 + 1/m) \tag{11}$$

D. Conversion time in DSCR-TDC

The conversion time T_{C_DSCR} of the DSCR-TDC may be found on the basis of the corresponding analysis for the SCR-TDC. More specifically, the T_{C_DSCR} is smaller from the $T_{C\ SCR}$ by the duration of the accumulation phase which is simple equal to the duration of the discretized time interval T_{In}:

$$T_{C\_DSCR}(T_{In}) = T_{C\_SCR}(T_{In}) - T_{In} = \sum_{k=1}^{n}\left[b_{n-k}\frac{T}{2^k m} + (1-b_{n-k})\cdot\left(T_{In} - \sum_{i=1}^{k} b_{n-i}\frac{T}{2^i m}\right)\right] - T_{In} \quad (12)$$

The plot of the normalized conversion time T_{C_DSCR} vs. the normalized input time interval T_{In} for the 12-bit DSCR-TDC according to (12) is shown in Fig. 4 and marked with red line. The DSCR-TDC maximum conversion time equals nearly the half of the maximum SCR-TDC conversion time (compare (13) to (8)):

$$T_{C\_DSCR\max} \cong T_{C\_SCR\max}/2 = T\frac{2^n-1}{2^{n-1}m} \cong \frac{T}{2m} \quad (13)$$

The conversion time T_{C_DSCR} reaches its minimum value equal to zero if charge redistribution process is as effective as possible, i.e., if the digital output word contains '1's only at a certain number of the most significant bits (1…10…0). It happens if T_{In} equals $T/2m$, $3T/4m$, $7T/8m$,…, $(2^n\text{-}1)/2^n m$, respectively. Thus:

$$0 \le T_{C\_DSCR} \le T/2m \quad (14)$$

Similarly as in the SCR-TDC, the ratio T_{C_DSCR}/T_{In} reaches its maximum equal to n/m if the effectiveness of charge redistriution is low. Thus:

$$0 \le T_{C\_DSCR}/T_{In} \le n/m \quad (15)$$

The sum of the maximum discretized time interval width T and its conversion time $T_{C\_DSCR\max}$ defines the maximum time space $T_{SC\_DSCR\max}$ between beginnings of consecutive time intervals on the converter input that may be processed in the DSCR-TDC is:

$$T_{SC\_DSCR\max} = T + T_{C\_DSCR\max} < T(1+1/2m) \quad (16)$$

Moreover, note on the basis of (12) and (16) that:

$$T_{SC\_DSCR\max} = T_{C\_SCR\max}$$

Thus, the plot of the $T_{C\_DSCR\max}(T_{In})$ illustrates at the same time the maximum time space $T_{SC\_DSCR\max}$ between beginnings of consecutive conversion cycles in the DSCR-TDC.

Conclusions

In the most pessimistic scenario (i.e., for SCR-TDC with a single current source), the conversion time may approach the converter input range T. On the other hand, in the optimistic scenario (i.e., for DSCR-TDC with two current sources), the conversion time do not exceed $T/2m$ and may even equal zero where $m=I_b/I_a$ (Fig. 4).

References

[1] H.Y. Yang, R. Sarpeshkar, "A time-based energy-efficient analog-to-digital converter", *IEEE Journal of Solid-State Circuits*, vol. 40, no 8, pp. 1590–1601, 2005.
[2] Y. Tsividis, "Event-driven data acquisition and digital signal processing: a tutorial", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 8, pp. 577-582, 2010
[3] A.A. Lazar, E.A. Pnevmatikakis, "Video time encoding machines", *IEEE Transactions on Neural Networks*, vol. 22, no. 3, pp. 461-473, 2011.
[4] Allier, E., Sicard, G., Fesquet L., Renaudin, M., "A new class of asynchronous A/D converters based on time quantization", *Proc. of IEEE Intern. Symp. on Async. Circ. and Syst. ASYNC 2003*, pp. 196-205, 2003.
[5] K. Kozmin, J. Johansson, J. Delsing, "Level-crossing ADC performance evaluation toward ultrasound application" *IEEE Trans. on Circuits and Systems I: Regular Papers*, vol. 56, no. 8, pp. 1708-19, 2010.
[6] D. Kościelnik, M. Miśkowicz, "Asynchronous sigma-delta analog-to-digital converter based on the charge pump integrator", Analog Integrated Circuits & Signal Processing, vol. 55(3), pp.223-238, 2008.
[7] D. Kościelnik, M. Miśkowicz, "Designing time-to-digital converter for analog-to-digital conversion", *Proc. of IEEE Work. on Design & Diagnostics of Electronic Circuits & Systems DDECS 2007*, pp. 275-80, 2007.
[8] M. Jabłeka, M. Miśkowicz, D. Kościelnik, "Uncertainty of asynchronous analog-to-digital converter output state", *Proc. of IEEE International Symposium on Industrial Electronics ISIE 2010*, pp. 1692-97, 2010.
[9] D. Kościelnik, M. Miśkowicz, "A clockless time-to-digital converter", *Proceedings of IEEE Convention of Electrical and Electronics Engineers in Israel IEEEI 2010*, pp. 516-519, 2010.
[10] D. Kościelnik, M. Miśkowicz, "Time-to-digital converter with direct successive charge redistribution", *Proceedings of IMEKO International Workshop on ADC Modelling, Testing and Data Converter Analysis and Design IWADC 2011*, 2011.