

## A 6-bit 3GS/s Flash ADC in Bipolar 0.25 um for the radiotelescope SKA

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**Abstract-**A flash Analog to Digital Converter (ADC) at 3 Giga samples per second (GS/s) was developed using QUBIC4X which is a 0.25 um SiGeC process from NXP Semiconductors. The ADC has a bandwidth close to 1.2 GHz with a resolution of 6-bit. The full design employs a differential structure. The ADC uses a parallel architecture consisting of the following components: track and hold, comparators, and a fat tree encoder. An embedded test system will help us to validate the data transmission, and it is made by a Linear Feedback Shift Register (LFSR). An additive scrambler block allowed us to transmit the data without an accompanying clock signal. The core of the digital circuit is in Emitter-Coupled Logic (ECL). The input is adapted to 100  $\Omega$  differential, and the outputs use standard Low Voltage Differential Signaling (LVDS). The input voltage range is about 0.5 Volts. The complete system has a power consumption of 2.6 Watts and the Effective Number of Bits (ENOB) is higher than 4.4 at 1490 MHz.

### I. Introduction

Heterodyne receivers have generally been used in radio astronomy. It brings high frequency down to a low frequency range which can be directly treated by digital processing systems. Such a system has its associated complexity (see e.g. Fig: 1.a) with a long RF chain (LNA, filter, mixer, oscillator). An important goal is to reduce the RF chain, increase the bandwidth to directly process the received frequency (RF) of the radio receiver. In order to dramatically reduce the system complexity, the goal is to acquire the whole frequency band between 300 MHz and 1.5 GHz (UHF-L band) using only one receiver (Fig: 1.b) [1]. This band corresponds to the mid-frequency band of the SKA (The Square Kilometre Array). The Analog to Digital Converter (ADC) described here is an essential component of a phased-array radio astronomy instrument which employs a hierarchical architecture for applying phase and amplitude parameters (beamforming) in order to create a phased array of many thousand elements [2], [3]. One of the important points is the ADC which has to reach the following specification: a high sampling rate ( $> 3$  GS/s), a minimum wideband of 1.2 GHz, a 6-bit architecture using a 0.25 um technology.

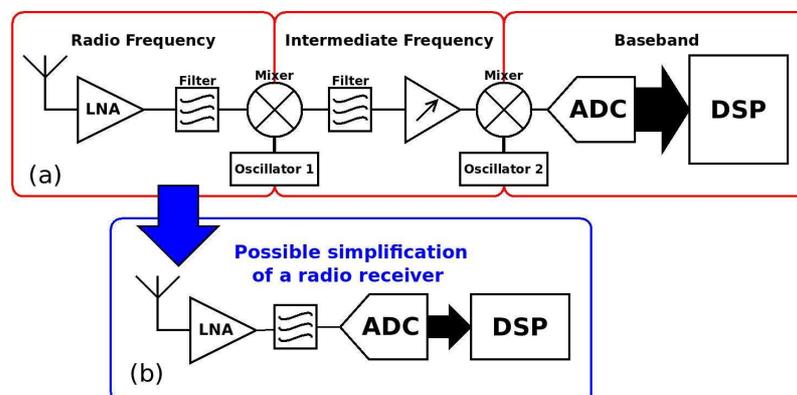


Figure 1. a. Heterodyne receiver on L-band (ADC  $\ll$  1GS/s)  
b. Simplified radio receiver L-band (ADC  $> 3$  GS/s)

### A. ADC Requirements

For this first study, one of the important requirements was the use of the 0.25  $\mu\text{m}$  technology of NXP, which is suitable for prototyping at reduced cost. This technology is used for the first prototype of the beamformer chip used on a demonstrator EMBRACE [2] (prototype receiver for the middle band of SKA). This paper presents the design, the implementation, simulations and characterizations of a 6-bit flash ADC in 0.25  $\mu\text{m}$  and its integrated test system. Its characteristics are:

- A sampling speed of 3 GS/s
- An effective resolution bandwidth (ERBW) higher than 1200 MHz
- An adapted input signal with 500 mV
- A power consumption of 2.6 Watts
- A minimum ENOB of 4.5-bit.

### II. ADC Architecture

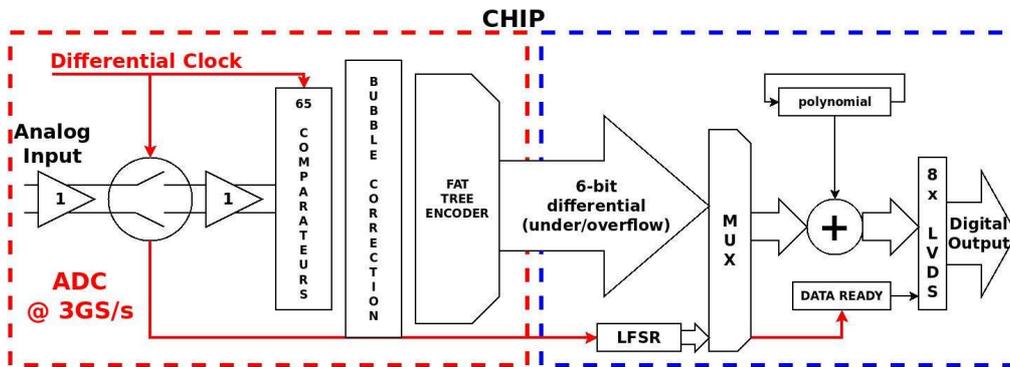


Figure 2. ADC Bloc diagramm

Our flash ADC is composed of the following stages (Fig: 2): a track and hold (T/H), comparators, a bubble correction, a fat tree encoder, a Linear Feedback Shift Register (LFSR), demultiplexer to switch with the different modes, and a scrambler to encode and transmit the bit signal at high frequency without synchronisation (data ready). Each block is fabricated in differential bipolar topology. The digital part is based on Emitter-Coupled Logic (ECL) [4] [5]. Two factors are significant: the sensibility of the comparator and the T/H accuracy in latch mode.

### B. Track and Hold

The T/H study is based on [6] [7]. The goal is to reduce the feedthrough and the droop rate, to adapt the input and to have low impedance on output. Three parts make up this T/H (Fig: 3): An input buffer, T/H (switch with a charge capacitance) and an output buffer.

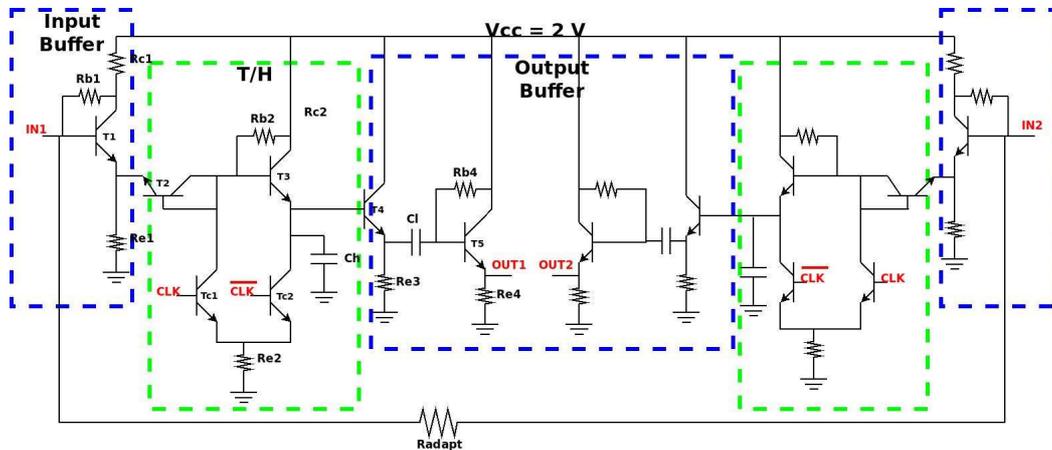


Figure 3. Differential Track and Hold

Figure 4 shows simulation results. Droop rate and the feedthrough errors were reduced by optimization. The calculated droop rate is lower than 3 mV/100 ps. The gain is equal to -4 dB. The output voltage range is about 300 mV differential. Differential architecture allows good noise isolation (figure 4.c and 4.d) and eliminates the charge injection.

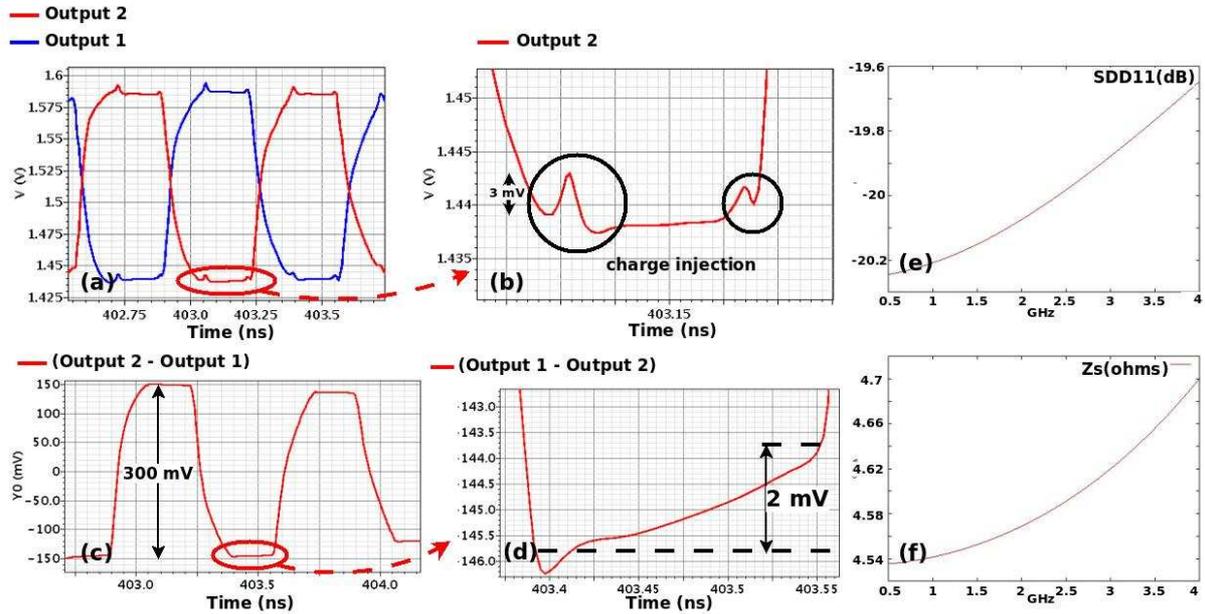


Figure 4. Output transient simulation result in single and differential (a, b, c, d), input adaptation and output impedance of track and hold (e, f)

### C. Comparators

The comparator uses ECL D-Latches and pre-amplifier. Fig: 5 shows the electrical architecture of the comparator. The pre-amplifier has a large bandwidth and provides sufficient gain to obtain a large voltage. Using a Monte Carlo statistical analysis, a yield higher than 90% is obtained at 3 GS/s for a quantum of 1 mV in the worst case. This predicts a good operation for 2 mV detection (300 mV input range). The high transition frequency of the bipolar process makes it possible to achieve this frequency rate with reasonable power consumption. Following [8] which explains the trade-off between accuracy, speed and power in CMOS ADC, the following equation is derived for application in the bipolar process with equivalent process-dependent parameters:

$$\text{Accuracy}^2 = \frac{1}{A \times \text{Speed}} \cdot \text{Power} \quad (1)$$

Where A is a process-dependent parameter.

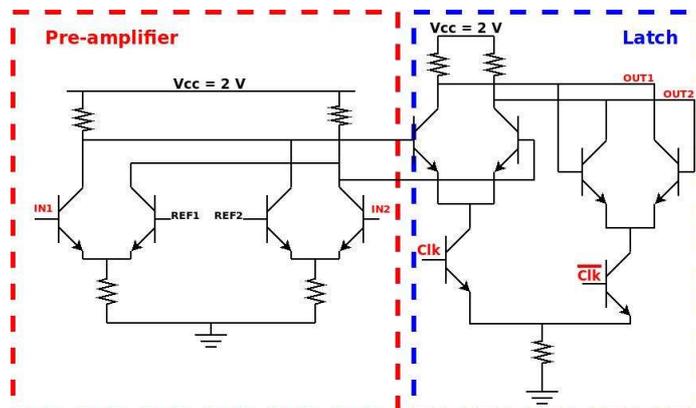


Figure 5. Comparator schematic

The ladder comparator is composed of 65 comparators, with overflow and underflow to prevent clipping. The ladder comparator is divided into 8 parts with each one having a buffer for the clock to increase the matching impedance. The ladder resistance is composed of low value resistors in order to match with the comparator. A value of 2 ohms is used for a unit resistance to decrease noise.

#### D. Digital and Test system

The digital part of the ADC is composed by a Bubble Correction (BC) and a Wallace Tree Encoder (WTE). The synchronization is improved by adding a D-Latch between the BC, the WTE, and the output digital part. The latch architecture is similar to the latch employed in the comparator structure. A test system is integrated on chip to evaluate the transmission to the data acquisition board. A LFSR is also integrated in the circuit for test purposes. The output data can be scrambled allowing the possibility to use Clock Data Recovery (CDR) at the output without sending the clock itself. The transmission can be tested without using the ADC.

### III. ADC Layout

The layout is designed with the overall goal of minimizing cost. The layout is divided into sectors that are isolated by a guard ring. Each ladder resistance is composed of ten resistances for improved matching. The comparator ladder is symmetrically divided into 2 blocks to reduce the area on chip. The clock is distributed symmetrically with clock regeneration for each 8 comparators to improve the matching. LVDS are integrated in Output logical pads. The ADC layout with pads has a total area of 4.25 mm<sup>2</sup> (fig: 6). Table 1 shows specifications of the SiGeC ADC.

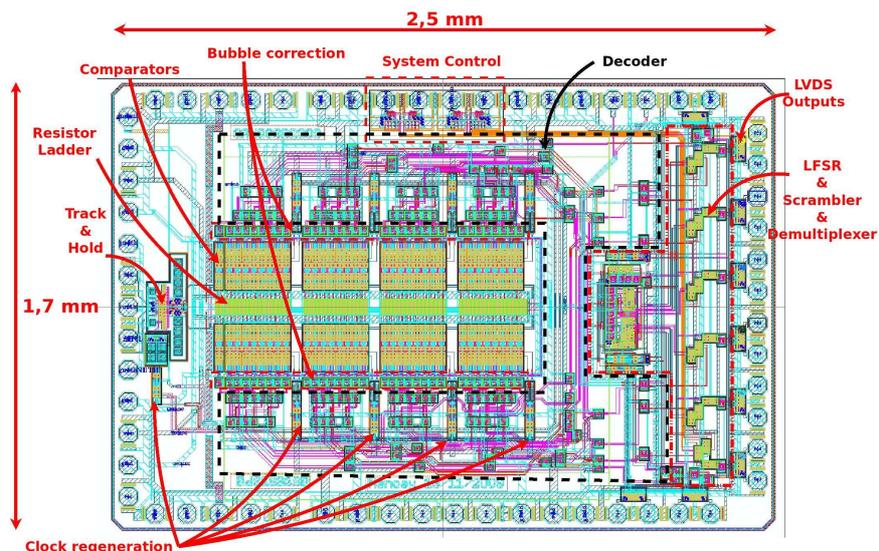


Figure 6. ADC layout

Process	0.25 $\mu\text{m}$ bipolar QUBIC4X
Input range	0.5 V
Sampling rate	3 GS/s
Bandwidth	1400 MHz
Supply voltage	2.5 V (T/H) 2 V (ADC and digital)
Total power dissipation	2.6 W
Die area with pads	4 mm <sup>2</sup>

Table 1. Specifications of the SiGeC ADC

A summary of the power consumption is shown in figure 7. Consumption is mainly due to the number of comparators and to the number of logic gates used in the digital logic.

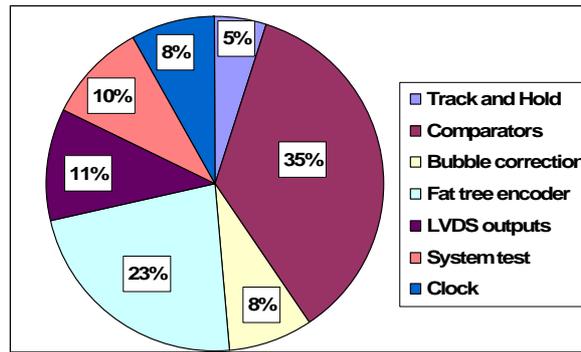


Figure 7 Consumption diagram for 2.6 W

#### IV. Simulation and Measurements

Static and dynamic parameters have been characterized in simulation. Dynamic parameters were computed with 700 point time resolution. The resistance and capacitance parasitic extraction simulation predicts an effective number of bits (ENOB) higher than 4.8 bits at 100 MHz to 4.4 bits at 1490MHz (Fig: 8). The static performance analysis of the flash ADC gives a DNL (Differential Non-Linearity) and INL (Integral Non-Linearity) smaller than 0.6 LSB predicted by simulation. The static performance shown in figure 9.

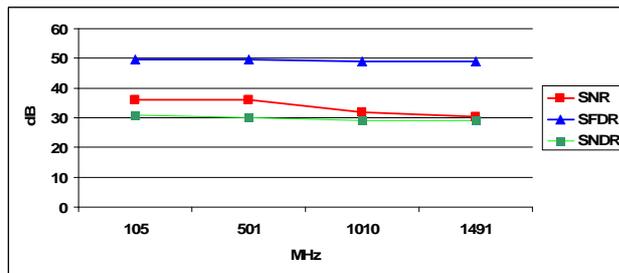


Figure 8 Dynamic results

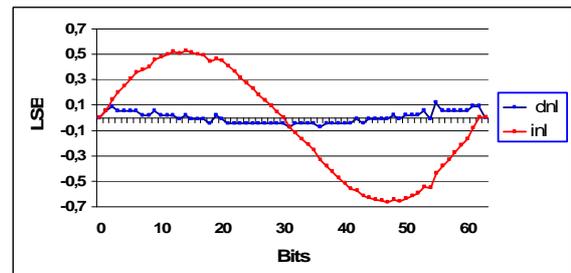


Figure 9 Static results

Testing of the ADC chip is ongoing since its delivery on date. The first test bench measured direct acquisition from the ADC board, which consists of grabbing raw data directly from each ADC bit without using any external demultiplexers. For the output data transmission we use optical fibers connected directly to the data acquisition board (Xilinx Virtex 6 FPGA board) using SFP+ connectors to evaluate static and dynamic parameters. The data transmission has been validated with LFSR at 3.125 GHz (18.75 Gbit/s for the six digital outputs). A significant configuration has been achieved in our FPGA firmware; especially for the data alignment, which was performed with a suitable calibration of our Xilinx RocketIO block in order to synchronize and to improve the BER for each binary data coming from the ADC chip. Figure 10 shows the first results of our ADC code for an input frequency at 100 MHz and a clock frequency at 2.5 GS/s (15 Gbit/sec). Errors and glitches appear in the received data. Misalignments of binary code are made and statics and dynamics parameters are not defined.

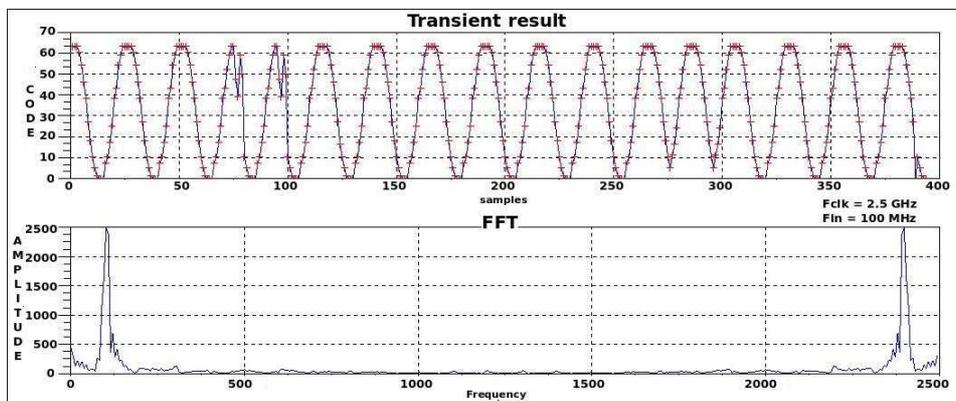


Figure 10 Result at 2.5GS/s with 100 MHz input frequency

Another test bench will be made in a few months with demultiplexer 1 to 8 to reduce the data rate on outputs. Each ADC bit will be connected to a demux chip, in order to compare the ADC data with the results obtained during the previous data transmission method.

## V. Conclusions

The Flash ADC operates at 3 GS/s with an ENOB > 4.4 bits for input frequencies up to 1.49 GHz in simulation. The ADC was produced with the 0.25 um QUBIC4X technology of NXP and it consumes 2.6 Watts. Further tests will be done to define the performance of the ADC. Efforts will be made to reduce the general power consumption in a next generation chip. To achieve this goal, a folding and interpolating analog to digital converter will be studied.

## References

- [1] P.J.Hall, The square Kilometre Array: An International Engineering Perspective, *Experimental Astronomy*, October 2004.
- [2] M Ruiter E Van Der Wal Embrace, A 10000 Element Next Generation Aperture Array Telescope, *European Microwave Conference 2009*, pp. 326-329, September 2009.
- [3] S.J Wijnholds, G W Kant, E Van Der Wal , Phased Array Results zith the first thousand Elements 2010, in proc , Prentice Hall Inc., *Wide Field Science and technology for the SKA*, Astron ISBN 978-90-805434-5-4.
- [4] Stephane Thuries, Conception et integration d'un synthetiseur digital micro-onde en technologie silicium SiGe:C 0.25 um , *PhD Thesis.*, december 2006.
- [5] Samad Sheikasei, Shahriar Mirabbasi, Andre Ivanov An encoder for 5 GS/s 4-bit flash ADC 0.18 um CMOS , *CCECE/CCGEI*, Saskatoon, May 2005.
- [6] Yevgen Borokhovych, Hans Gustat, Bernt Tillack, Bernt Heinemann, A low power, 10 GS/s Track and Hold Amplifier in SiGe BiCMOS Technology , *Essirc* v61.
- [7] Andrea Boni, Matteo Parenti , A 1GS/s 2.7V Track and Hold Amplifier with 10-b resolution at Nyquist in SiGe BiCMOS, *ESSCIRC* 2002.
- [8] Koen Uyttenhove, Michel S, Steyaert, Speed Power Accuracy Tradeoff in high speed CMOS, *IEEE*, 2002.