2011 International Workshop on ADC Modelling, Testing and Data Converter Analysis and Design and IEEE 2011 ADC Forum
June 30 - July 1, 2011. Orvieto, Italy

A 1-V 416-nW Fully Integrated Sensor Interface IC for Pacemakers

Salim Alahdab[1], Reza Lotfi[2], and Wouter A. Serdijn[1]

[1]Biomedical Electronics Group, Electronics Research Laboratory
Faculty of Electrical Engineering, Mathematics, and Computer Science
Delft University of Technology, the Netherlands
[2]Ferdowsi University of Mashhad, Mashhad,Iran
salim.alahdab@gmail.com, rlotfi@ieee.org, w.a.serdijn@tudelft.nl

***Abstract*—** An ultra-low-power, low-noise sensor interface IC for pacemakers is presented. The proposed architecture is designed to achieve small chip area and a good trade-off between power consumption and noise figure by using current-mode operation. The IECG signal, from 50mHz-100Hz, is first filtered by a bandpass filter. Subsequently, the signal output of the filter is converted into a current by a nonlinear transconductance (Gm) cell. The output of the Gm-cell is digitized by a nonlinear 8-bit 1kS/s Current-mode Successive Approximation ADC to compensate for the nonlinearity of the Gm-cell. The simulated input-referred noise is 5.48µVrms, achieving a Noise Efficiency Factor of 3.3, and the simulated power consumption for the overall system is 416 nW while operating from a 1 V supply.

I. INTRODUCTION

When the heart does not function properly, an artificial pacemaker is needed to correct the heart's contraction. However, more functionality at a limited power budget requires less power per function.

Therefore, the power consumption of the front-end, (sense amplifier), of the pacemaker has to be reduced. The design of an ultra-low-power sensor interface is a very challenging task due to the fact that the intracerdiac electrogram, IECG, is a very weak signal (1-5mV) at very low frequencies (50mHz-100Hz).

A significant amount of research has been dedicated to seeking ways to solve the above-mentioned challenges. A MOS bipolar pseudo-resistor used to filter such low frequencies was reported in [1], [2], [3]. These designs required a high supply voltage and consume relatively large power, yet result in relatively high Noise Efficiency Factor (NEF). A 1V 2.3 µW biomedical signal acquisition IC was introduced in [4], where a sample and hold circuit has been inserted into the output stage of the OTA to reduce the power. However, a high ADC clock rate is required to minimize the error caused by the switching of the output stage. A 895nW, 1V sensor interface IC for wearable biomedical devices was introduced in [5].

To reduce the power consumption even further, in the present paper, a new architecture for a sensor interface circuit for pacemakers combines ultra-low-power operation with low noise by using a non-linear current-mode ADC.

The paper is organized as follows: In Section 2, the proposed system architecture is discussed. In Section 3, the design details of each individual circuit block are explained. Simulations results and comparisons with previously published works are provided in Section 4.

II. SYSTEM ARCHITECTURE

In order to construct a bio-signal interface for wearable or implantable medical devices, a low-noise amplifier and a successive approximation register (SAR) ADC should be used [4], [5]. A SAR ADC consumes the lowest amount of power because it does not use an Operational Amplifier. A current-mode ADC is used because its power consumption is proportional to the full scale current input; the lower the full scale current input the lower the power consumption. Moreover, its chip area could be made smaller. No capacitors are used in the DAC, and thus it can be made very small compared to a voltage-mode SAR ADC [6].

Since the input referred noise of the whole system depends on the noise of the front-end, the gain of the bandpass filter is set such that the noise of the subsequent stages becomes negligible without increasing the chip area [1], [2], [3], [4], [5]. The output voltage of the bandpass filter is converted into a current by a non-linear Gm-cell that has the lowest power consumption compared to other techniques. The nonlinearity of the Gm-cell is compensated for by a non-linear DAC in the SAR ADC as shown in Fig. 1.

The SAR ADC is designed with a unary-weighted current source array serving as digital-to-analog converter (DAC). The sampled output current of the Gm-cell is compared to the reference current by a current comparator. The non-linear DAC compensates for the nonlinearity of the Gm-cell without increasing the power or the noise.

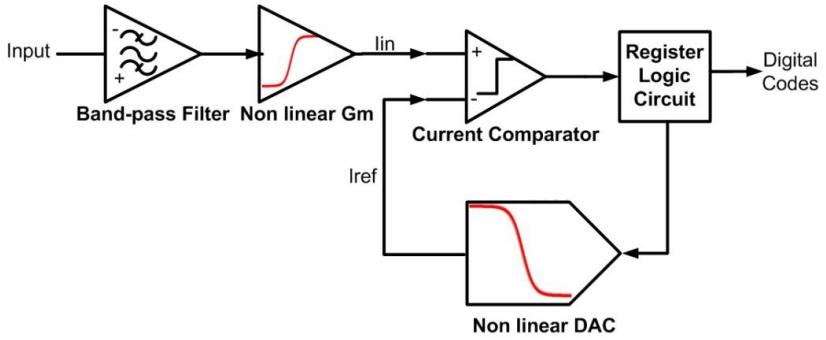

Figure 1. Proposed system architecture of the sensor interface.

III. CIRCUIT IMPLEMENTATION

A. Bandpass Amplifier/Filter

The schematic of the front-end amplifier/filter is shown in Fig. 2. It employs a capacitance feedback topology which is implemented by a two stage miller-compensated opamp. Using PMOS Pseudo-Resistors operating in their deep triode region creates a differential resistance in the order of 1T. A PMOST is chosen since the hole mobility is one-half to one-fourth of that of the electron, leading to larger resistance with similar dimensions. Two PMOSTs in series are chosen to reduce distortion for large output signals. Using pseudoresistors MT1-MT2 and MT3-MT4, the amplifier can filter low cutoff frequencies below 1 Hz without using any bulky external capacitors. Controlling the gate of the PMOST by a voltage source gives the required differential resistance without any additional circuit technique.

The major noise source of the IECG bandpass filter is flicker noise [1], [2], [3]. A PMOST input stage is chosen since it has lower flicker noise. The flicker noise is reduced by increasing the resultant product of length and width of M1-M2 [1], [7]. M3-M4 serve as a differential cascode stage to reduce the offset due to leakage and to reduce 2nd-order harmonic distortion [4]. The value of the DC voltage connected to M3 and M4 is 70mV. A Miller capacitor, C_{miller}, is used to allow more control over the high cutoff frequency as the gain bandwidth product is a function of C_{miller}. Choosing the gain to be of the amplifier 20dB rather than 40 dB relaxes the linearity requirements of the pseudoresistor element and reduces the chip area by using a smaller feedback capacitor C1 [2]. C1, MT3 and MT4, which are connected to the gate of M2, are implemented to allow the rejection of expected DC potential differences of the input signal [3]. The input referred thermal noise voltage of the opamp can be calculated from Eq. 1.

$$\overline{V_{in,thermal}^2} = \frac{8\,K\,I_D\,(nKT/q)^2}{I_D^2} \tag{1}$$

Apart from this noise voltage, the input current noise has to be taken into account as well. The higher the value of the input capacitor (C2), the lower the effect of this input current noise. In [1], [2], [3], [4], a large C1 was chosen to lower the current noise and the equivalent input noise voltage noise. However, these proposed designs chip area would be larger, especially with a Metal Insulator Metal capacitor.

As the supply current decreases, the total noise increases. The input referred noise voltage in this design was limited by the power consumption of the bandpass filter. The power consumption is set to be around 100nW, which is the typical power consumption of a two stage Miller opamp for IECG signals [4], [8]. The power consumption is mainly controlled by ID_1 and I_{out}. ID_1 is controlled by M1-M2, as shown in Fig. 2. Output current, I_{out}, is calculated to minimize the power and to be sufficient to drive the load connected to the filter, being a Gm-cell. M7-M8 were sized to deliver the required current and to minimize the noise by increasing the size aspect ratio. I_{bias} was chosen to be 30nA. The aspect ratios of M5, M6, M9 and M10 are increased to minimize the noise. The 100nW power consumption gives a total input referred noise voltage of about 5.48μV, leading to a NEF of 3.3.

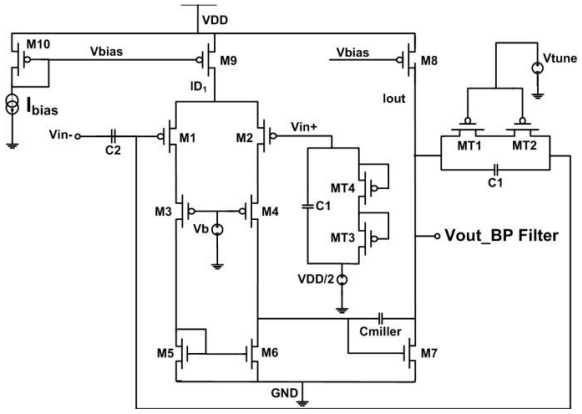

Figure 2. Schematic of the front-end amplifier/filter.

B. Operational Transconductance Amplifier

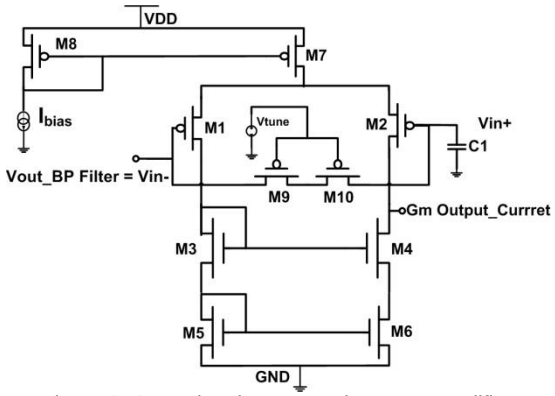

Figure 3. Operational Transconductance Amplifier

Fig. 3 shows the schematic diagram of the Operational Transconductance Amplifier used in the non-linear Gm stage. The output of the filter is fed to the Vin- input, and to the Vin+ input. In order to pass the DC component, 500mV, only, the signal fed to Vin+ goes through a very low-frequency filter, and thus ensures correct biasing.

The structure of the low-frequency filter is very similar to the one in the amplifier/filter. A cascode current mirror is used to ensure that the output current is mirrored accurately. The characteristic of the nonlinearity of the Gm is a hyperbolic tangent. The nonlinearity is compensated for in the current DAC. Using this simple Operational Transconductance Amplifier structure yields a low power consumption of 61nW with low noise.

C. Analog-to-Digital Converter

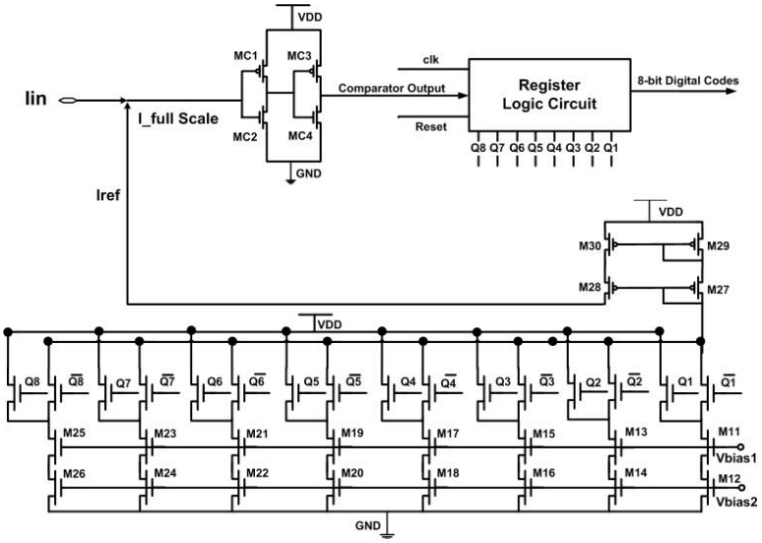

Figure 4. Circuit diagram of SAR ADC.

Fig. 4 shows the structure of the designed 8-bit currentmode SAR ADC. The current difference between Iin and Iref charges the input gate-to-source capacitance of the first inverter (integrating comparator), MC1-MC2. The second inverter, MC3-MC4, changes the sign of the output of the first inverter to have the same polarity as I_full Scale. Iref is obtained from the current DAC.

For the nonlinear (Tanh) current steering DAC, the optimal quantization levels obtained from Matlab simulation are [1, 2.26, 4.1, 7.95, 16.211, 31.8, 63.8, and 127.9]. These quantization levels are implemented by changing the aspect ratios of the current mirrors of the DAC. The current output of the nonlinear DAC is mirrored by PMOS current mirror M27-M30. Transistors M27-M30 are sized so as to give enough swing for the DAC.

M9-M26 are sized to provide the quantization levels of the non-linear DAC. The current sources are connected to complementary switches connected to the supply voltage (VDD) in order to reduce the leakage current when the switches are off. When one branch is active, they ensure that there is no static current flowing in the inactive branches. An NMOS current mirror is chosen for the DAC since it has a smaller subthreshold slope than a PMOS version in order to have a larger gain [7]. The closer the sub-threshold slope to ideal value, 1, the larger the gain.

As shown in Fig. 5, the input current (Iin) is sampled by a current-mode sample and hold (MS1, MS2, M1-M8, and C1) [6]. A CMOS switch is used to provide enough conduction, as the terminal voltages are neither close to V_{DD} nor V_{SS}. Also, the use of a CMOS switch reduces clock feedthrough and charge injection.

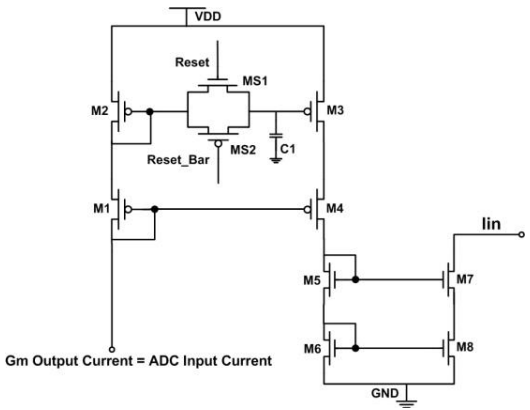

Figure 5. Input Current of ADC

As shown in Fig. 6, M1-M4, M7 and M8 are used to generate gate bias voltage (Vbias1) [9]. M7 is diode-connected. M8 is sized to create a Vds sufficient to keep M9 and M10 in the saturation region. M1-M4 are sized to produce 1LSB=100pA from the current source of 1nA. M4-M5 are used to generate mI_DAC to bias M7 and M8.

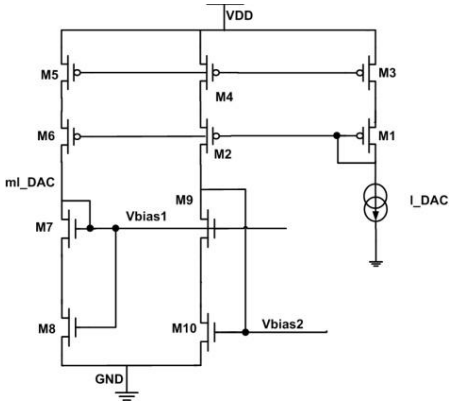

Figure 6. Bias Voltage of ADC

The matching between transistors in this design is generally not critical because any mismatch and its consequent gain error can be easily compensated for by adjusting I_DAC during device calibration. However, a careful matching between transistors M11-M26 is important because it can affect the accuracy of the ADC. The widths of transistors M11-M26 increase from LSB to MSB. Therefore, matching in the MSB transistors is better compared to that of the LSB transistors, as desired [6]. One of the main advantages of a current-mode SAR ADC is the ability to control the power consumption by I_DAC=1LSB according to Eq. 2; the lower the I_DAC the lower the power consumption of SAR ADC, as long as the noise and accuracy requirements are satisfied.

$$\text{Total Power} = (I_{fs}.V_{DD})_{Comp} + [(1\ \text{LSB} + \text{mLSB} + I_{fs})V_{DD}]_{DAC} + P_{logic} \quad (2)$$

1LSB is set to be 100pA. Full scale current, I_fs, is 25.5nA for the 8 bit-current SAR ADC. Power consumption of the logic circuits, P_{logic}, is 200nW, which can be reduced by optimizing the logic circuits. m is equal to 5 to provide enough voltage swing for M7 and M8.

IV. SIMULATION RESULTS

The design is simulated using IBM 0.13µm CMOS technology parameters. The temperature is set to 37^{o}C, being the temperature of the human body. All transistors operate in weak inversion.

A.Filter/Amplifier

The magnitude of the frequency response, the input referred thermal noise power spectral density and the frequency integrated input referred thermal noise are respectively simulated and shown in Fig. 7, Fig. 8 and Fig. 9. The simulation results yielded a bandwidth ranging from 20mHz~111Hz with a midband gain of 19.51dB. The input referred noise of this design is calculated from the output squared noise voltage divided by the squared bandpass gain. Then, the result of the division is integrated over the signal bandwidth, from 50mHz to 100Hz. The noise voltage equals 5.48 µV.

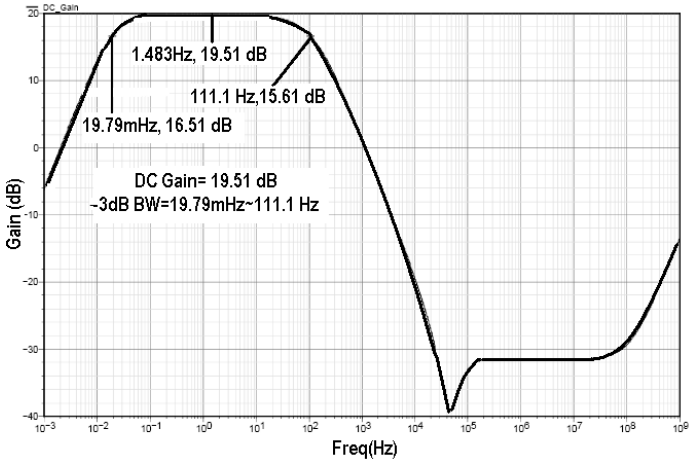

Figure 7. Bandpass Filter Frequency Response

B. Analog-to-Digital Converter

The linearity of the SAR ADC was simulated using a full scale ramp signal lasting 2.048 seconds. The result is shown in Fig. 10. The input referred thermal noise of the ADC, simulated from 50mHz to 100Hz, equals 51pA, which is less than 1LSB. Therefore, SNDR almost equals THD^{-1}. The simulation results of this work have been compared with other state-of-the-art designs, as listed in Table. I. The power consumption of the SAR ADC alone is just 255nW.

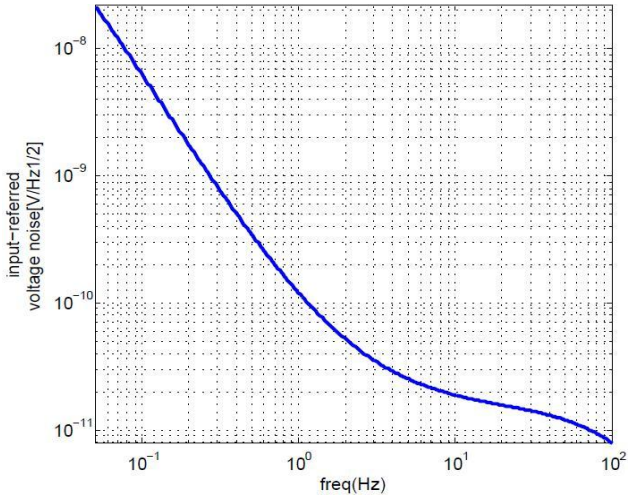

Figure 8. Input referred thermal noise power spectral density of Bandpass Filter

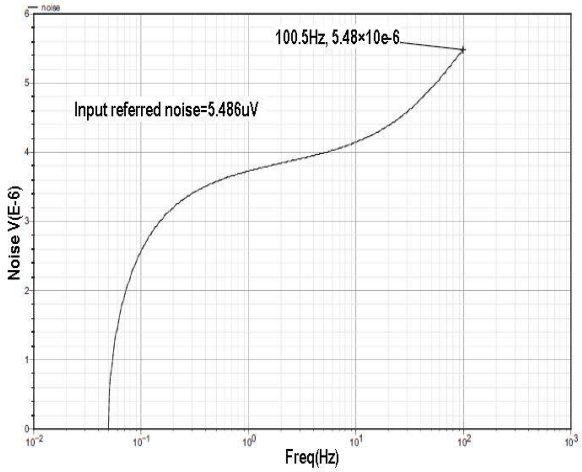

Figure 9. Input referred thermal noise of Bandpass Filter integrated from 50mHz to 100Hz

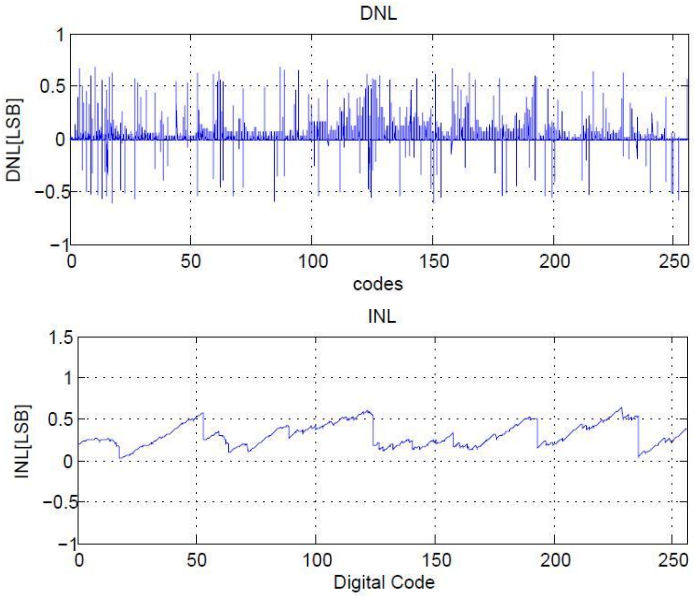

Figure 10. DNL and INL of ADC with non-linear DAC

C.System Simulation

Each block of this design has sufficient power consumption to minimize the overall noise. Even though, as shown in Table. I, the power percentage of the 8-bit ADC is higher than that of the ADC presented in [5], approximately each bit in this work consumes only 32nW, while in [5] each bit consumes 42.7nW. The estimated chip area of this work is much less than [5] because a current SAR ADC does not require capacitor array like a voltage SAR ADC. The THD is calculated to be -46.81, dB which is reasonably close to the ideal value of -49.98dB. However, if a linear DAC were to be used, the THD would be -42.32 dB.

Parameter	Design in [1]	Design in [2]	Design in [4]	Design in [5]	This work
V DD(v)	±2.5	±1.7	1	1	1
Process Technology(μm)	1.5	1.5	0.35	0.35	0.13
Active Area(mm2)	0.16	0.201	1	1	≈0.177 [4,9]*
Mid-band Gain(dB)	39.5	39.3	40.2	45.6/49/53.5/60	19.51
BW(Hz)	0.025~7.2K	0.015~4K	0.003~245	0.05~292	20m~111
Input referred noise(μV)	2.2 (0.5~50KH)	3.6 (20~10KHz)	2.7 (0.05~250Hz)	2.5 (0.05~31\292)**	5.48(0.05~100)
NEF	4	4.9	3.8	3.26	3.3
Sampling Rate	-	-	1kS/s	1kS/s	1kS/s
Resolution(bit)	-	-	11	12	8
THD(dB)	-	-	-	-	46.81
DNL(LSB)	-	-	±1.5	±0.8	< ±0.6152
INL(LSB)	-	-	±2	±1.4	< ± 0.637
ENOB	-	-		10.2	7.483
FOM(J/Conv)	-	-	-	0.197p	0.6580p
Power Distribution [front-end amplifiers,ADC](W)	-	-	330n(14,34%),1,.97 (85,65%)	429n(48%), 512.2n(52%)	161n(38,7%), 255n(61,29)%
Total Power Consumption(W)	80μ	27.2μ	2.3μ	895n***	416n

*Estimated chip area . **The bandwidth of the input referred noise is not specified, narrowband (31Hz) or wideband (292Hz). ***The power consumption is 450 for narrowband ECG.

Table I. Comparison between this Work and Recent Published Works

Clearly, due to the nonlinearity compensation in the non-linear DAC, an improvement of around 4.5 dB over the linear DAC is obtained. In other words, implementing a non-linear DAC reduces the harmonic distortion caused bythe nonlinearity of the Gm block effectively.

D.Monte Carlo and Process Corner Simulation

To have an indication of the reliability of the design and the efficacy of using a non-linear DAC, process corner simulations have been conducted. The results for THD of the combination of the Gm block and the ADC with a non linear DA are presented in Table. II.

Process Corner	THD(dB)
TT	-46.81
FF	-44.83
SS	-42.32
FS	-45.76
SF	-41.75

Table II. Process Corner Simulations of Gm Connected to ADC with Non-Linear DAC.

The THDs of FS and SS deviate the most from the THD at the typical corner (TT), being 48.81 dB. The performance at FS and SS corners could be enhanced by optimizing the current mirror in the DAC. The results in Table II prove that the non-linear DAC effectively compensates for the nonlinearity of the Gm block over all process corners.

A Monte Carlo Simulation has been done with 5 runs for the overall system. The number of runs could be increased but the simulation time is very long, in the order of days. The mean value of the THD is -44.936 dB. The mean is only 1.864 dB less than the simulated typical value. The highest value is -46.55dB and the lowest value is -42.83 dB.

V. CONCLUSIONS

In this paper, a 1-V 416-nW fully-integrated sensor interface IC for pacemakers is presented. The proposed design shows improvements in various aspects compared to other recent works. The power consumption of the whole system is 416nW which is 46.5% of the previously lowest reported design with comparable performance for ECG applications. The bandpass filter achieves a NEF of 3.3, which is very close the lowest NEF reported in the literature (of 3.26). Choosing the gain to be 20 dB relaxes the MOS pseudoresistor design. To save power, a conventional Gm-cell is designed to convert the voltage into a current with low power consumption. A nonlinear current SAR ADC is designed to compensate for the nonlinearity of the Gm-cell and thereby reduce the overall power consumption.

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